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# ANALOG AND DIGITAL-MULTISTAGE TIME-AVERAGING FILTERS

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# I. DIGITAL TIME AVERAGING FILTERS

## A. Introduction

In time measurements involved in the detection of elementary particles using large counters, the time uncertainty introduced by the finite propagation velocity of the produced signal may be significant compared to the desired time resolution.

Here, a novel method is introduced to drastically reduce this effect,[1] whose essential ingredients are the time properties of delay lines and AND and OR logic gates.

Consider a counter of length L with light collected at both ends by photomultiplier tubes. If the light-signal propagates in the counter with an effective velocity v, then the time for the signal to travel from one end to the other is

$$\Delta t_0 = L/v \quad .$$

If a particle traverses the counter at a distance L = x with respect to one end of the counter, the event will be perceived at times $t_1$ and $t_2$ by the two photomultiplier tubes, represented by lines $S_1$ and $S_2$ in Fig. 1 where

$$t_1 = t_0 + x/v, \quad t_2 = t_0 + \frac{L-x}{v}$$

and $t_0$ is a constant determined by the time that the particle traverses the counter.

## B. Analysis of the Method

### 1. Time Properties of Logic Gates

Now, consider the two photomultiplier outputs of the counter, after suitable discrimination, as the inputs to an OR gate. The

earlier half of this time diagram will be selected at the OR gate output as indicated in Fig. 4. An AND gate will select the later half of the same time-diagram. In other words, the OR and AND gates act as "time ordering and slicing" operators,

$$t_{AND} = \max(t - \delta t_0,\ t + \delta t_0) = t + \max(-\delta t_0,\ \delta t_0) = t + |\delta t_0|$$

$$t_{OR} = \min(t - \delta t_0,\ t + \delta t_0) = t + \min(-\delta t_0,\ \delta t_0) = t - |\delta t_0|$$

where $t = t_0 + \frac{\Delta t_0}{2}$.

Therefore the time uncertainties of $t_{OR}$ and $t_{AND}$ have been cut in half.

2. Basic Circuit

The $t_{AND}$ and $t_{OR}$ time diagrams are displaced in time by $\Delta t_0/2$ with respect to each other, as can be clearly seen in Fig. 2 and also from relations (7), (8). If, however, the OR output is delayed by $\Delta t_0/2$, then the two time-diagrams will be synchronized again as the original ones in Fig. 1.

This idea is implemented in the basic circuit of Fig. 3. An OR and an AND gate are put in parallel and each of them accepts the two signals as inputs. A delay line of $\Delta t_0/2$ is put at the output of the OR gate to mix the two signals in time. The resulting time-diagram of the two outputs is equivalent to the original one, but its time uncertainty range has been reduced by a factor of 2 from $\Delta t_0$ to $\Delta t_1 = \Delta t_0/2$. In addition, the output time diagram is delayed by $\Delta t_0/4$ with respect to the input one. Here, for simplicity, we neglect the inherent delay of the OR and AND gates and of the lines carrying the signals from one to the other.

Clearly, one can consider this circuit as the single stage unit in a time uncertainty reducing filter, which could be cascaded an arbitrary number of times.

Another important property is that the time diagram range for the two outputs will have a fixed value of $\Delta t_0/2$ determined uniquely by the amount of delay at the OR gate output and independent of the input's true range, provided it is smaller or equal to $\Delta t_0$:

$$\Delta t_{in} \leqslant \Delta t_0$$
$$\Delta t_{out} = \Delta t_0/2 \quad .$$

These properties are also characteristics of other circuits which are variations of the basic circuit, as well as their combinations.

C. Synthesis of "Time Averaging" Filters

Now we consider the design of filters each of which could consist of an arbitrary number, n, of single stages in series. In each such filter, the time range of the kth stage is reduced with respect to the previous one by 2, the single stage reduction ratio,

$$\Delta t_{k+1} = \frac{\Delta t_k}{2} \quad .$$

Consequently, for an n-stage filter, we will have at the output

$$\Delta t_{out} = \Delta t_n = \frac{\Delta t_0}{2^n} \underset{n\to\infty}{\rightarrow} 0; \; \Delta t_{in} \leqslant \Delta t_0 \quad ,$$

where $\Delta t_0$ is the maximum time range of the initial input (Fig. 1).

Now, if at the last stage, n, the OR output is delayed by $(\Delta t_0/2^n)$ and fed back as an input into the AND gate of this $n^{th}$ stage,

the AND output will have a time range

$$\Delta t_{out} = \frac{\Delta t_0}{2^{n+1}} \quad .$$

By simply inspecting the time-diagram of such a filter in its next stages, one can immediately predict that the filter time delay has a maximum limit of $\Delta t_0/2$, as the number of stages increases. It is easy to prove this conclusion rigorously.

Finally, at the $n^{th}$ stage, one can prove that the two outputs will arrive at times

$$t_{n+},\ t_{n-} \rightarrow \frac{t_1 + t_2}{2} + \frac{\Delta t_0}{2} \text{ as } n \rightarrow \infty \quad .$$

Therefore, a filter acts as a "time-averaging" device of the two initial inputs apart from a fixed offset $\Delta t_0/2$.

D. A Four-Stage Filter (Implementation and Testing)

To provide improved time-of-flight resolution for Experiment E450 at the ZGS, 36 time-averaging filter channels, each consisting of four stages were built. Twenty channels were built with delay lines corresponding to a $\Delta t_0$ at 4.2 nsec and 16 channels with $\Delta t_0$ = 5.6 nsec. The logic was ECL 10000 and the delays were achieved with RG-174 cable, cut to length and soldered onto the circuit. Four channels were packaged in a single width NIM module without crowding. A schematic of the circuit is shown in Fig. 4. The RG-174 cables were cut to the calculated lengths and soldered onto the boards.

One convenient method of testing the modules was to take calibrated cables from a splitter, two cables with delays of 10 ns and two with delays of 8 and 12 ns. The output walk was measured on a Tektronix 485 scope by first setting up the system with the 10 ns cables and then switching

to the 8 and 12 ns cables and then reversing the cables.

Typically, the total walk was found to be between .1 ns and .2 ns over the range which corresponded to $\Delta t_0 = 4.2$ nsec, whereas the walk design value is

$$\Delta t_{04} = \frac{4.2}{2^5} = .13 \text{ nsec} \quad .$$

We consider this agreement good in view of the rather limited effort spent in timing each channel.

Clearly, for careful timing of the system, one must take into account the propagation delay of the ECL logic and the propagation delays on the printed board. Generally speaking, our experience was that for $\Delta t_0 \sim 4$ nsec and for filter channels of four stages, all circuits could be timed with no problem by trimming RG-174 cables.

Finally, the total TAF propagation delay due to the gates and printed circuit board lines was measured and found to be about 10-11 nsec, implying a propagation delay per AND gate of about 2 nsec.

E. Experimental Results

In Fig. 5, we show three TOF distributions, accumulated online using these TAF's during the course of the experiment. Each corresponds to an individual counter located at the indicated angle ($\theta_{lab}$) and distance (D) with respect to the incident particle direction and target position, respectively. The time axis of each distribution has not been corrected for the time offset due to the timing of the electronics. The two main peaks, observed in each distribution, correspond to pions and protons indicated with circles in the reactions shown at the upper left corner of the same figure.

The observed widths can be conveniently accounted for by using only the premeasured time resolution of the start and stop PMT's. This implies that the TAF time walk cannot be more than .1 - .2 nsec, in good agreement with our previous tests of these devices.

F. Future Applications

These TAF circuits should be extremely useful in providing on-line TOF information down to 50 psec time resolution or even lower, from counters of large dimensions. Also, they should be very useful in experiments with ultrafast decision-making logic with subnanosecond timing requirements, using signals from counters of large dimensions.

Immediate plans by our group include the use of these TAF's at Los Alamos in experiments similar to E450 and also in total cross-section difference ($\Delta\sigma_L$ and $\Delta\sigma_T$) measurements of pp and pn scattering.

In total cross-section measurements, precise timing information from the so-called transmission counters will be very helpful for a clean separation between pions, protons and deuterons.

## II. ANALOG TIME AVERAGING FILTER

### A. Principle

The problem of precise timing with a counter of large dimensions can also be solved with the following analog method.

Consider the two counter signals turning on, at times $t_1$, $t_2$, a current source of constant current I and charging a capacitor, C, set originally at a negative voltage

$$V_0 = \frac{Q_0}{C}$$

until it reaches ground at time $t_g$. An output pulse is generated then,

independent of the individual times $t_1, t_2$, since

$$Q_0 = I(t_g - t_1) + I(t_g - t_2) = I(2t_g - \Delta t)$$

depends only on the "true" time that the particle passes through the counter, where

$$\Delta t = t_1 + t_2 \sim L \text{ (length of the counter)} = \text{constant} .$$

Figure 6 shows diagrammatically the capacitor voltage dependence on time for three different cases:

(a) Passage of particle through one of the counter's edges.

(b) Passage through its center.

(c) Passage at a distance L/4 from one edge.

B. Implementation

Figure 7 shows an implementation of the Analog Time Averaging Filter which was built and tested with a large scintillation counter. The circuit accepts two NIM level inputs from the two photomultiplier discriminator channels which have presumably been timed externally. Each input turns on a current source, the outputs of which are summed on a capacitor. A trimpot is provided to allow equalization of the two current sources. The summing capacitance is provided by the Drain-Source capacitance of a VMOS FET in parallel with some external padding. The VMOS FET allows fast clearing of the charge accumulated on the capacitor. A MECL 10116 line receiver acts as a discriminator to provide timing output of the point where the capacitor voltage crosses the reference. The output is then translated back to NIM.

The circuit is quite simple and functions with adequate reliability. Instability due to dielectric absorption was not noticeable during tests with the large scintillation counter.

C. Testing

First, the circuit of Fig. 7 was calibrated using a pulser. A NIM level pulse was fed separately into each of the two inputs. The output pulse timing was adjusted, using a Tektronix 485 scope, with a pot screw placed in series with the 900-Ω emitter resistor of input A, until the output timing became the same for both inputs. Next, the circuit was tested by using two pulses, arriving at each input with different amounts of delays $t_1$, $t_2$, such that their sum $t_1 + t_2$ was kept constant. The output pulse timing was monitored with the scope. The observed time shifts for various sets of $t_1, t_2$ values were always limited with ±100 psec.

Finally, the two outputs of a two-feet long scintillation counter, after proper discrimination, were fed into the circuit. The counter's timing was tested using both a $Ru^{106}$ source and cosmic particles defined by two small trigger counters above and below the long counter.

The output signal's time-histogram was recorded using a qvt-type (LRS) multichannel analyzer for several hit-positions of the counter. The time-histogram peaks did not shift by more than ±150 psec.

D. Time Resolution and Deadtime

The time resolution of such a filter depends on the original calibration accuracy and is limited by current source fluctuations, and voltage and charge fluctuations of the capacitor.

Also, the filter's deadtime is primarily determined by the capacitor-related RC, which in our case is about .5 μsec.

## III. DIGITAL-ANALOG FILTERS

Finally, one could consider the possibility of bringing the input of an

analog filter at the output of a digital one. With such a hybrid system, one could very easily refine the timing of a large counter down to the few picoseconds uncertainty of the gates, ignoring always the uncertainties from other sources, like photomultipliers.

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Reference

1. "Multistage Time Averaging Filters for Timing Measurements with Large Counters", G. Theodosiou and J. Dawson, ANL-HEP-PR-79-40 (November 1, 1979), to be published in Nuclear Instruments and Methods.

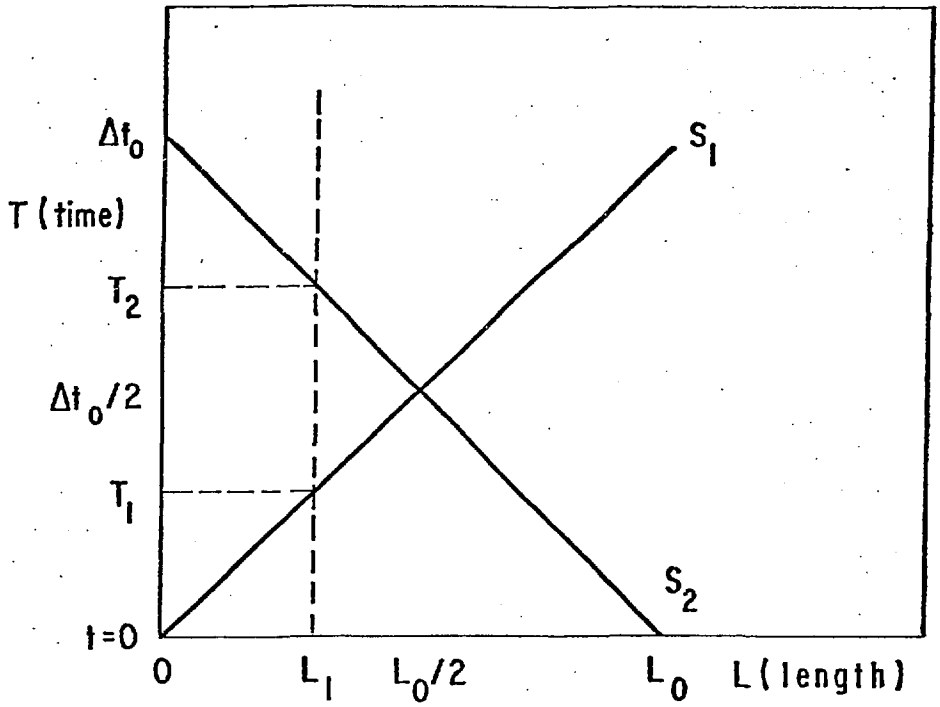


Fig. 1 The time diagrams $S_1$, $S_2$ of the two scintillation counter outputs.

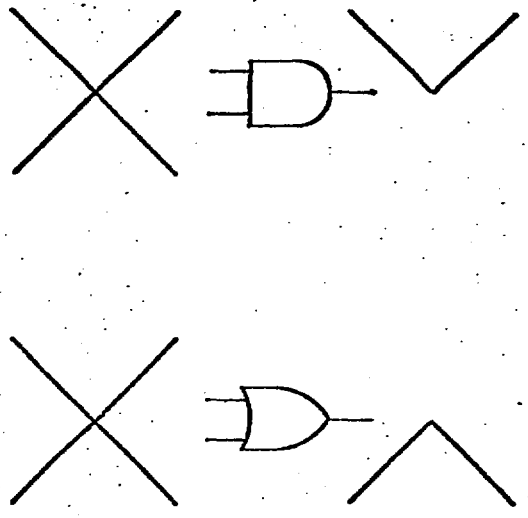

Fig. 2 Action of AND and OR logic gates on a time diagram.

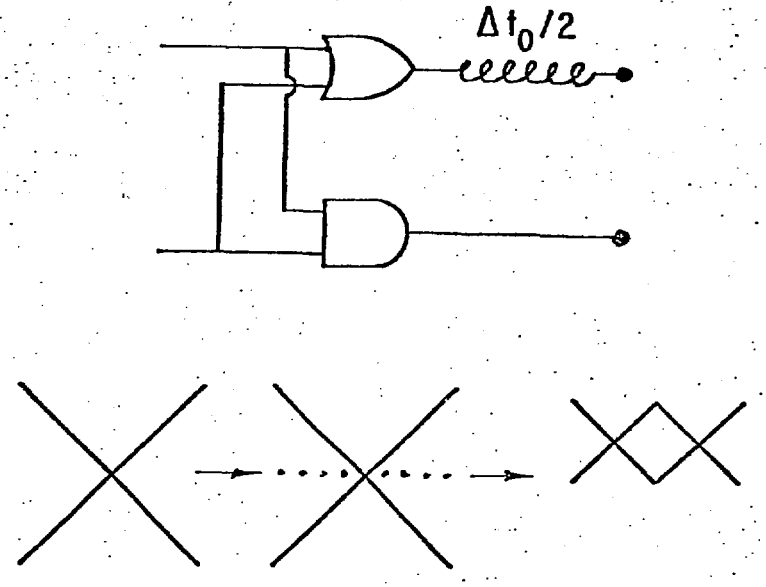


Fig. 3 Logic and time diagrams of the "basic" circuit.

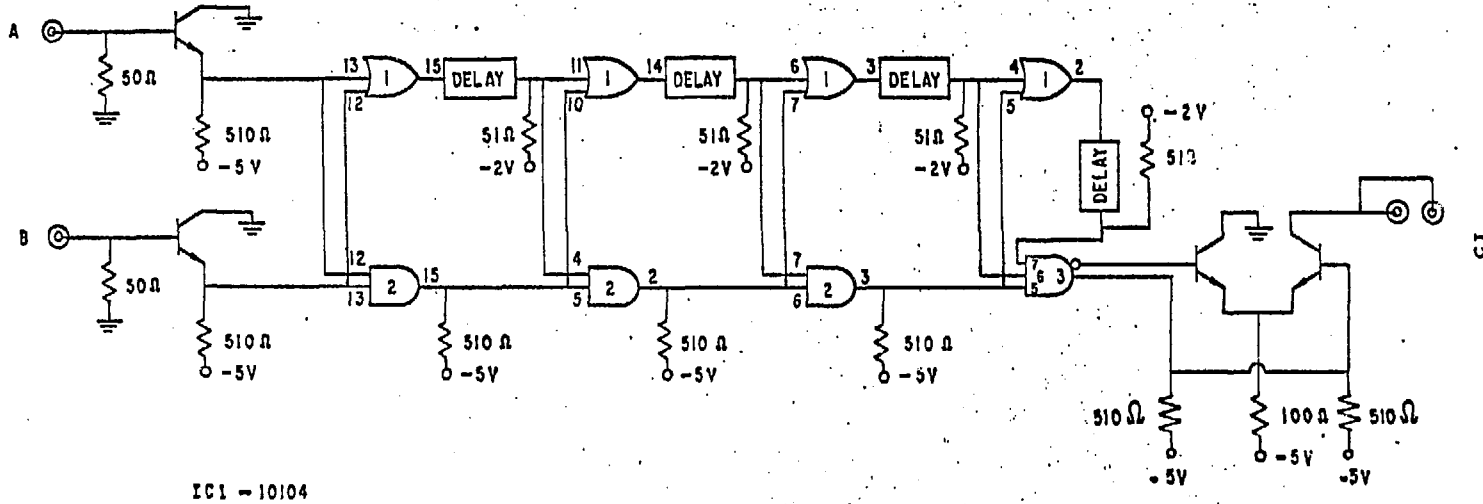


Fig. 4 Schematic of a four-stage TAF channel.

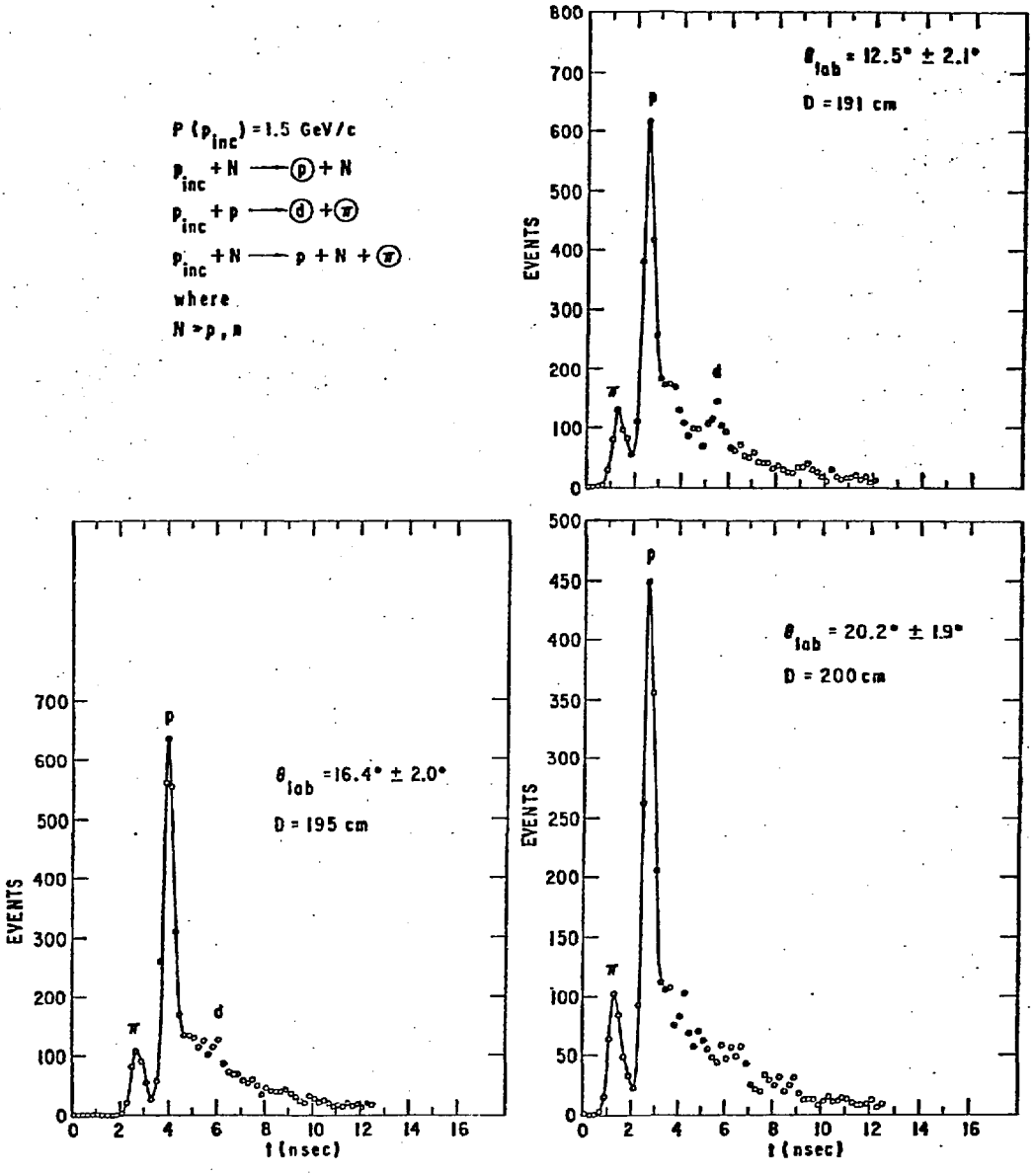


Fig. 5 TOF distributions from three different counters for particles coming from events of the pN → pN, pNπ, dπ type. Observed peaks can be identified with final state protons (p), pions (π) and deuterons (d) traversing these counters.

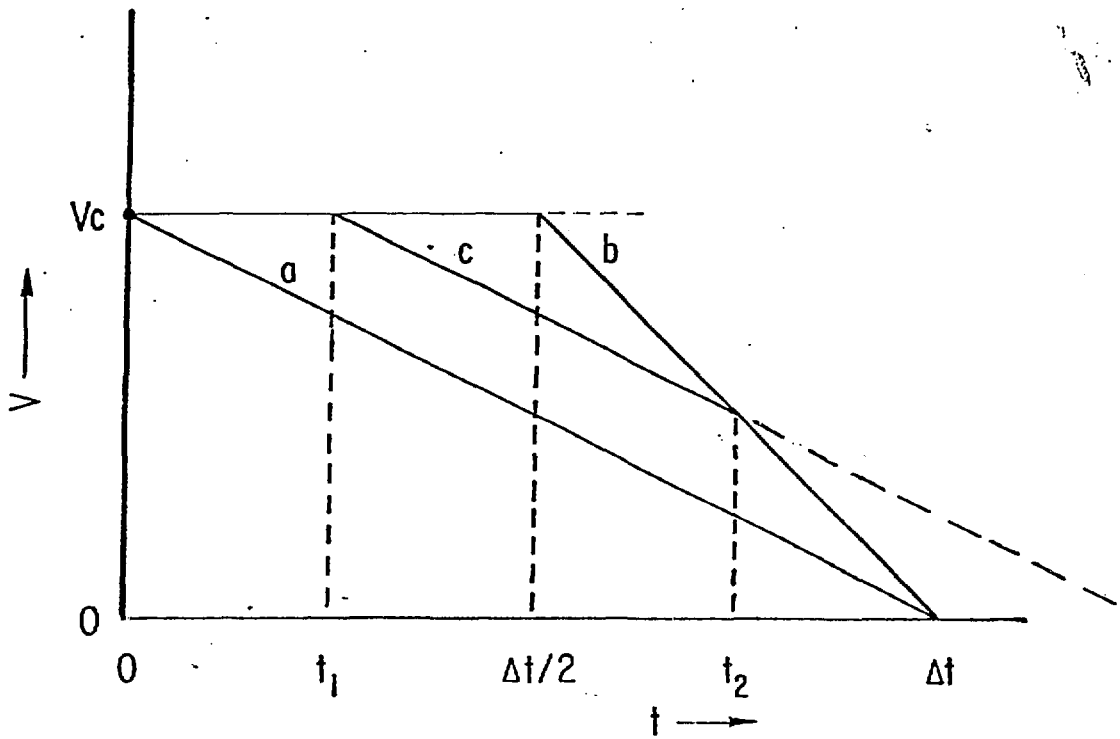


Fig. 6 Capacitor-voltage time-diagram for passage of a particle through
(a) one of the counter's edges,
(b) its center,
(c) at a distance L/4 from one edge.

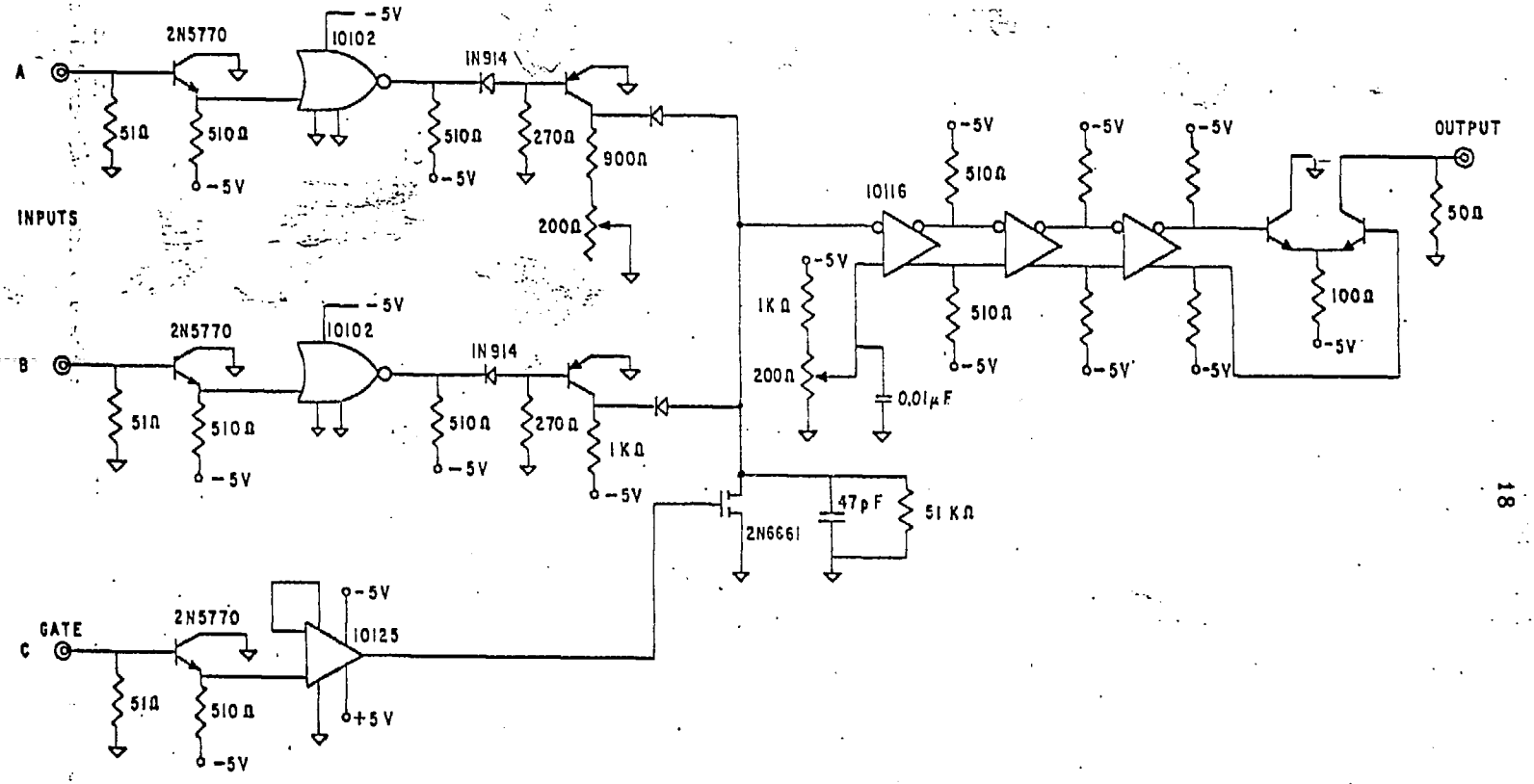


Fig. 7 Analog time-averaging filter time diagram.