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PHASE 2 OF THE ARRAY AUTOMATED ASSEMBLY TASK FOR THE
LOW COST SILICON SOLAR ARRAY PROJECT

First Quarterly Report, October 1–December 31, 1977

By

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April 26, 1978

Work Performed Under Contract No. NAS-7-100-954873

Westinghouse R&D Center
Pittsburgh, Pennsylvania



MASTER

U.S. Department of Energy



Solar Energy

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J. R. Szedon, R. B. Campbell, R. N. Ghoshtagore
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TABLE OF CONTENTS

1. Summary	1
2. Introduction	2
3. Technical Results	3
3.1 Process Sequence Analysis.	3
3.2 Junction Formation	6
3.2.1 Front Junction Preparation	6
3.2.2 Back Junction Formation	9
3.3 AR Coating	13
3.4 Cell Separation	14
4. Conclusions	22
5. Program Status	24
6. References	26
7. Acknowledgements	27

LIST OF FIGURES

1. Normalized solar cell efficiency as a function of substrate metal impurity concentration. From R. H. Hopkins et al., Ref. 2.
2. Effects of front and back surface laser scribing in the conversion efficiency of selected cells in Czochralski material.
3. Effects of front and back surface laser scribing on the fill factor values of selected cells in Czochralski material.
4. 2009-6LS Laser scribed from back -- Note metallization line; and penetration depth of scribe. Length of Scale Bar: 100 μm .
5. 2009-6LS Laser scribed from back -- Note total penetration after laser scribe dwell. Length of Scale Bar: 100 μm .

LIST OF TABLES

1. Summary of Yield and Material/Supplies Cost Estimates in 1977 Dollars for the Proposed Array Processing Sequence for Dendritic Web Silicon Solar Cells at Nominal 13% Efficiency.
2. Outline of n+/p Cell Processing Steps.
3. Cell Performance Comparison, Electronic vs. Reagent Grade POCl₃ Diffusant Sources.
4. Metallic Impurity Content (ppm) of J. T. Baker POCl₃, Reagent vs. Electronic Grade.
5. Boron Doped-Oxide BSF Calibration Experiments.
6. Effectiveness of AR Coatings Prepared from Organometallic Precursors.
7. Mean of Fraction Changes in Fill Factor and Efficiency Resulting from Laser Scribing.

1. SUMMARY

During this quarter a process sequence has been proposed and analyzed with regard to yield and cost of direct materials for fabrication. Cells of at least 13% conversion efficiency and panels of 10% efficiency have been assumed. Material costs, excluding silicon, were estimated as low as \$0.19/watt (1975). Use of the JPL Interim Price Estimation Guidelines gives a projected contribution to selling price of \$0.24/watt (1975) for the direct materials used in processing. If silicon is included, the contribution to selling price is \$0.46/watt (1975). Areas have been identified in which cost improvements might be made to meet the price goal of \$0.50/watt, including equipment and labor considerations.

Development effort during this quarter has been applied to junction formation, anti-reflection coating and laser scribing. Junction formation effort was in two areas: (1) establishing the process parameter ranges for the back surface diffusion from a boron-doped oxide and for the front junction diffusion using POCl_3 and (2) determining if the purity of the POCl_3 source material is critical to cell performance. In the latter case, no effect of purity on cell performance was detected, although the reagent grade POCl_3 contained 20 ppm of titanium (which strongly suppresses lifetime if incorporated in silicon as grown) vs. 0.02 ppm for the electronic grade.

Anti-reflection coatings of TiO_2 have been prepared on cells formed in dendritic web silicon by spin-on application of a liquid metallo-organic precursor. Achievement of 12 to 13% conversion efficiency after single layer coating was common.

Laser scribing to remove dendrites from the ribbon and to delineate cell areas has been demonstrated. The presence of photoresist, AR or metallic films on the ribbons does not significantly affect scribing. Laser scribing has been found to degrade cell performance, presumably by damaging the front collecting junction. Proper control of laser penetration during back-surface scribing is expected to solve this problem.

2. INTRODUCTION

The objective of this program is to establish a process sequence and to develop key process steps for low cost manufacturing of solar arrays from dendritic web, single crystal, silicon in ribbon form. Specifically, all costs, including web silicon at \$0.17/watt, are to be considered with the aim of producing encapsulated modules of 10% conversion efficiency for a selling price of \$0.50/peak watt in 1975 dollars.

A simplified process sequence, serving as the initial basis for development work on this program, is presented in Section 3.1 and analyzed on terms of direct materials and electricity cost contributions to module selling price.

Since dendritic web silicon can be handled as long lengths of ribbon through most of the cell fabrication steps (cleaning, junction formation, AR coating and metallization) conceptual processes for continuous processing have been proposed. In most cases, the operation of a proposed process as a continuous, rather than a batch, method should lead to lower costs in materials, equipment and labor. During the first quarter, investigations were begun on technical aspects of junction formation, AR coating and cell separation. These investigations, as discussed in Sections 3.2 through 3.4, provide a basis for determining the feasibility of key parts of the proposed process sequence.

3. TECHNICAL RESULTS

3.1 Process Sequence Analysis

Table 1 summarizes key aspects of the process sequence initially selected for development on this program. For the estimates of yield for each step (Column C) two values are given. The first is conservative, based on best estimates of current practice; the second (in parenthesis) is optimistic and is an attempt to reflect the improvements expected of a properly automated process sequence. This is expected to be of particular significance for the more complex, multi-operation step such as junction formation, AR coating and metallization.

Estimated step costs for materials and supplies (including electrical energy) to produce 13% cells are given in Column D. These have been obtained from engineering estimates of material usage in current processing. In certain cases, (e.g. back junction formation, AR coating and electroplating) the figures reflect the especially favorable economics of the proposed process schemes as applied to dendritic web silicon material. For the junction formation step, the possibility of lower cost dopant source chemicals for the front junction is treated parenthetically. The ability to achieve the program goals using this cost reduction will be assessed on the program. Costs in the AR coating step are expected to be controlled by photoresist usage. If evaporated Ta_2O_5 is used, photoresist and evaporated material costs are comparable. The use of a liquid precursor for TiO_2 should result in low costs with spray application to dendritic web silicon (treated parenthetically). Estimated metallization costs are dominated by the titanium and palladium. Cell separation costs are approximately equally affected by laser energy, photoresist and junction etching costs. Encapsulation costs are dominated by the glass (~75%) and the adhesive (~25%). The former are based on the use of two sheets of double strength glass.

Table 1 Summary of Yield and Material/Supplies Cost Estimates in 1977 Dollars for the Proposed Array Processing Sequence for Dendritic Web Silicon Solar Cells at Nominal 13% Efficiency

Step Number	Description	Estimated* Yield (%)	Material/Supplies Cost (\$/watt)		Effort on This Program	
			Step Cost	Yield Affected Cost Cconservative Optimistic		
A	B	C	D	E	F	G
01	Surface preparation	94(98)	.0115	.0172	.0136	P
02	Junction formation	96(98)	.0937 (.0177) ⁺	.1320	(.0201) ⁺	D
	Back		.0058	--	--	
	Front		.0879 (.0119) ⁺	--	--	
03	AR coating	96(98)	.0080 (.0040) [#]	.0110	.0090	D
04	Metallization	89(96)	.0265	.0345	.0295	D
05	Cell separation	96(98)	.0115	.0133	.0123	D
06	Interconnection	95(98)	.0046	.0051	.0050	P
07	Encapsulation	95(93)	.1154 [#]	.1215	.1177	P
			$\pi = 0.67(0.85)$	$\Sigma = 0.3290$	0.2077	

* Estimated yield of multi-operation steps as given; estimate for highly automated processing is given in parentheses.

⁺ Reflects lower materials cost of reagent grade POCl₃ as compared with electronic grade materials.

[#] Reflects use of a liquid precursor for the AR coating instead of an evaporated dielectric.

[#] Panel efficiency of 10% assumed.

Steps cost have been extended in Columns E and F to account for the total yield at any step of processing through encapsulation. The conservative extension (Column E) uses the conservative yield estimates of Column C and the less optimistic step cost estimates in Column D; the optimistic extension (Column F) uses the parenthesis Column C estimates and the lowest step cost figures from Column D.

Overall, the conservative materials/supplies cost estimate is about \$0.33/watt in 1977 dollars (\$0.29/watt in 1975 dollars) with the cost of silicon web at \$0.17/watt (1975) cannot meet the program price goals. The optimistic cost estimate (\$0.35/watt including silicon in 1975 terms) benefits greatly from the reduced cost of front junction formation and from the higher overall yield at that early stage in processing. This notwithstanding, the price of modules prepared using the proposed process sequence would be \$0.46/watt (1975), to account only for the silicon (at a cost of \$0.17/watt) and the direct materials.*

It is clear that a revision of the proposed sequence to lower direct materials costs is necessary for the goal to be achieved. Preliminary detailed analysis of the process sequence of Table 1 indicates that the direct material costs associated with metallization, cell separation and interconnection (steps 04, 05 and 06) should be lower than originally estimated. Of course, the largest contribution to materials costs is in the encapsulation step. Realistically, it is here that additional significant reductions in materials cost will be required to achieve the price goal of \$0.50/watt.

In Column G are indicated those steps which will receive development effort on this program. Three of those, junction formation, AR coating and metallization, involve processes whose automation appears to be especially attractive for the ribbon form of dendritic web silicon.

* The JPL Interim Price Estimation Guideline has been used with a price/cost ratio of 1.3. (1)

The fourth, cell separation is required to provide individual cells for interconnection in an array. The other three steps, surface preparation, interconnection and encapsulation will be treated only in terms of demonstrating that acceptable procedures can be used in each case to allow final fabrication of completed modules. The remainder of this first report treats technical matters associated with junction formation, AR coating and cell separation which were addressed during the first quarter of work on the program.

3.2 Junction Formation

3.2.1 Front Junction Preparation

A significant contribution to the cost of materials for cell fabrication is made by the electronic grade phosphorus oxychloride used in gaseous diffusion of the front junction. The cost of POCl_3 could be reduced to about 0.03 of the electronic grade if the reagent grade could be used. The problem in changing grades is a factor of 200 difference in the maximum specified total heavy metals content for the two grades (e.g. 0.21 ppm for electronic grade versus 40 ppm for the reagent grade). A preliminary experiment has been run to determine if cell performance is affected by the purity of the POCl_3 diffusant source.

One base line group of cells was processed using Baker electronic grade POCl_3 for formation of the front junction. For a test group of cells, Baker Reagent grade POCl_3 was used in a parallel furnace arrangement. Both groups were made using 1 to 3 Ω cm p-type Czochralski silicon from the same wafer supply lot. Except for the POCl_3 diffusion step, the wafers were merged into a single group for the other cell processing steps. A short description of the process sequence is given in Table 2.

TABLE 2

Outline of n+/p Cell Processing Steps

Surface cleaning
POCl₃ diffusion
Front and back oxide removal
Top surface metal evaporation (1700 Å Ti, 500 Å Pd, 23 kÅ Ag)
Lapping to remove back N+ layer
Photolithographic delineation of top metal
Back metallization (as front)
Contact sintering (550°C, H₂, 15 min.)
Mesa delineation using photolithography and HF:HNO₃: HAc etch

The finished cells were evaluated using a quartz halide source (91.6 w/cm²). In addition to I_{sc} and V_{oc} data for each cell, four sets of current-voltage values were taken for computerized curve fitting to determine values of fill factor. A summary of the results of this curve fitting and of the comparisons between the baseline and test lots is given in Table 3. An overview of the comparisons between lots is afforded by the line marked A giving the test lot (i.e. reagent grade POCl₃) parameters as a percentage of the base line lot (i.e. electronic grade POCl₃) values. No significant differences exist in terms of V_{oc} and I_{sc}. Values of fill factor and efficiency for the test lot are approximately 3% higher than in the base line case. From the point of view of the experiment this is not a significant change, indicating that there is no distinction between the two grades of POCl₃ used as the diffusant source.

Table 4 gives the metallic element analyses, as supplied by J. T. Baker, for the particular lots of POCl₃ used in the experiment. Of particular interest are the Ti, Cr, Mn and Fe levels. Introduction of these species at levels of about 0.1 ppm in Czochralski silicon during growth result in either minority carrier base lifetime reduction or recombination center density enhancement leading to severe reductions in

TABLE 3

Cell Performance Comparison.
 Electronic vs. Reagent Grade POCl₃ Diffusant Sources

71121 TEST OF REAGENT VS. ELECT. GRADE POCL3 MON. MAT.
 ARRAY AM1: PO=91.60MW/CM² NO AR COATING

ID	ISC	VOC	FF	FFF
1R*	22.50	.554	.713	9.40
1R	22.10	.573	.732	9.80
2P	22.60	.575	.733	10.07
3R	22.60	.575	.750	10.30
4R	22.60	.572	.707	9.67
5P	22.10	.571	.745	9.95
R1	22.40	.575	.767	10.44
R2	22.50	.576	.762	10.44
R3	22.40	.569	.728	9.81
R4	22.30	.571	.760	10.23

AVERAGES: 71121 BASELINE
 22.40 .573 .733 9.96
 STD .24 .002 .015 .22

71121 TEST OF REAGENT VS. ELECT. GRADE POCL3 MON. MAT.
 22.40 .573 .754 10.23
 STD .07 .003 .015 .26

PERCENT OF BASELINE
 A → 100.0 99.9 102.8 102.7
 STD% 1.4 .8 4.2 4.9

Table 4
Metallic Impurity Content (ppm) of J. T. Baker POCl₃,
Reagent vs. Electronic Grade

<u>Metallic Elements</u>	<u>Reagent Grade</u>	<u>Electronic Grade</u>
Ti	< 20 ppm	< 0.02 ppm
Cr	50	Not detectable
Mn	30	0.002
Fe	300	< 0.02
Mg	70	< 0.1
Zn	< 20	.02

solar cell efficiency (Fig. 1).⁽²⁾ Of this set of elements, introduction of all but Ti at levels below 0.005 ppm has no measurable effect. In the case of titanium, as little as ~ 0.001 ppm in the grown silicon crystal reduces cell efficiency by about 20% below that of an undoped control. Thus, the relatively high titanium content (~ 20 ppm) of the reagent grade POCl₃ does not produce any detectable efficiency reduction which occurs with as little as five parts per billion of Ti deliberately incorporated in silicon crystals during growth.

The lack of effect on cell performance of high concentrations of Ti, Mn, Cr and Fe in the POCl₃ source as compared with deliberate doping of the growing crystal with metallic impurities may reflect the fact that stable oxides and glasses are formed making these impurities not available for diffusion. Deliberate use of much higher concentrations of metallic impurities in the POCl₃ source could be useful in determining if a threshold concentration exists.

3.2.2 Back Junction Formation

On the program, consideration will be given to forming the back p+/p junction by using a boron-doped oxide prepared by chemical vapor deposition. Good control of the uniformity and reproducibility of such a diffusant source is expected. For an effective back surface field region, good control of the doping profile is important. The CVD approach is

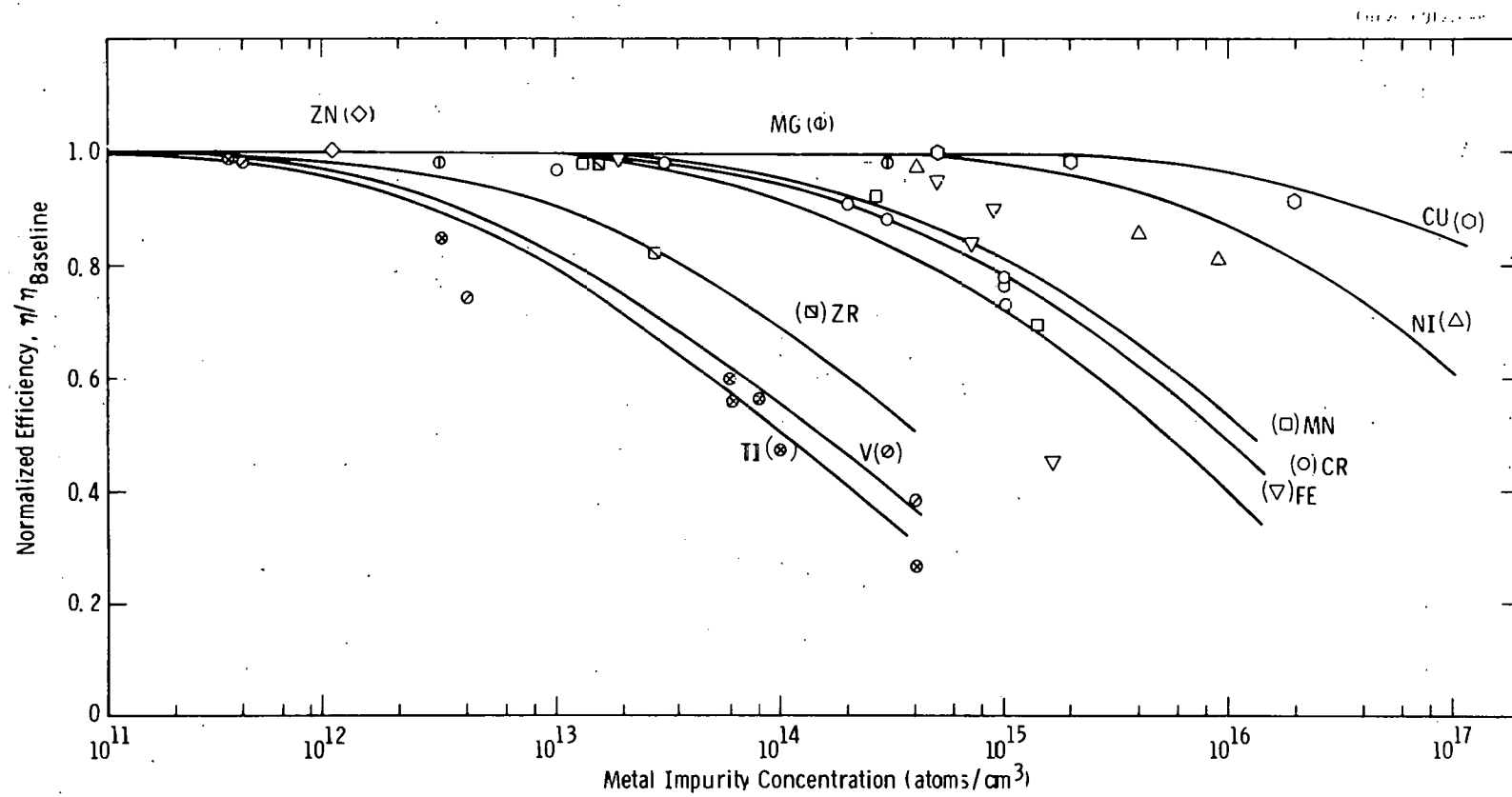


Fig. 1 Normalized solar cell efficiency as a function of substrate metal impurity concentration. From R. H. Hopkins et al. Ref. 2.

particularly attractive in the use of low temperatures to prepare the doped oxide. Work during this quarter has been aimed at calibrating the deposition and annealing parameters which relate to the formation of the doped oxide and of the diffusion into the substrate prior to formation of the front junction.

Table 5 gives a summary of the parameters which have been examined empirically. Results have been obtained in terms of the properties of the boron-doped layer (such as sheet resistance, depth of penetration, etc.) which will be used for selecting optimum conditions for cell fabrication. The results of the calibration experiments will also permit later assessment of the sensitivity of the back junction characteristics to the preparation parameters.

3.3 AR Coating

In studies made before this contract effort, workers at Westinghouse have demonstrated that films prepared from liquid organometallic precursors can be used as very effective AR coatings on solar cells produced using Czochralski silicon wafers. The composition of the precursors can be formulated to yield simple oxides such as SiO_2 , TiO_2 or Ta_2O_5 or mixtures of oxides with tailored optical properties. In the case of TiO_2 , clear films have been produced with index of refraction of about 2.4. The technique has been used to produce multi-layer coatings as well. For the work to date, the thickness of the films has been controlled by adjusting viscosity of the precursor and by spinning the substrates, analogously to photoresist practice in the IC industry. Processing of continuous lengths of dendritic web silicon will require development of dip or spray application methods.

In initial work on this program, cells were spin-coated using liquid organometallic precursors of TiO_2 and SiO_2 . Ranges of values for coating viscosity and for spin-speed were used in these preliminary experiments. After coating, the samples were baked at 400°C in vacuum. The primary aim of this work was to determine the practical limits to short circuit current enhancement in state-of-the-art web silicon cells coated in this manner.

Table 5

Boron Doped-Oxide BSF Calibration Experiments

<u>Objective</u>	<u>Variables</u>	<u>Range of Variables</u>	<u>Related Variables</u>
A. Uniformity of Deposition (in horizontal r.f. system)	1. Reactor Geometry		
	(i) Inlet nozzle to susceptor separation	8 to 18 inches	A.1 (iii), (iv) A.2 (i), (ii) B.1 (i)
	(ii) Temp. uniformity across deposition zone	$\pm 3^\circ$ to $\pm 10^\circ\text{C}$	A.1 (iii), (iv) A.2 (i), (iii)
	(iii) Susceptor tilt angle	$2\frac{1}{2}^\circ$ to 15°	A.1 (i), (ii), (iv) A.2 (i), (ii), (iii)
	(iv) Total gas flow rate	13.75 ℓ/m to 26.75 ℓ/m	A.1 (i), (ii), (iii) A.2 (i), (ii), (iii)
	(v) Nozzle (concentric) connection to inlet	Permutation and combination of N_2 , O_2 , SiH_4 and B_2H_6 intels	A.1 (i), (iii), (iv) A.2 (i), (ii)
	2. CVD Variables		
	(i) Deposition temperature	350° to 520°C	A.1 (ii), (iii), (iv), (v) A.2 (ii), (iii) B.1 (i)
	(ii) Oxygen, SiH_4 and B_2H_6 concentrations	4.7 to 9.1% O_2 0.09 to 0.18% SiH_4 9×10^{-3} to 3.6×10^{-2} B_2H_6	A.1 (i), (ii), (iii), (iv) A.2 (i), (iii)
	(iii) $\text{B}_2\text{H}_6/\text{SiH}_4$ ratio effect on deposition rate	$1.2 \times 5X$	A.2 (i), (ii)

Table 5 (Cont'd.)

<u>Objective</u>	<u>Variables</u>	<u>Range of Variables</u>	<u>Related Variables</u>
B. Optimum Doped Oxide	1. Composition of Doped Oxide		
	(i) B_2H_6/SiH_4 ratio for appropriate R_s	0.1 to 0.4	A.2 (i), (ii)
	(ii) Doped or undoped (cap) oxide thickness ratio (to inhibit transport to active surface)	1.0:0.0, 0.4:0.6 and 0.4:0.2 (μm)	---
	(iii) Total deposited oxide thickness required for BSF, $POCl_3$ mask, & subsequent front surface etch	1.0 to 0.6 μ	---
	2. Doped Oxide Annealing		
	(i) Ambient composition (and total flow rate)	10 to 50% O_2 in N_2 (1 - 5 l/m) ²	A.2 (i), (ii) B.1 (i) B.2 (ii), (iii)
	(ii) Temperature	900 - 1100°C	A.2 (i), (ii) B.1 (i), (ii) B.2 (iii)
	(iii) Time	1/3 - 4 hrs.	B.1 (i), (ii) B.2 (i), (ii)

Table 6 gives values for I_{SC} , fill factor and efficiency of these cells before and after coating. The ratio is given to show improvement after coating. The first three cells in the table were fabricated on Czochralski crystals while the last seven were on dendritic web silicon. All but one of the samples were from the same diffusion run.

The data for sample 1 show the effect of a single layer of TiO_2 ($n = 2.4$); sample 2 a double layer of SiO_2 ($n = 1.4$) over TiO_2 . The remainder of the samples were double coated under various experimental conditions. For the web cells a maximum improvement of 43% in efficiency was noted. The significance of these initial experiments is the demonstration that 13% efficient web silicon cells can be fabricated using the organometallic derived AR coatings.

3.4 Cell Separation

The ribbon form of dendritic web silicon allows, in principle, continuous processing of the material through most of the cell fabrication process. Removal of the dendritic edges and transverse separation of cells from the ribbon is required. The former is a step unique in the use of this material. Edge removal and cell separation should involve little waste of material, and resulting in rectangular cells for a module with high packing factor. Diamond scribing could be used as it was in Westinghouse work on dendritic web silicon cells for space arrays in the 1960's. However, laser scribing is more attractive in not requiring mechanical support. Scribing speed, effects on device performance, yield and cost of the two approaches must be evaluated.

The feasibility of laser scribing as a technique for cell separation and delineation was tested on samples of dendritic web material, and on solar cells prepared from Czochralski (CZ) material and solar cells prepared from web material. The tests were made using a KORAD KRT laser with 5000 W peak power at the Westinghouse Advanced Technology Laboratories in Baltimore. The repetition rate was 1000 Hz with a spot diameter of about 15 μm . At a travel rate of about 4 cm/sec, each pass penetrated the silicon by about 50-100 μm .

Table 6

Effectiveness of AR Coatings Prepared from Organometallic Precursors

<u>SAMPLE</u>	<u>I_{SC} (mA)</u>		<u>FF</u>			<u>EFFICIENCY (%)</u>		<u>POST PRE</u>	
	<u>PRE</u>	<u>POST</u>	<u>POST PRE</u>	<u>PRE</u>	<u>POST</u>	<u>POST PRE</u>	<u>PRE</u>		<u>POST</u>
1 (single)	22.8	29.5	1.29	.77	.73	1.00	10.4	13.9	1.34
2 (double)	22.0	30.5	1.39	.73	.77	1.05	9.4	14.0	1.49
3	20.8	28.9	1.39	.73	.77	1.05	8.7	12.8	1.47
4	20.1	27.9	1.39	.74	.76	1.03	8.5	11.8	1.39
5	19.2	24.9	1.30	.71	.70	.99	7.6	9.5	1.25
6	21.1	29.4	1.39	.71	.72	1.01	8.6	12.2	1.42
7	21.6	31.0	1.44	.75	.73	.97	9.4	13.3	1.41
8	21.4	30.5	1.43	.74	.74	1.00	9.0	12.9	1.43
9	21.9	29.6	1.35	.76	.73	.96	9.5	12.4	1.31
10	21.1	29.5	1.40	.75	.73	.97	9.0	12.4	1.38

The first test was to determine if laser scribing, followed by breaking, could be used to remove the dendrites from the web. Samples of dendritic web (about 160 μm thick) both annealed and unannealed were scribed with no breakage or shattering noted. A normal vacuum hold down was used. Tests were made with one and two passes of the laser. The dendrites could be broken off after a single pass, more force and greater care were required than in the case when two passes were used. The second pass was needed because of the slightly thicker web material near the dendrites. A single pass across the width of the web was sufficient for separation in that direction.

In addition to these tests, a number of solar cell structures on CZ and web silicon substrates were subjected to top surface and back surface laser scribing and then separated by breaking. The cells had n+/p front junctions only and were in the following state of completion: (1) mesa etched and AR coated; (2) mesa etched, not AR coated; (3) not mesa etched, not AR coated; (4) mesa etched, photoresist coated and (5) mesa etched, AR coated and photoresist coated. The photoresist coating was considered to permit etching of the silicon after scribing. In all cases the back surface was metallized with either evaporated aluminum or evaporated layers of titanium, palladium and silver.

In the cases for which the cell structures had been mesa etched, the laser scribing was done inside the mesa. With the non-mesa etched samples, a cell approximately 1 cm^2 in area was scribed.

It was noted that the presence or absence of various coatings (AR or PR) or metallization had no physical or electrical effect on the scribing process, and in all cases the cells readily fractured after a single pass with the laser at full power.

The samples were measured after laser scribing and fracturing, that is, no post-scribing treatment was used. Figures 2 and 3 show the efficiency and fill factor of selected samples before scribing (\cdot), after scribing on back surface and fracturing (\square) and after scribing on the front surface and fracturing (\odot). For cells which had not been etched

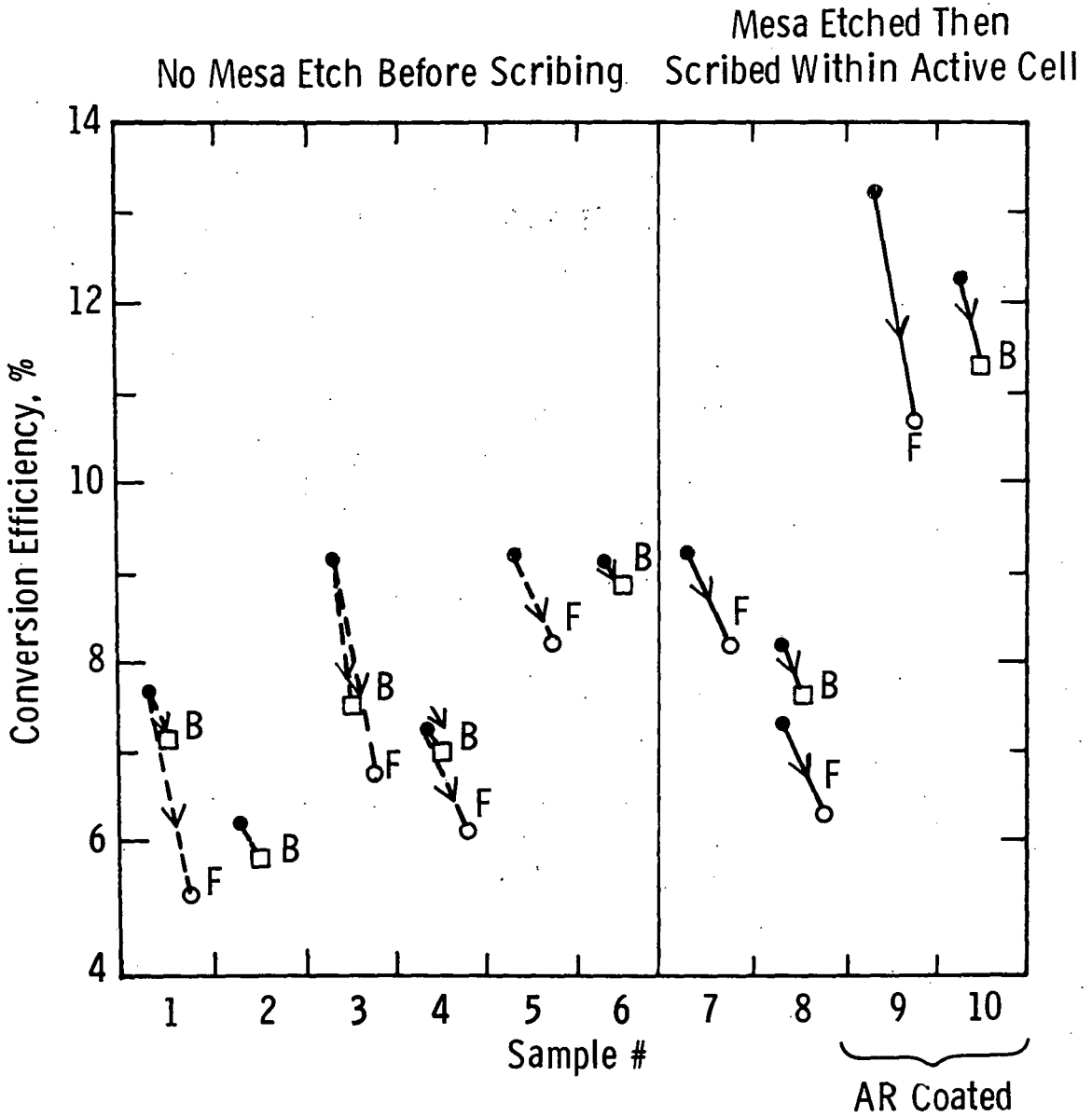


Figure 2

Effects of front and back surface laser scribing on the conversion efficiency of selected cells in Czochralski material.

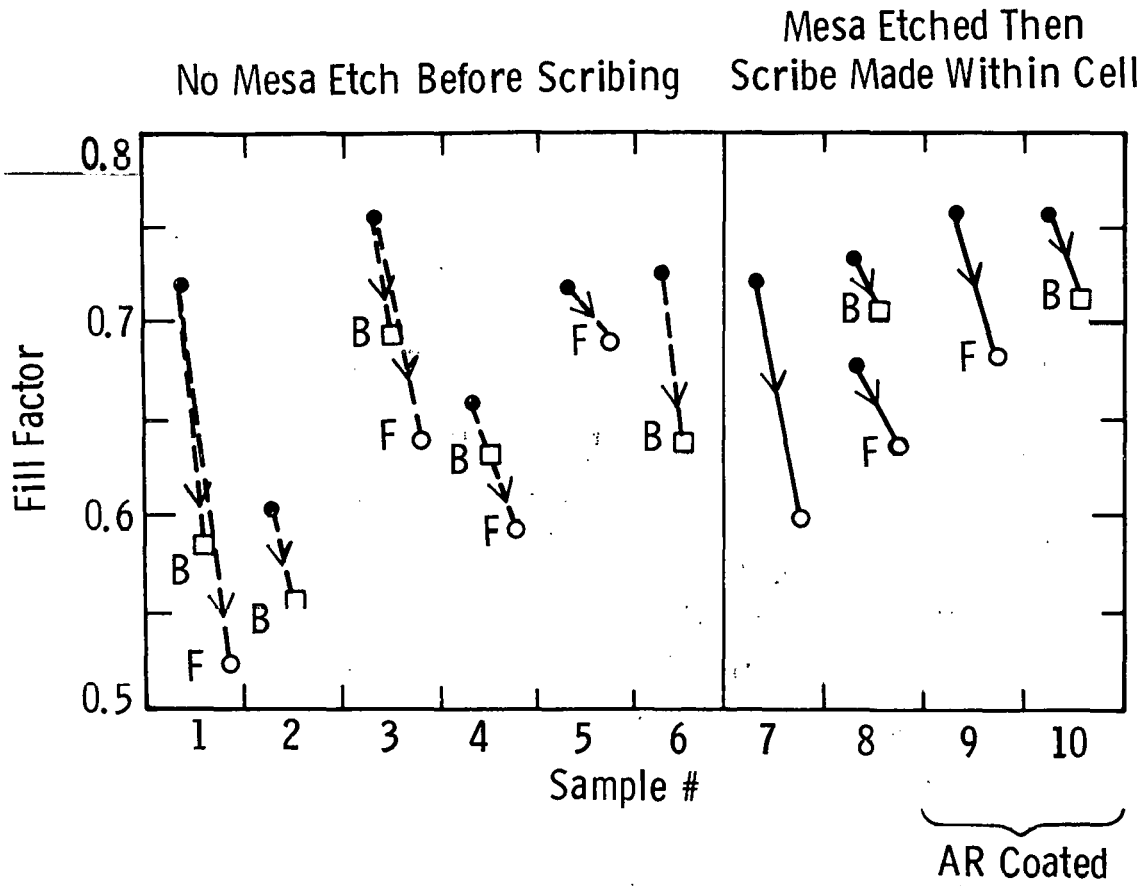


Figure 3

Effects of front and back surface laser scribing on the fill factor values of selected cells in Czochralski material.

before scribing (Samples 1 through 6 in), the initial values (.) in each case were determined by using the average for similar etched cells of the same diffusion run.

Although the data is scattered, it shows that back surface scribing is less damaging to the cell than is front surface scribing. Fractional change in efficiency (η) is

$$\Delta\eta/\eta(\text{FF}) = (\eta_f - \eta_i)/\eta_i$$

with i and f indicating initial and final values. The fill factor is treated similarly.

The factor Δ was calculated for the efficiency and fill factor of each sample and the results averaged. Table 7 shows the summary.

Table 7

Mean of Fractional Changes in Fill Factor and Efficiency Resulting from Laser Scribing

<u>Parameter</u>	<u>Scribing Condition</u>	<u>Average Fractional Change</u>
Fill factor	front scribed	-0.125
Fill factor	back scribed	-0.074
Efficiency	front scribed	-0.161
Efficiency	back scribed	-0.098

Detailed IV measurements on a number of these samples showed that changes in fill factor (and efficiency) were due to junction degradation after scribing and fracturing with increased forward currents at low voltage. This effect was most noticeable in the front scribed cells.

All data given in Figs. 2 and 3 and in Table 7 were obtained from laser scribed samples which had not been processed after scribing, that is they were not cleaned or etched.

A number of the back scribed cells were examined using optical and scanning electron microscopy. Figure 4 is a scanning electron micrograph showing a typical region on a back surface scribed cell. The laser scribe, spikes penetrate (on the average) about 40% of the cell thickness with some spikes penetrating up to 75% of the cell thickness. This type of penetration should not damage the junction (which is about 0.5 μm from the top surface). Figure 5, however, shows the probable cause of the degradation. Depicted is a region where the laser dwelled for a short period of time. Here the spikes penetrated completely through the crystal. When these regions were removed by extensive chemical etching of the silicon, the scribed cell regained its pre-scribed parameters.

The results shown in Figs. 4 and 5 explain why the damage on the front scribed cells is greater than on the back scribed cells. With front scribing, the entire periphery of the junction is disturbed. Increased junction leakage or actual shunt current flow paths can occur along the entire perimeter. With back scribing, a much smaller length of junction perimeter is damaged with consequential smaller effect.

The solution to this problem requires reduction of laser power and elimination of retrace or dwell during the process. This should result in scribed cells which show no degradation in cell properties after scribing.

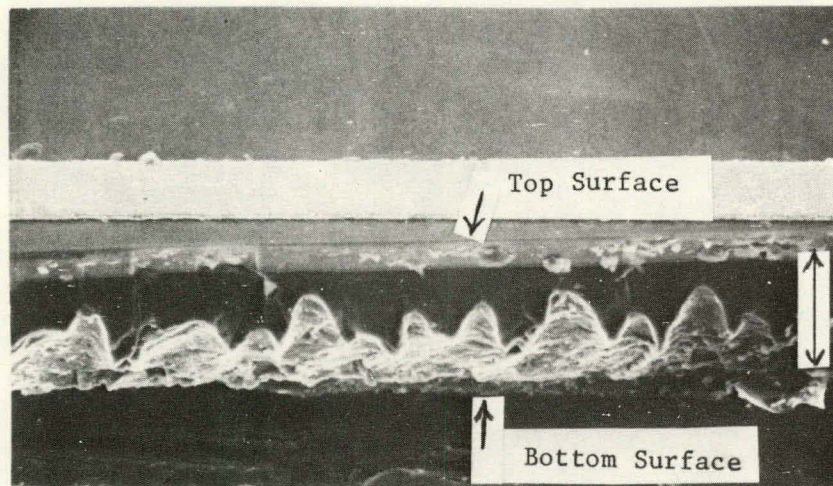


Fig. 4 2009-6LS Laser scribed from back
 -- Note metallization line; and
 penetration depth of scribe -
 Length of scale bar: 100 μm .

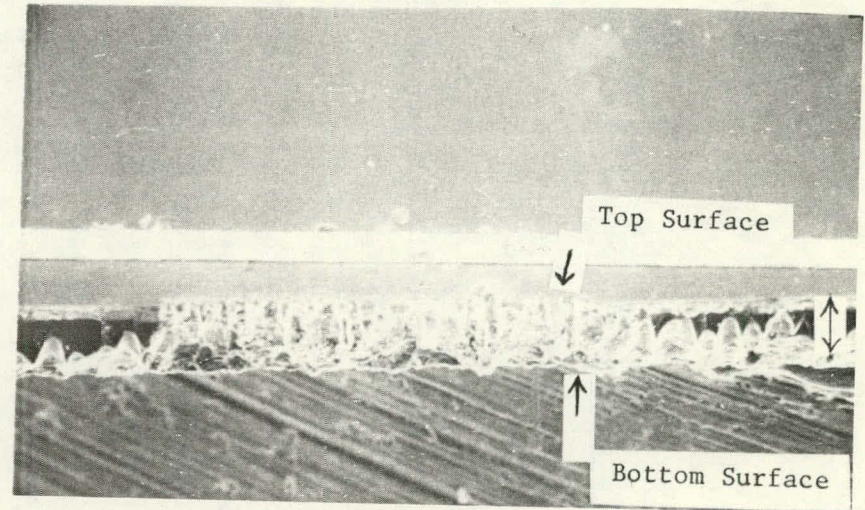


Fig. 5 2009-6LS Laser scribed from back
 -- Note total penetration after
 laser scribe dwell. Length of
 scale bar: 100 μm .

4. CONCLUSIONS

The proposed process sequence for the fabrication of solar cell modules from dendritic web silicon with an overall yield of 85% has been analyzed in terms of silicon sheet, direct materials and utilities costs. Using the JPL IPEG approach, a module selling price of \$0.46/watt on 1975 dollars is estimated in association with these direct costs. Of the material costs, that for the encapsulation is dominant. If that is excluded, then the proposed process sequence would give solar modules selling at a price of about \$0.32/watt (1975) to account for silicon, direct materials and utilities. Thus, \$0.18/watt of the selling price could be associated with the equipment, building and labor costs and allow the price goal to be achieved.

These figures will be used for guidance of more detailed future assessments of the proposed process sequence.

Cell performance is not detectably degraded by the use of cheaper, reagent grade POCl_3 for front junction formation instead of the electronic grade chemical. Although concentrations of Ti in the range of 0.0001 ppm to 0.01 ppm, deliberately incorporated into Si during growth, produce efficiency degradation ranging from 20 to 80%, no detectable degradation was observed for a Ti concentration of about 20 ppm in the POCl_3 reagent grade diffusant source. Similarly, Fe in the POCl_3 at 300 ppm and Cr at 50 ppm and Mn at 30 ppm) had no detectable effect, whereas at the 0.02 ppm impurity level in silicon significant degradation of efficiency has been reported for these species.

Double layer AR coatings can be prepared on dendritic web silicon cells from liquid organometallic precursors to produce values of conversion efficiency of 13%. Baking of the coatings at 400°C presents no problems.

Laser scribing and fracture can be used to remove dendrites from web material without breaking or shattering. Back surface laser scribing of cells is readily accomplished through the normal back surface metallization layer. Back surface laser scribing as performed during this period produces an average fractional reduction in efficiency of about 0.10 (and in fill factor of about 0.07) in comparison to 0.16 (and 0.13) for front surface scribing. Laser degradation of cell performance is associated with damage at the front junction. Such damage has been produced inadvertently in localized areas during back surface scribing. Etch-removal of the laser affected portion of the front junction restored pre-scribing cell performance.

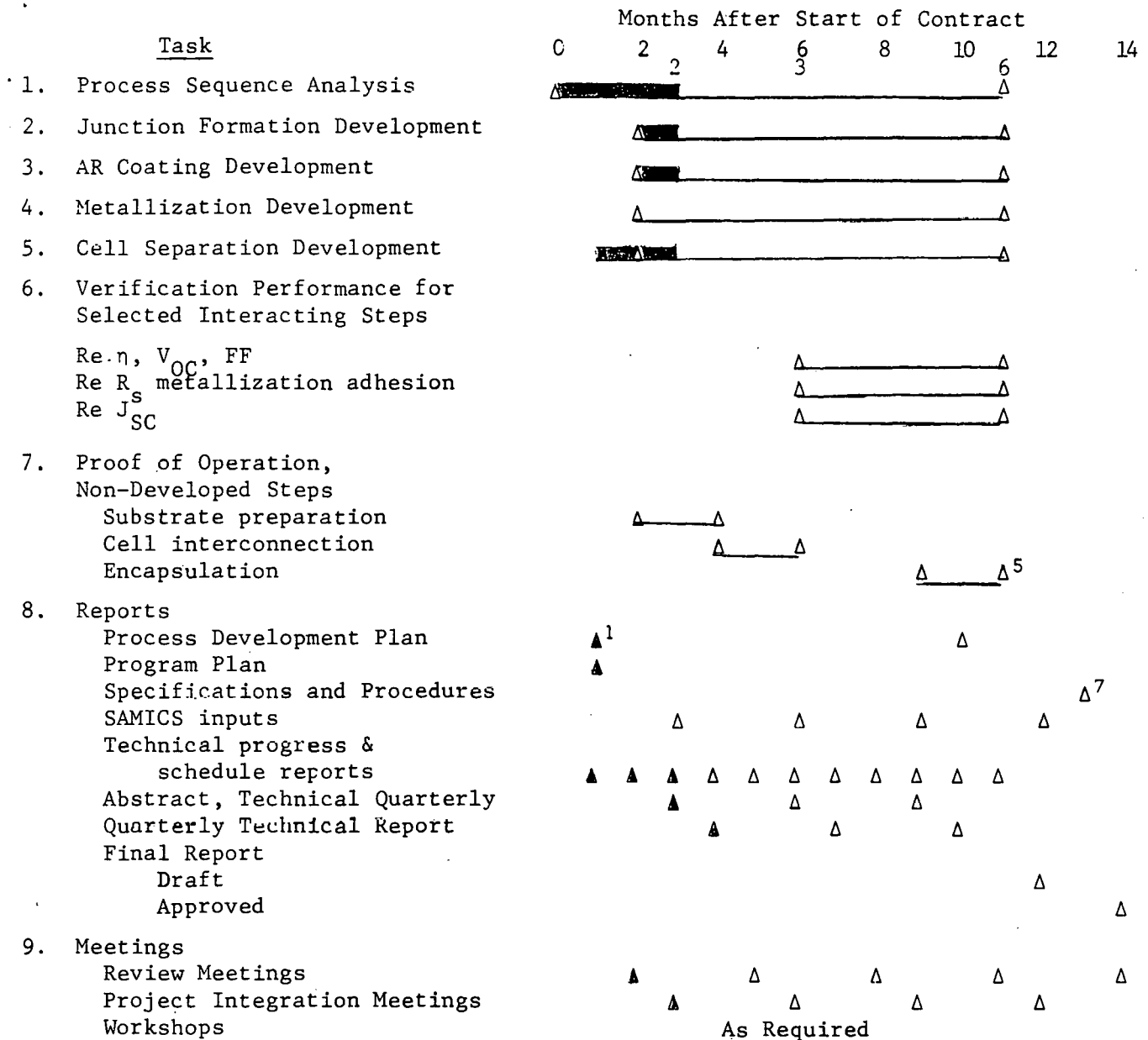
5. PROGRAM STATUS

5.1 Present Status

As shown in Fig. 6, the work on this program is generally on schedule. Metallization development (Task 4) has not begun as planned. The proposed metallization method requires a photoresist rejection technique for removing the thin evaporated Ti-Pd layer except in the area of the gridded front electrode. This technique has not been established yet. Work on substrate preparation, as a part of Task 7, has been delayed, pending the availability of required information from a concurrent program, JPL Contract No. 954654. SAMICS Format A descriptions of the steps involved in the proposed process sequence have been prepared. These are being checked for accuracy before submission.

5.2 Future Work

Experiments on junction formation using POCl_3 deliberately doped with high concentrations of Ti will be performed to establish if the reagent grade chemical can be used without sacrificing cell performance. Work will be done on p+ back surface field regions prepared from CVD doped oxide sources. AR coating effort will focus on the acceptability of dip application of the liquid organometallic precursor for TiO_2 . In addition, the etchability of the AR coating will be investigated to permit grid electroding after AR coating. Laser scribing experiments will be conducted with close control of the laser penetration from the back surface. This will be done to determine if damage to the front junction can be avoided during scribing, thus preventing degradation of cell performance.



Milestones:

1. Approved Development Plan.
2. Preliminary Technical and Economic Evaluation Completed
3. Revised Process Sequence Established.
4. Process Verifications Completed.
5. Proof of Operation Completed.
6. Final Process Plans Established.
7. Material, Supply and Process Specifications and Process Procedures Delivered.

Figure 6
Approximate Task Schedule and Milestone Chart

6. REFERENCES

1. Interim Price Estimation Guidelines: A Precursor and an Adjunct to SAMIS III, Version One. JPL Document No. 5101-33, September 10, 1977.
2. R. H. Hopkins, et al., Seventh Quarterly Report Silicon Materials Task of the Low Cost Solar Array Project (Phase II). ERDA/JPL-954431-77/3.

7. ACKNOWLEDGEMENTS

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