Report on Application Specific Integrated Circuits
for Relativistic Heavy Ion Detectors

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ASIC Engineering Considerations

Detector systems for RHIC experiments are invariably going to be large and complex. Thus it behooves the planners to incorporate elements that have little need for adjustment, calibration and correction to the produced data. For example, if power, size and cost considerations permit, time can be digitized directly (i.e. with counters, shift registers, etc.) where no adjustments, calibrations or corrections are required. The circuit either works correctly or not at all. This kind of circuit behavior is extremely valuable in dectectors with 10^5 or more channel elements. In analog to digital conversion applications, direct conversion (i.e. flash ADC) may be prohibitive in cost, size and power. Here major effort must be given to minimize the magnitude of offset and conversion gain variance. Where possible self correction and adjustment should be applied at the subsystem level.

ASIC Engineering Problems

Their are many levels of involvement in the development and production of ASIC's. The simplest level is to specify device properties, locate vendors capable of meeting these specifications, select the vendor, usually after a bidding process, and verify that proto-type and production devices meet these specifications. These minimal requirements might include logic simulation of digital devices or spice type simulation of analog circuits. A minimum organization to successfully carry out such an ASIC project would include a project manager, preferably with ASIC experiemce but at least having a broad knowledge of available technologies. The organization should include one or more people of logic or analog design simulation experience. It should include people capable of developing test facilities. This is a major effort. For example, gate array ASIC's are generally tested by the manufacturer for logic functions but usually require the user to perform his own detailed testing because of the unique speed or function demands of ASIC's in this field. This is a substantial hardware and software effort. Ordinary gate arrays can often be tested

with commercial pattern generators and logic analyzers but invariably interfaces must be constructed, control devices designed and constructed to do parameter or margin tests etc. Even a simple gate array or memory device will require large combinational test sequences that can only reasonably be practical under software control and analysis.

In this simple example of ASIC development for which detailed silicon or gallium arsinide design is left to an outside vendor, a short list of personnel and equipment might read as follows:

Personnel: Project Leader (experienced)

Logic design and simulator (digital)

Analog design and simulator (analog)

Test system designer for hardware implementation

Test system designer for software implementation

Equipment: Computer and software for simulations & test management

Pattern Generator

Logic Analyzers – Digital and Analog

Application Specific Interface and Controller

Ordinary lab equipment (i.e. scope, meters, power supplies, etc.)

This list is suitable for the simplest of ASIC development and would only apply where the appropriate Cell libraries are available to the vendor. If circuit elements not available from Cell libraries are required a new level of complexity is encountered. This may involve in house chip layout and spice type simulations even for digital circuits. In this case the above list quickly expands to include silicon level design and layout capability with a perhaps extended learning curve plus chip level probe and test facilities probably including a clean room.

The MPS II drift chambers shift register project is illustrative of the process of ASIC development. This device is a 1024 bit 4 channel shift register capable of running at greater than 330 Mhz while dissipating 200 mw. The project was funded in 1978. The first step was to canvas the industry. Some 30 companies were visited and in most cases high level

technical discussions were held. Only three of these vendors were convincing as to their capabilities to meet the requirements. Two of them responded to the RFQ. The contract was awarded to RCA. Their design was an advanced CMOS-SOS process in which all logic Cells had to be designed and simulated since no circuits in their Cell libraries could approach the speed requirement. The output circuit led to a patent. Many months of design reviews were held before a prototype run was attempted. In fact, the first three prototypes runs failed for a variety of reasons.

Early on in the project (before the contract was awarded) it was clear BNL had to take responsibility for all testing, even at the wafer level since the speed of this ASIC was more that an order of magnitude beyond RCA's in house test capability. This effort alone accounted for more that a man year of engineering and developement. The tester had to measure time to 100 ps, operate the chip from DC to 330 Mhz and exercise parameters for margin tests. All of this under software control and in a fraction of a second. The instrument was designed to test chips at the wafer level or as packaged parts.

After prototype runs yielded successful parts on the pilot line, the processing was moved into production facilities. Wafers were produced and returned to the pilot line for testing. Yields varied greatly. At one point 60 wafers were damaged beyond repair because of misaligned fingers on the probe card. The vendor should have found this problem before destroying $10,000 worth of wafers. They didn't until the BNL group convinced them of their faulty probe card. This is an example of how closely an ASIC development group must follow the manufacturing process to maintain cost control. Device yields varied greatly, in part because this ASIC was an advanced state-of-the-art technology and the vendor had a poor understanding of the effect of production parameter variations on device performance. This is a situation that is likely to prevail anytime ASIC properties deviate from those of normal production devices. Chip development this far from the mainstream of production chips can only elicit cost plus fixed fee agreements or foundry only vendor responsibility. For the shift register, the final cost was three times the "budgetary" figures initially given. The time from contract signing to delivery of 20,000 working channels was about 36 months.

An ASIC project to develop analog memories has some features simular to the shift register ASIC. Some elements of the design such as amplifiers, memory Cells and switches are not available from Cell libraries. Thus design and simulation of these elements are required either within the project group or as part of a vendor contract. The accuracy, stability and reproducibility characteristics of this ASIC will require clever ideas in circuit design and extensive test and evaluation capability first at the prototype level where design changes are still possible and later during production where less flexibility is required but speed and efficiency become important. Since the Analog memory specification has not yet been set it is possible only to create a "typical" set of test requirements of things to be measured:

1. Transfer gain and linearity
2. Offset and stability
3. Rise and fall response times
4. Memory decay time
5. Noise
6. Dynamic range
7. Cross talk
8. Clock to data acquisition timing
9. Sensitivity to supply voltages
10. Sensitivity to temperature
11. _____

This review of problems encountered in ASIC design and production may seem somewhat daunting but suggests such projects require careful personnel and equipment planning. In particular some of the design tools may require extensive training and practice along the learning curve.