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New Main Ring Control System*

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NEW MAIN RING CONTROL SYSTEM

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The Fermilab Main Ring control system has been operational for over sixteen years. Aging and obsolescence of the equipment make the maintenance difficult. Since the advent of the Tevatron, considerable upgrades have been made to the controls of all the Fermilab accelerators except the Main Ring. Modernization of the equipment and standardization of the hardware and software have thus become inevitable. The Tevatron CAMAC serial system has been chosen as a basic foundation in order to make the Main Ring control system compatible with the rest of the accelerator complex. New hardware pieces including intelligent CAMAC modules have been designed to satisfy unique requirements. Fiber optic cable and repeaters have been installed in order to accommodate new channel requirements onto the already saturated communication medium system.

* Operated by Universities Research Association Inc., under contract with the US Department of Energy.

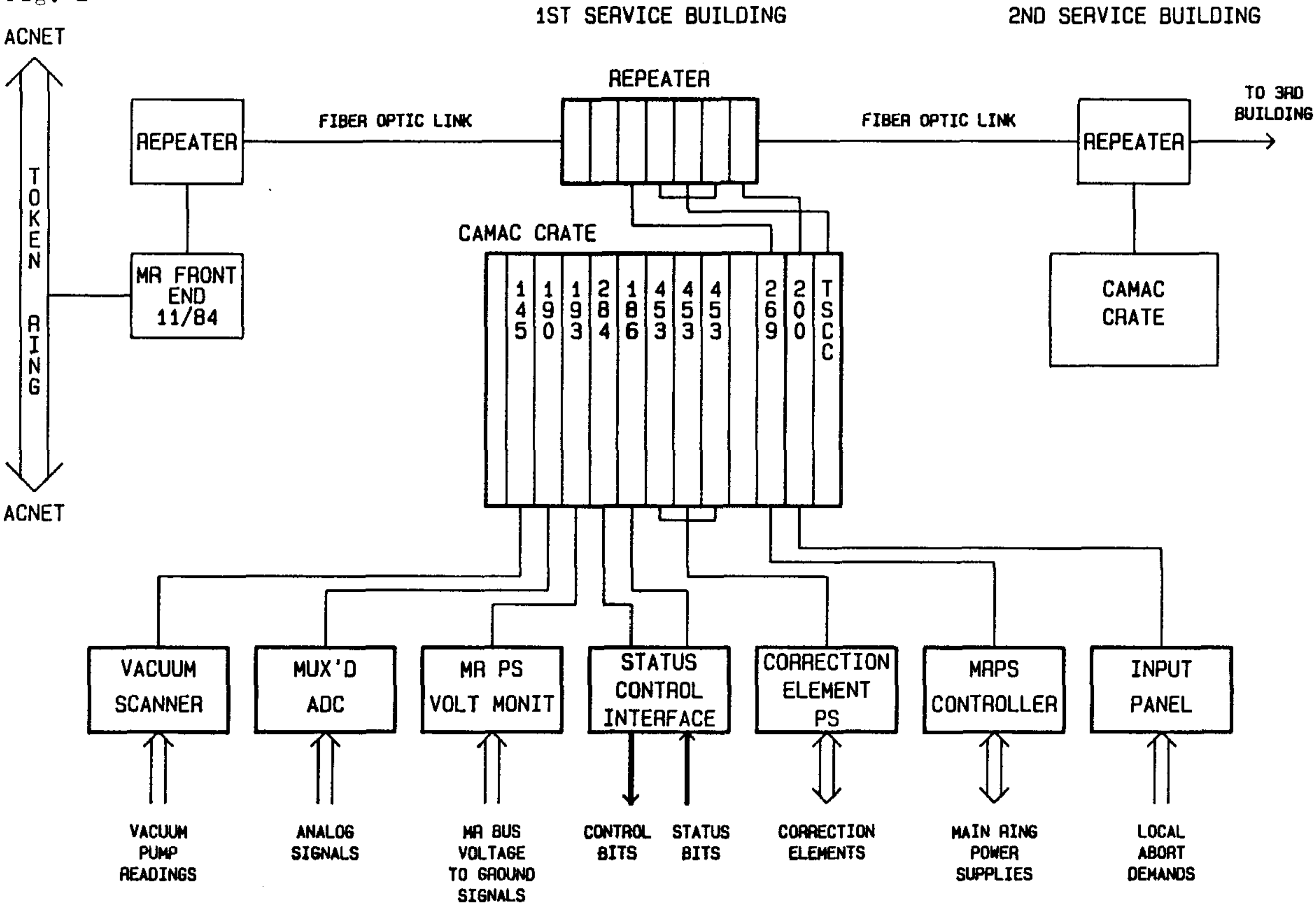
1. Introduction

The first generation Fermilab Main Ring Control System was installed in the early 1970s. The equipment has aged, and obsolescence of some of the spare parts has made maintenance work difficult. Since the advent of the Tevatron, considerable upgrades have been made to the controls of all the accelerators except the Main Ring (Although some improvements have been made to the Main Ring by adding necessary modules to the Tevatron.). Modernization of the equipment and standardization of the hardware and software have thus become inevitable. The CAMAC serial system, which had been used for the Tevatron, has been chosen as a basic foundation in order to make the Main Ring control system compatible with the rest of the accelerator complex.

The Main Ring control system upgrade work started in the early part of 1988. Some CAMAC modules, which had been developed for the Tevatron, have been constructed, and cables have been assembled. New modules and chassis have been developed and constructed.

A five month shutdown started at the end of June, 1989. Removal of old equipment and cables has been done first. Equipment rack and cable tray installations have followed. Now at the end of October, 1989, major cables have been pulled, and a majority of hardware pieces have been installed. Some software pieces have been written, and testing of different subsystems is beginning. By the early part of December, 1989, the entire accelerator including the Main Ring is expected to be operational and accelerating beams.

Fig. 1


1ST SERVICE BUILDING
2ND SERVICE BUILDING
ACNET
TOKEN RING
ACNET
REPEATER
MR FRONT END 11/84
FIBER OPTIC LINK
REPEATER
FIBER OPTIC LINK
REPEATER
TO 3RD BUILDING
CAMAC CRATE
145
190
193
284
186
453
453
453
269
200
TSCC
CAMAC CRATE
VACUUM SCANNER
MUX'D ADC
MR PS VOLT MONIT
STATUS CONTROL INTERFACE
CORRECTION ELEMENT PS
MRPS CONTROLLER
INPUT PANEL
VACUUM PUMP READINGS
ANALOG SIGNALS
MR BUS VOLTAGE TO GROUND SIGNALS
CONTROL BITS
STATUS BITS
CORRECTION ELEMENTS
MAIN RING POWER SUPPLIES
LOCAL ABORT DEMANDS

As to newly designed hardware, CAMAC 193 Eight Channel Transient Recorder module has been developed to record and analyze voltage to ground signals on the main busses when a ramp trip occurs. A description of the 193 module is given in Section 2.1. CAMAC 453 Quad Waveform Generator module has been developed to control twelve dipole conrrection element power supplies per building. The module is flexible and capable of generating waveforms for series of cycles with different energy levels and updating waveforms at a rate of 720 Hz. A description of the 453 module is given in Section 2.3. Other newly developed hardware pieces are CAMAC 145 Vacuum Readback Interface module and SCI (Status Control Interface) chassis, whose descriptions are given in Sections 2.2 and 2.4 respectively. Brief descriptions of other support systems (i.e., Fiber Optic Link, Main Ring Power Supply Link and Main Ring Abort System) are also given in Sections 3.1 thru 3.3.

The Main Ring control system including the front end computer and the fiber optic link is shown in Fig. 1.

2. New Developments

2.1 The Eight Channel Transient Recorder - CAMAC 193

The Main Ring has four magnet busses (i.e., bend lower, bend upper, quad focus and quad defocus). Each of these busses has a number of magnets and a number of power supplies connected in series. Voltages measured on these busses in reference to the ground are monitored so that they can be properly operated and maintained.

The CAMAC 193 module monitors the magnet bus voltages in three different modes (i.e., single channel read, snapshot and transient record). In the single channel read mode, the host computer can read the time-stamp and the ADC data on a specified channel at its leisure.

In the snapshot mode, the host specifies an arm event and a delay value. The 193 module collects data for all the eight channels after the specified delay from the arm event. For example, if the operator needs to look at the bus voltages in all the service buildings around the ring 2 milliseconds after the "Main Ring Beam Sample" time, he specifies a delay value of 2 and a clock event code of $2C. All the 193 modules that are distributed around the ring collect data for eight channels at the specified time. The operator can then read and plot the data on a graphic display. The graphic plot of the data enables him to examine voltage distributions on the magnet busses, which allow him to locate faulty power supplies or ground faults on the busses.

In the transient record mode, the host specifies an arm event and a number of sample triggers. The 193 module continuously collects and stores data in a circular memory buffer (2K bytes per channel) for eight channels, and it stops the data collection the specified number of sample triggers after the arm event. For example, if the operator needs to know what happens to the bus voltages before and after the "Ramp Fast Trip" event, he specifies a clock event of $23 and a delay value of 1000. All the 193 modules around the ring stop the data collection 1000 sample triggers after the trip event has occurred. The operator can later read and plot the data.

He can plot a set of data for one point in time. As he does the same thing for different points in time before and after the trip event, he can tell what has chronologically happened to the bus voltages.

The 193 module consists of two pc boards with a common front panel. The Board-C is a computer/ CAMAC interface board which contains an Z8002, RAM, PROM, clock event sources, interrupt controllers, a multichannel timer and a CAMAC interface. The Board-P is a peripheral board which consists of an ADC subsystem and a time-stamp counter.

The main characteristics of the CAMAC 193 module are as follows.

Board-C

(1) CPU: Zilog Z8002 clocked at 6 MHz.

(2) Memory: 44K bytes of RAM, 16K bytes of PROM.

(3) TCLK event sources: One for time-stamp reset and seven for general use.

(4) External inputs: Four arm and trigger signals.

(5) CAMAC interface: F & A to vector conversion is done in single PROM.

Board-P

(1) ADC: 10 μs conversion per channel, 12-bit resolution, selectable up to 8 differential channels, -10.24 to +10.235V voltage range.

(2) Time-stamp counter: 16-bit counter, clock rate selectable for 100 KHz, 10 KHz, 1 KHz or 100 Hz.

K. Seino designed the hardware and J. Smedinghoff wrote the firmware for the 193 module [1].

2.2 The Vacuum Readback Interface - CAMAC 145

A question was raised whether the Main Ring vacuum control subsystem should have been changed to what the Tevatron had. However, it was decided not to make extensive modifications on the entire subsystem but to make some improvements on the vacuum readback. In the Main Ring vacuum control subsystem, vacuum control operations are still performed via separate hardware pieces which consist of digital input and output modules and an SCI (Status and Control Interface, which is described in Section 2.4) unit.

The CAMAC 145 module was designed with the Motorola MC68000 microprocessor and the MC68881 floating-point corprocessor. The serial vacuum data which come from a vacuum scanner unit are first converted to parallel data. The serial to parallel conversion and its supporting circuits were implemented in the Altera EPM5128 erasable PLD. A special BCD data format of the vacuum scanner is then converted to the IEEE standard floating-point format.

The module calculates an average reading from up to sixty-three channels of vacuum data approximately once a minute, excluding bad readings. It also generates alarms when the average vacuum value is out of limits or when fifteen or more pumps are returning bad readings.

Distributed intelligence (i.e., floating-point conversion, averaging and alarm scanning) had not been available on the old Main Ring control system. These improvements will reduce computational burdens on the host computer, and the standard data format will allow Main Ring vacuum devices to be placed on "Parameter Pages" and "Datalogger Lists".

K. Seino designed the hardware and B. Hendricks wrote the firmware for the 145 module [2].

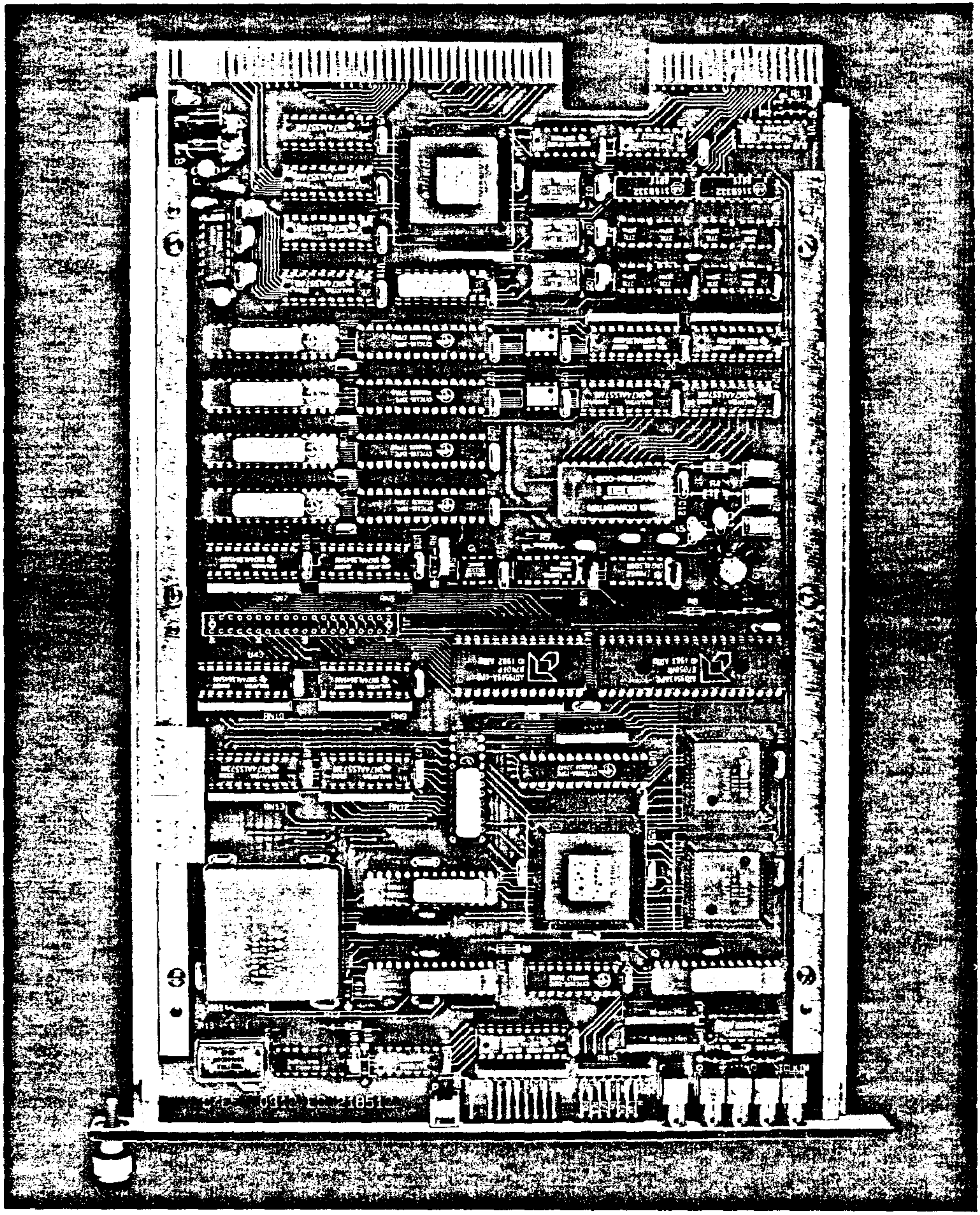
2.3 The Quad Waveform Generator/ Power Supply Controller - CAMAC 453

The accelerator is presently operated in series of cycles, each of which may deal with a different energy level and serve a different purpose (e.g., proton acceleration, antiproton acceleration, bunch coalescing, studies, etc. -----). In order to meet new requirements, a series of waveform generators has been developed, starting from simple modules (160, 165 and 265), through a moderately complicated one (365), to a complicated but flexible one (465).

The CAMAC 465 module is a single wide module, which controls one power supply. The analog output from the module is updated at a rate of 10 KHz.

The CAMAC 453 module is a double wide module, which is capable of generating semi-independent analog outputs at a rate of 720 Hz and performing digital controls for up to four dipole correction element power supplies. The 453 module consists of "A-Board" and "B-Board". The A-Board is essentially the 465 module with minor modifications. The B-Board encompasses a quad DAC, analog monitoring circuits and additional digital input/ output controls.

The 465 module (or the A-Board) is a densely populated board as shown in Fig. 2. In order to accommodate many functional blocks (some of them are of high speed) in a limited space, the board was designed with the latest components available at the time. Some of these components were Intel 80960KA CPU, Fujitsu MB81C78A RAMs, Cypress CY7C251 PROMs, Altera EPM5032s and EPM5128s.



The main characteristics of the CAMAC 453 module are as follows.

Output Function

(1) Output waveforms:

output = sf1*m1*f(t) + sf2*m2*g(M1) + sf3*m3*h(M2)

where sf1, sf2 and sf3 are constant scale factors having a range of -128.0 to +127.9,

m1, m2 and m3 are raw MDAT (a link distributing accelerator parameters in real time) readings divided by 256,

f(t) is an interpolated function of time which is initiated by the "OR" of up to 8 TCLK (Tevatron clock) events,

g(M1) and h(M2) are interpolated function of selected MDAT parameters.

(2) Tables: Each term in the output functions will have eight possible tables with a maximum of 32 entries each. Table selection is effected by an interrupt. Sixteen interrupt levels are available, each being asserted by the "OR" of up to 8 TCLK events. Upon assertion of an interrupt, the module begins using three user specified tables (one for each term in the output function) for each of the four output waveforms.

A-Board

(1) CPU: Intel 80960KA (32 bit) clocked at 20 MHz.

(2) Memory: 32K (or 128K) bytes of RAM, 64K bytes of PROM.

(3) TCLK decode/ interrupt: 16 levels, "OR" of up to 8 TCLK events each.

(4) MDAT interface: Decodes and stores up to 16 parameters.

(5) CAMAC interface: CPU reads F & A combination and validates it against vector table.

(6) Digital inputs: 16 optically coupled status bits.

(7) Digital outputs: 3 sets of relay contacts, 4 bits of TTL signal.

B-Board

(1) Analog outputs: 4 buffered outputs from Analog Devices AD664 DAC (4 channels, 12 bits).

(2) Analog monitoring: 4 analog outputs are multiplexed, converted back to digital and latched for reading from CAMAC and A-Board, total update rate is 25 KHz for 4 channels.

(3) Digital inputs: 16 optically coupled status bits.

(4) Digital outputs: 4 bits of TTL signal.

(5) CAMAC interface: F & A combinations are decoded with EPLD.

A. Franck and J. Gomilar designed the hardware, and B. Hendricks wrote the firmware for the 453 module [3].

2.4 Status Control Interface - The SCI Unit

In order to control and monitor the Main Ring magnet busses and power supplies and other support systems (i.e., the vacuum, cooling and safety systems), a large number of digital input and output bits have to be read and set.

L. Anderson designed a chassis called "SCI", which is interfaced to the CAMAC system via two CAMAC modules 186 and 284. The 186 module provides up to 256 bits of digital input with an external multiplexing chassis. A multiplexer card residing in the SCI unit decodes four address lines, which originate at the 186 module, to select one of sixteen digital input channels at a time. The 186 module also provides twelve pulsed control bits, whcih are distributed to proper external devices via the SCI unit. The 284 module provides sixteen additional pulsed control bits, which are fed to a relay box via the SCI unit. Relay contacts are used to turn on/ off pumps and valves for the vacuum system and to turn on/ off pumps for the water cooling system.

The SCI unit is made of an 7" x 19" Euro-crate, Euro type 3U plug-in cards and a plug-in power supply module. The unit also has a local channel select/ monitor facility for digital inputs. The main characteristics of the SCI unit are as follows.

Digital Input:

(1) Data bits are updated every 160 microseconds.

(2) 13 channels (16 bits per channel), TTL compatible, terminated to ground with 1000 ohm resistor

(3) 3 channels (16 bits per channel), optically coupled, for AC controllers (controllers for 13KVAC vacuum breaker)

Digital Output:

(1) 3 sets (3 bits per set), TTL compatible, pulsed high for 10 microseconds, for AC controllers

(2) 16 bits of relay contacts, pulsed for 0.75 seconds

3. Other Support Systems

3.1 Fiber Optic Link

A bundle of ninteen Heliax cables had been installed around the Main Ring for the Tevatron. However, because of ever increasing demands for communication media, all the cables in the bundle had been used at some parts of the ring. In order to overcome shortage of communication media and to meet future expansions, a fiber optic trunk cable containing twenty-four fibers has been installed.

Fiber optic repeaters have been designed, built and installed for use with above mentioned optic fibers for the Main Ring CAMAC serial system, the Main Ring power supply link and the Main Ring abort system.

R. Ducar designed the fiber optic repeaters, and the fiber optic link was installed under his supervision [4].

3.2 Main Ring Power Supply Control System (or Link)

The Main Ring Power Supply System consists of a number of power supplies powering three separate magnet busses; bend, quad focussing and quad defocussing. The power supplies are located in 15 of 24 service buildings distributed around the ring. During typical operations, the current ramps from 100 amps to 1700 amps with a cycle time of 10 seconds.

The control system for the Main Ring power supplies consists of two DEC PDP 11/55 minicomputers, a link transmitter and CAMAC 269 link receiver modules. The link transmitter was designed by R. Mahler, and it is capable of generating 10 Mbs data frames and sending ramp data to all the power supplies at a 720 Hz rate. The CAMAC 269 module was designed by R. Ducar, and it receives ramp data and passes it on to the power supplies [5], [6].

The new system has advantages over the old system. First, it allows communication with all of the power supplies at a 720 Hz rate, because of the faster serial data rate. Second, it allows diagnostics of the link, which were not previously provided. Third, its communication protocol and link transmitter resemble some of the Tevatron links, which made the hardware implementation easier.

3.3 Main Ring Abort Loop

The Main Ring Abort Loop consists of a CAMAC 201 Source module, a repeater/ link system and CAMAC 200 Abort Concentrator modules.

The active signal of the abort loop is a 5 MHz square wave, being originated by the 201 module at the Service Building C0, which is transmitted clockwise around the ring via the fiber optic repeater/ link system. The presence of the active signal on the abort loop, as received by a 200 module at C0, is interpreted as "Beam Permit". The cessation of the signal, as detected at C0, is interpreted as "Abort". When this condition occurs, a CAMAC 279 Beam Sync Clock Interface/ Timer module generates a trigger to abort the Main Ring beam in synchronization with the revolving beam. The 200 modules are located in each of the 30 service buildings around the ring. They receive the upstream status of the link and provide a local peremit to allow the 5 MHz signal to pass downstream.

CAMAC modules 200, 201 and 279 had been designed by R. Ducar for Tevatron applications [7], [8].

Acknowledgments

We wish to express our appreciation to our manager, P. Lucas, for his guidance and support. We also wish to thank R. Crouch, T. Gierhart, R. Hagler, T. Hendricks, D. Jarvis, R. Klecka and R. Koldenhoven for their hard work in constructing and installing the hardware pieces.

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Figure Captions

Fig. 1. The new Fermilab Main Ring Control System including the front end computer and the fiber optic link.

Fig. 2. The A-Board of the CAMAC 453 Quad Waveform Generator module.