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Design of an Advanced Readout Chip for Silicon Strip Detectors

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Abstract

Work was begun in 1990 on the development of an advanced readout chip (ARC) for silicon strip detectors. Features of the proposed device include compatibility with close bunch spacing and double sided detectors, and on chip analog storage, digitization, and data sparsification. Chips have been designed to check all of these concepts, fabricated in the VTI 2 micron process, and tested. The circuit configurations and test results are presented in this paper.

I. INTRODUCTION

The requirements of future experiments at Fermilab have created a need for a silicon strip readout chip which can acquire signals at beam interaction times of as fast as 132 ns. A time delay is required to form a trigger, necessitating the use of an analog pipeline to store the signals temporarily. In order to minimize signal processing downstream and maximize readout speed, it is highly desirable to do A/D conversion on the chip. A switched capacitor front end and A/D has been designed at Fermilab which accomplishes these goals.

II. CIRCUIT DESIGN AND OPERATION

The following important design criteria were adopted for development of the ARC:

1). Signal acquisition is stopped during digitization and readout, to reduce input coupling problems.
2). The front end is completely reset every beam crossing to avoid potential pileup problems which can occur with RC or continuous reset schemes.
3). The risetime is digitally adjustable to accommodate different interaction times, as well as to compensate for the effects of variable input capacitance and process variations on the risetime.
4). A common digitally set threshold is used for data sparsification of all channels, requiring close attention to compensation of offsets and charge injection.
5). Gain is incorporated into the analog storage stage to eliminate the need for an intermediate gain stage, simplifying device operation.
6). For simplicity and low power dissipation, each channel uses a Wilkinson type A/D with a common counter and ramp.

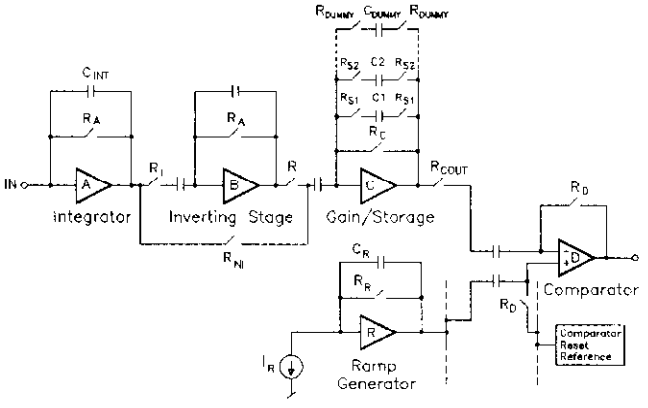

Fig. 1 . Front end configuration for one channel

Figure 1 is a block diagram of the resultant design, from the integrator through the comparator (which is part of the Wilkinson A/D).

A. Integrator

Since the input integrator is loaded with detector capacitance, it is difficult to reset quickly. This leads to a design which has an integrator with a "slow" switched reset and limited gain (and thus large dynamic range), capacitively coupled to a fast amplifier. The bandwidth of the system is limited in the integrator, so that the per bucket fast reset can be accomplished in the amplifier, which is the gain/storage stage in Figure 1. The amplifier then effectively performs a double correlated sample on the integrator output. The integrator must be periodically reset to avoid eventual saturation, and this can be accomplished by performing a slow reset during beam gap intervals and during readout.

The integrator is essentially a double cascode configuration with a large PMOS input transistor operating near weak inversion. Since a relatively large current (200 ua) must be set through the input transistor to acheive low noise, the integrator power dissipation represents a substantial portion of the total. Therefore, a reduced power supply (2.7V) is used here to minimize dissipation. Running the input transistor source at a reduced voltage has the added benefit of back biasing the bulk to source junction, which reduces the noise contribution of the back gate transconductance and the bulk resistance (a noise improvement of approximately 15% was measured). The DC reset voltage of the integrator output is adjustable, so the dynamic range can be optimized for either

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polarity input signal. The risetime of the integrator can be adjusted by switching one or more different valued capacitors onto the dominant node.

B. Inverting Stage

In order to maximize the available range and simplifiy and optimize the design of the stages following the integrator, a unipolar design philosophy is followed. That is, a negative going integrator output is assumed. In order to accept either polarity input signal, an inverting stage (gain=-1) which can be placed in series with the integrator output is required. This is a very simple inverting amplifier with the gain set by feedback capacitor ratio. Inserting the inverting stage in the circuit path results in minimal delay increase and risetime degradation.

C. Gain/Storage

The functions of gain and analog storage can actually be combined into one stage where the feedback capacitor that sets the gain also functions as the storage element (assuming acquisition and readout are not desired simultaneously). The single stage configuration has several advantages over an approach with separate gain and storage stages: 1) a single stage is simpler and takes less area and power, 2) fewer switches are required, and 3) the same switches are used for both acquisition and readout, resulting in good charge injection cancellation. The main disadvantage of this approach is that storage capacitor mismatches result in cell to cell gain variations. However, this is acceptable if the capacitor matching error is less than the A/D resolution.

This stage is implemented as a simple double cascode amplifier, which is necessary to obtain sufficient open loop gain to maintain accuracy. The fast reset required in this stage can be most easily and effectively implemented by a simple FET switch between input and output nodes. However, this results in the amplifier output being reset to one end of its range. This is not a problem given that a unipolar design approach is followed. Opening the reset switch causes charge injection into the input of the amplifier. In order to preserve the maximum possible time for signal integration, the reset switch charge injection is simply allowed to add to the incoming signal (which is timed to occur immediately after reset release). The resultant sum is then stored. The charge injection can then be easily subtracted out later during readout.

D. Comparator

When a pipeline readout and digitization is desired, a storage capacitor voltage is compared to a ramp voltage by a high gain comparator block. The time that is required for the comparator to trip is then proportional to the storage capacitor voltage. This design features an AC coupled comparator so that offsets may be nulled. It is typical to provide some sort of external reference which effectively sets the ramp starting voltage and assures that even for zero signal, the ramp must slew for some distance before tripping the comparator. However, the configuration shown in Figure 1 requires no external reference. An internal reset reference simply sets the DC reset point of the comparator inputs to one end of the range (since operation is unipolar), and there is no offset between the ramp starting point and zero signal. Thus for proper operation, some small signal input is necessary to ensure that the comparator starts out in the proper state. This required signal is typically less than any sparsification threshold that would be set, so this is deemed acceptable. An alternative would be to simply inject a small offset voltage on the ramp before starting, ensuring digitization of the signal all the way down to zero.

E. Ramp Generator and A/D Converter

The ramp voltage generator driving the A/D comparator is implemented as one circuit which is capable of driving all channels in parallel. This eliminates any channel to channel offset which would be caused by individual ramp generators. The design of this block is simplified by the fact that only one polarity ramp is needed. The feedback capacitor which sets the ramp rate is made to be of the same type as the integrator feedback capacitor. This provides a very desirable first order insensitivity to system gain variations due to chip to chip integrator capacitor value variations.

A block diagram of the multi-channel A/D scheme is shown in Figure 2. An external clock is gated to an eight bit Gray code counter when the ramp is started. Each channel has a latch which stores the state of the counter when the comparator is tripped. To set a threshold, a negative number is loaded into the counter (MSB=1). Any channel which latches a positive count (MSB=0) is then over threshold and should be read out. Since the MSB is used as a flag, the A/D has effectively seven bits of resolution. The MSB flags from all channels feed a channel prioritizer, which controls the sequential digital readout of the data and address of all channels over threshold.

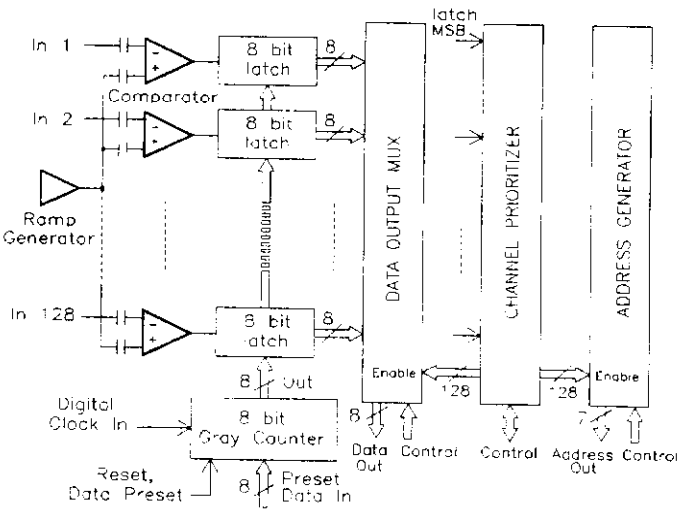

Fig. 2 . A/D and readout configuration

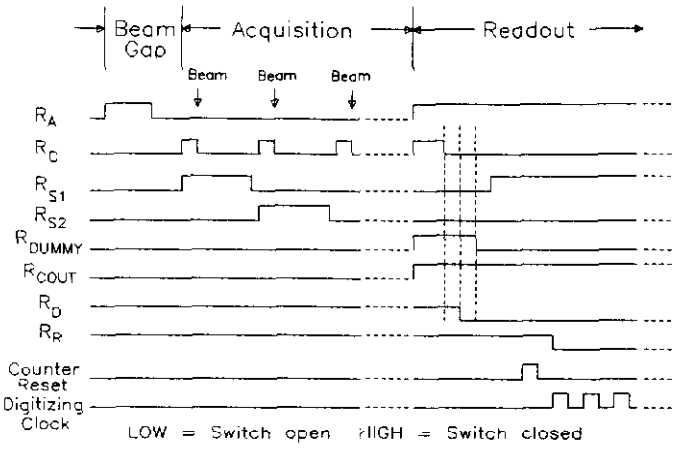

Fig. 3 . Timing diagram

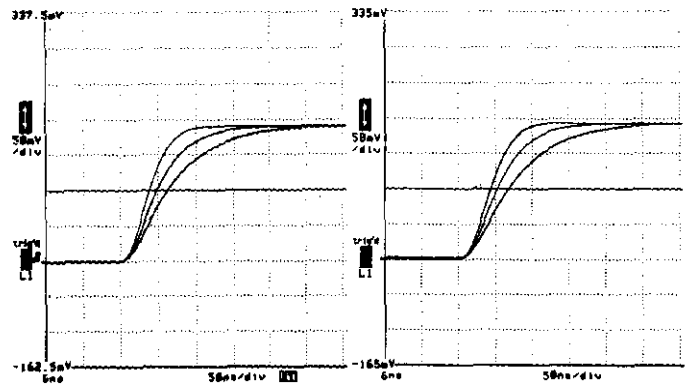

Fig. 4 . Measured system risetime

F. Clocking scheme

Figure 3 is a timing diagram of the proposed clocking scheme. Note that only the gain/storage reset (RC) is operated every interaction. Sampling the signal on a storage capacitor occurs just before the next reset (RS1, RS2, ...). The acquisition control signals can be derived from a single master clock. To initiate pipeline readout, an extra dummy storage capacitor is needed to reproduce the charge injection effect of opening the storage reset switch. The comparator reset (RD) is released with this charge injection effect present at the storage output, which will effectively cause it to be subtracted out when reading any other storage capacitor voltage. The dummy capacitor is then removed, and the capacitor of interest is placed in the storage feedback to read out the desired signal voltage. After the A/D counter is reset, the ramp and clock are started. This clocking pattern theoretically subtracts out all offsets and charge injection effects.

III. TEST RESULTS

To date, numerous test chips of all sections have been designed and produced using the VTI 2 micron process.

Two front end test chips were produced which essentially contain the circuitry up through the storage stage. (Only two storage capacitors were used here for simplicity). The first chip actually contains a fast resetable amplifier between the integrator and storage to raise the gain, and the second chip contains only integrator and storage, as in Figure 1. Figure 4 is a hardcopy of the measured risetime of the system (measured at the storage output of the first chip) for two different values of input capacitance. For each case, the risetime has been digitally programmed to three different values that would be approximately appropriate for interaction times of 132 ns, 200 ns, and 400 ns. This shows that risetime is easily optimized for a variety of conditions. The noise was measured to be approximately 600 electrons + 50 e/pf for the 200 ns case, and 700 + 50 e/pf for the 132 ns case.

Measurements on the second test chip show the speed to be slightly slower than on the first chip, and the noise to be somewhat higher at approximately 600 electrons + 60 e/pf (200 ns case). The performance difference in the two chips is not due to any configuration difference, and seems to indicate run to run differences in performance of the same integrator.

The power dissipation of the integrator and gain/storage is about 1.0 mw.

An A/D test chip was designed which consisted of eight identical channels, spaced with a 45 micron pitch. Each channnel consisted of a four element storage stage (three active elements plus a dummy) followed by an A/D. Sparsification and readout circuitry served all channels. Testing was performed by injecting different signal amplitudes into one channel at a time, or combinations of channels. Setting a threshold by preloading the Gray counter with a negative number gave the desired result of reading out only those channels above the threshold. When running the digitizing clock at 40 MHz (and toggling the Gray counter on both edges of the clock), digitization of a full scale signal is completed in 1.6 us.

The test results show that the scheme employed is indeed effective in reducing offsets. The effective offset variation was measured to be 1 mv rms. This includes element to element storage offset in addition to channel to channel comparator offset variations. Gain mismatch, due to capacitor ratio errors, was found to be less than 1%. Since poly-metal1-metal2 capactors were used, this is as expected. The linearity error of the A/D over the full range was less than 0.5%. The quiescent power dissipation of the comparator (relevant for acquisition mode) is about 0.3 mw.

IV. CONCLUSIONS

A multi-channel silicon strip readout chip has been designed with a fast, programmable risetime integrator, an analog pipeline, and A/D conversion with sparsification. Test chips have been produced which verify all of these concepts. Measurements are very encouraging and show that performance is close to desired. Conversion to a 1.2 micron process and complete integration is planned for the near future.