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Voltage-Clearance Recommendations for Printed Boards

IPC (Institute for Interconnecting and Packaging Electronic Circuits) Task Group on Electrical Clearance

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INTRODUCTION

Present and future trends in printed board designs point to higher circuit densities with narrower lines and closer spacings. Some designers are now laying out boards with 0.13 mm (0.005 inch)* lines and spacings. The reduction of nominal spacing between conductive elements has raised questions concerning the adequacy of present voltage-clearance recommendations in IPC and other guidance documents. The present recommendations are considered too conservative in that they are weighted with large safety factors, especially for small clearances, and are frequently disregarded by many designers as, for example, the requirement of 0.38 (0.015) minimum clearance between uncoated conductors for voltage differences of 0 to 50 volts. Published voltage breakdown measurements made on printed boards with comb patterns with their enhanced conductor test lengths show breakdowns occurring at much higher voltages than those specified for the clearances in existing documents.[1-6]

A Task Group was set up by the IPC to review published breakdown measurements and to make any additional measurements necessary to provide voltage-clearance recommendations which can be used for the revision of IPC documents and for those documents generated by IPC members for use in their own organizations. This report presents the recommendations of this group.

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*Dimensions are in millimeters with inches in parentheses.

The International Electrotechnical Commission (IEC) through Subcommittee 28A (Insulation Coordination for Low-Voltage Equipment) has proposed a draft for clearances and creepage distances for low-voltage equipment. This proposal, which gives clearances for different voltage levels, is based on an extensive joint study by Lehner, Safran, Schau, and Weise[1] of voltage breakdown and conductor spacing and on the experience gained on apparatus built to their recommendations which has been used in German postal equipment for over 5 years. This usage has included outdoor closed housings as well as clean dry rooms.

The recommendations of their study, which are based on some 250,000 measurements in different environments and degrees of pollution, were incorporated in a proposal to change VDE 0110.[7] Included in these measurements are those with partial discharge voltages, surge voltages, continuous voltages, and mixed dc and ac voltages in atmospheres with varying levels of temperature, humidity, and dust.

Recommendations from the Lehner, Safran, Schau, and Weise study and supporting data from this Task Group and from other studies provide the basis for recommended minimum clearances for different voltage levels between conductive elements on a printed board. A summarization of pertinent data is presented to permit designers to assess the risk involved in deviating from recommended clearances for different

board end-use environments. These recommended clearance values incorporate safety factors from the measured data. A designer should not design to a failure condition.

The Task Group recognized at the outset that with limited testing facilities, manpower, and test boards available, a comprehensive study of voltage breakdown in different environments could not be undertaken. In view of the data already published covering typical use environments, a decision was made to test only at a worst case environment, evaluating both coated and uncoated boards. In other more benign environments, voltage breakdown levels are expected to be equal to or greater than those in this environment, and clearance recommendations based on this environment will have general applicability for almost all IPC user environments. For open marine environments where salt may deposit on equipment, special protection may be required.

The worst case environment selected was 75°C, 95 to 100 percent relative humidity, and a pressure of 0.385×10^5 Pascals (289 Torr) which is equivalent to roughly 7600 meters (25,000 feet) altitude. A preconditioning treatment prior to measurement consisted of 1 week at 75°C, and 95 to 100 percent RH. The environmental pressure or altitude was limited by the experimental difficulties of maintaining 75°C and 95 to 100 percent RH. Breakdown at other altitudes can be estimated through the use of the Paschen Curve.[8]

Experimental Measurements

The test pattern used is shown in Figure 1. The B01 or backside is similar to the A01 or front side which is shown. The comb patterns are based on the IPC B-25 design, that is, 0.17 (.0065), 0.32 (0.0125), and 0.64 (0.025) lines and spaces. Leads to the connector tabs were arranged to minimize breakdowns in the connectors. Equivalent lengths of conductor separations tested for each comb section are 280 to 300 (11 to 12) in the 0.17 section, 150 to 180 (6 to 7) in the 0.32 section, and about 80 (3) in the 0.64 section.

Forty boards of this test pattern were fabricated for the Task Group by Rockwell-Collins using photo tools generated at Sandia National Laboratories Albuquerque (SNLA). Copper was pattern plated in a pyrophosphate bath to 0.04 (0.0014) thickness on a thin clad, 1/3 oz. copper, FR 4, 1.5 (0.06) thick laminate. A tin-lead coating was plated on the copper and later reflowed using infrared fusing.

Of the 40 boards tested, 20 were uncoated or bare and 20 had a 0.05 ± 0.03 (0.002 ± 0.001) thick Conothane-type 1155 urethane coating. The test pattern permits 48 tests per board, four comb patterns for each of the three nominal separations or clearances, and four tests per comb. Thus a total of 20 x 48 or 960 tests could be run on bare or uncoated boards and a similar number on coated boards.

The original plan was for four testers to test ten boards each, five coated and five uncoated. Because of unforeseen difficulties, one of the testers was unable to carry out the testing, and that group of boards was tested at SNLA several months after the testing of an initial set. Another tester was Delsen Laboratories in Glendale, California. Data was not received from one of the testers, although it was said to correspond to that obtained from the other tests.

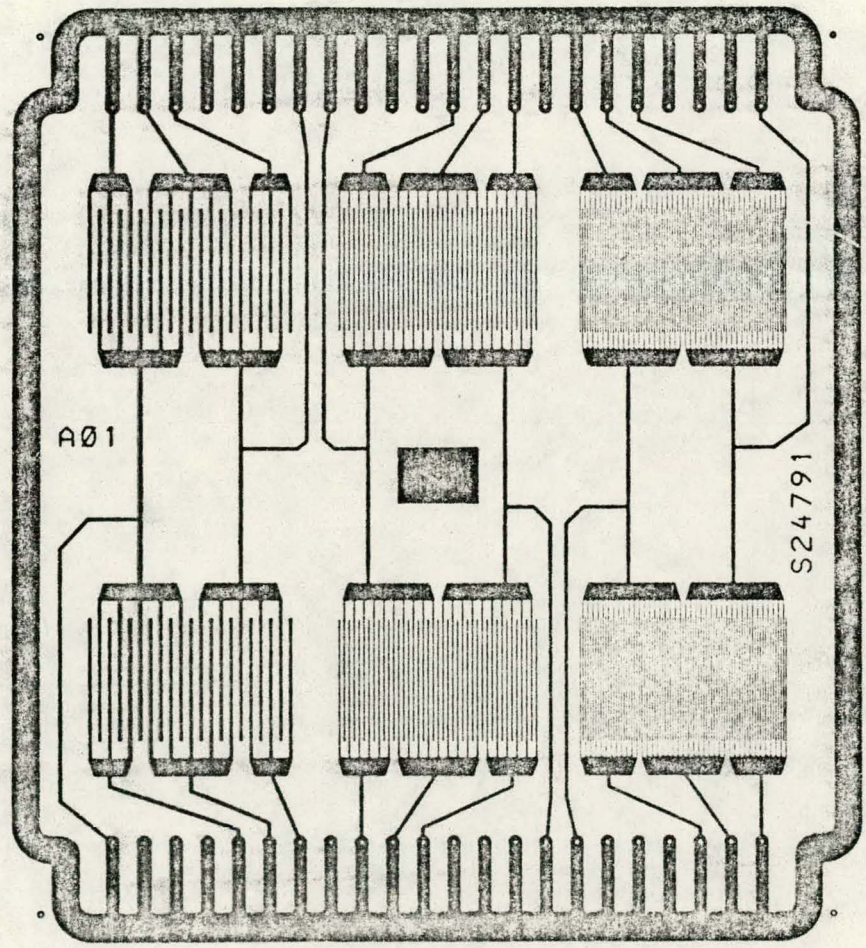

Figure 1. Test Pattern

All boards were examined for visual defects and electrically for shorts upon receipt at SNLA. Very few comb sections were eliminated from testing because of defects. All boards were cleaned using a deionized water boil, 1,1,1, trichloroethane vapor degrease, a deionized water rinse, and an isopropyl alcohol rinse, followed by an oven drying at 75°C for 1 hour. The urethane coating was applied by dipping and draining, then oven curing at 75°C for 8 hours.

A solvent extract resistivity test performed by Naval Avionics Center, Indianapolis, per MIL-P-28809 on a bare board, showed resistivity of the wash extract to be 24.5 M Ω-cm using a test water of 30 M Ω-cm. This can be compared to the MIL-P-55110C specification requirement of 2 M Ω-cm. Another board tested on an Omega II instrument showed a similar cleanliness level.

Testing at SNLA consisted of applying a dc voltage at 250 volts per second until breakdown occurred, producing a current of 4 or more mA which triggered cut-off of a Hypotronics Model 830-20 M 1 high-voltage power supply. Overhead fluorescent light provided some uv illumination to the test pattern. Breakdown location was observed through a window in the test chamber. Conductor separation was measured optically at or near the breakdown location. Tests performed at Delsen Testing Laboratories were at 250 $\pm$ 50 volts dc/sec on a Hypotronics Model HD-125. Cut-off was triggered at about 5 mA.

Results

Voltage breakdown values for the measured conductor separations are shown in Figure 2 along with least squares average, 99 and 99.9 percent (95 percent confidence) curves. Similar breakdown information is shown for coated boards in Figure 3. Breakdown ranges for bare and coated boards for the three nominal separations are shown in Table 1.

The scatter in breakdown voltages is much higher for coated than bare boards. Tests at SNLA were limited to 5 kV, and many of the values in the 1 to 5 kV range represent breakdowns in other than the comb pattern under test. Most, but significantly not all of the breakdowns on coated boards were higher than those on bare boards.

TABLE 1

Breakdown Voltage Ranges
for Different Nominal Separations

Separation	Bare Boards	Urethane Coated Boards
0.17 (0.0065)	320 to 800 Volts	400 to 5000 Volts
0.32 (0.0125)	520 to 1080	640 to 5300
0.64 (0.025)	560 to 1500	1160 to 5800

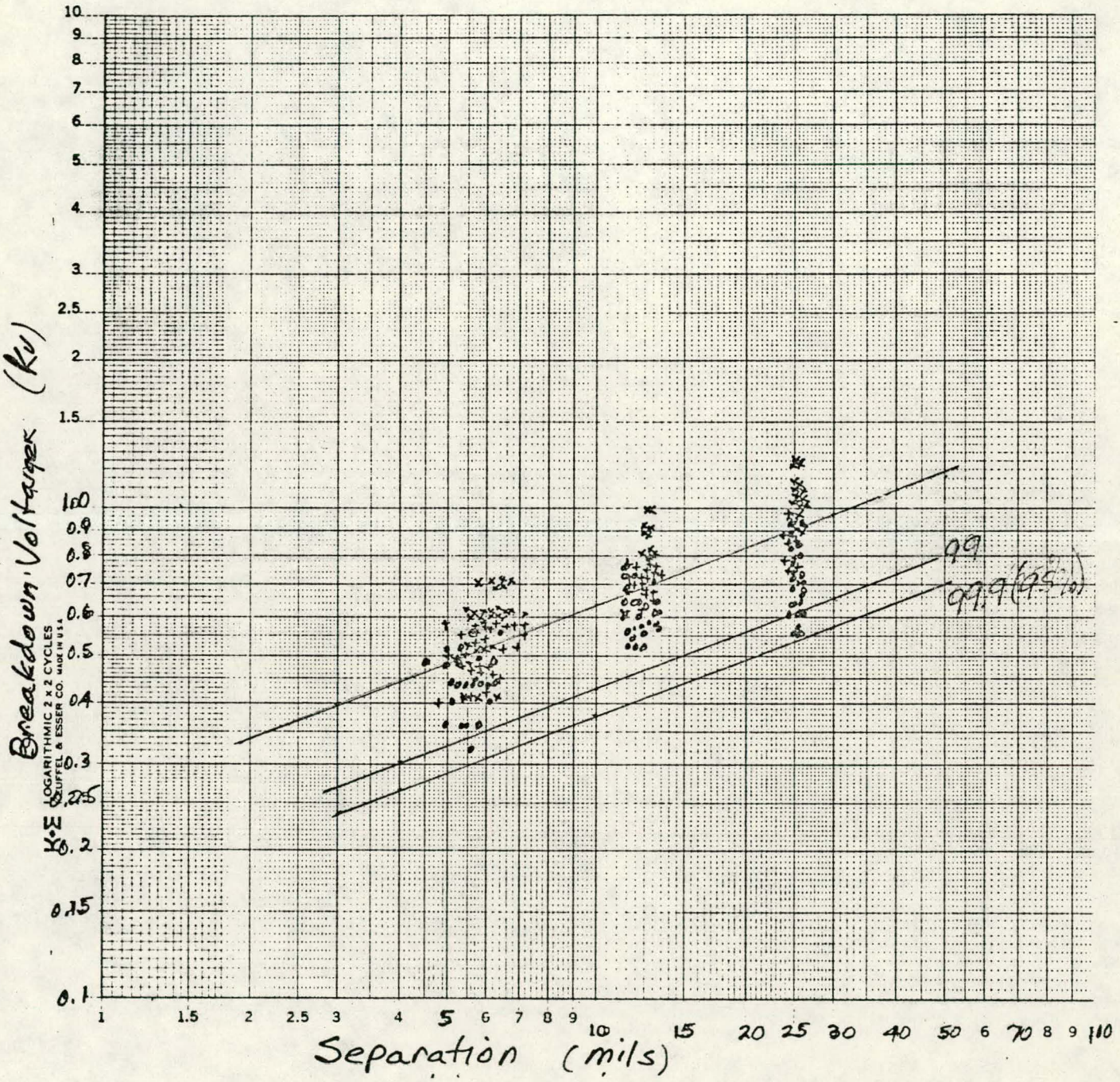

Figure 2. Breakdown voltages for different conductor separations on bare boards at 75°C/100% RH/289 Torr.

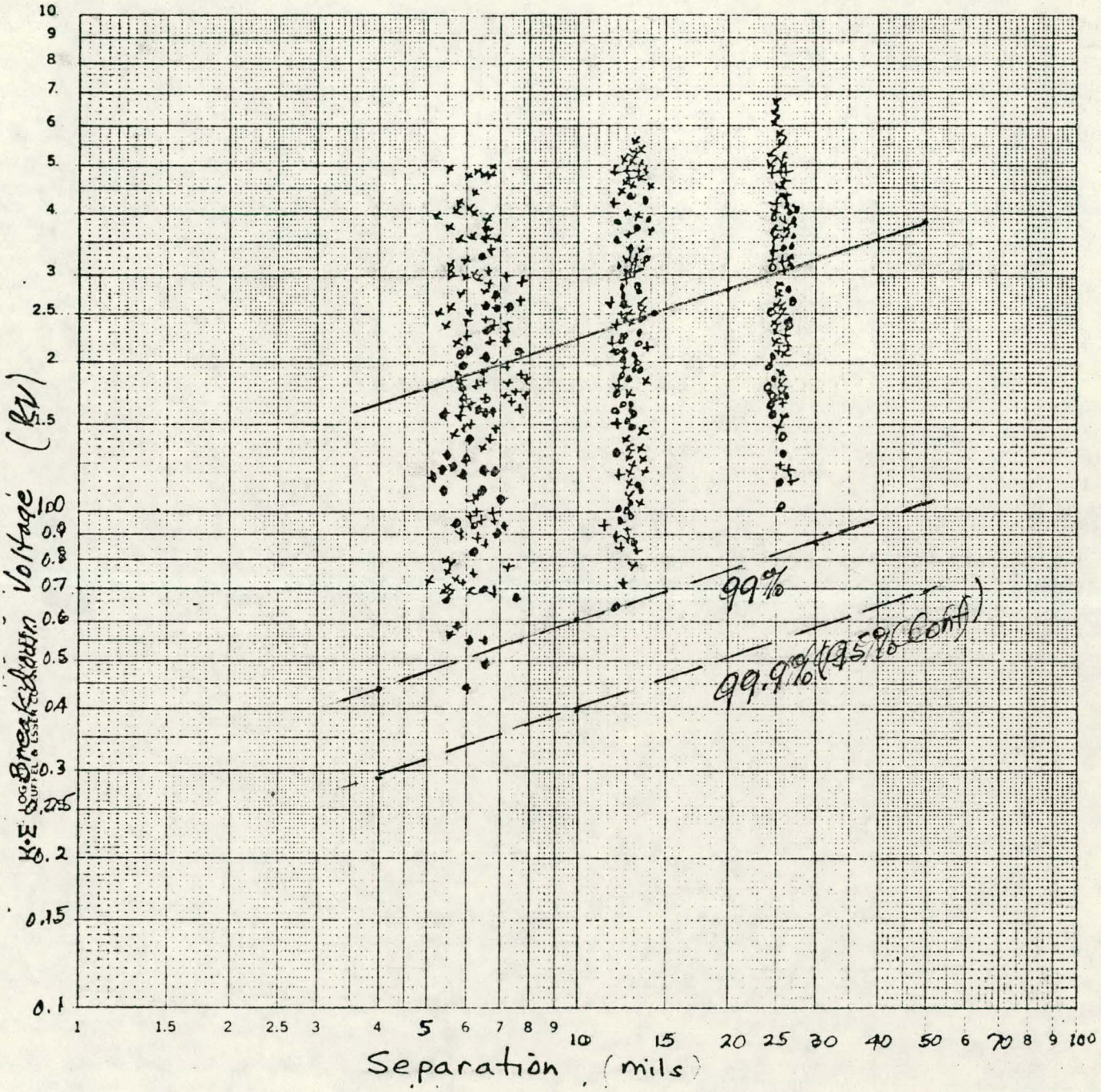

Figure 3. Breakdown voltages on different conductor separations on urethane-coated boards at 75°C/100% RH/289 Torr.

Figure 4 shows least squares curves for the different test sets. Delsen reported max and min values for the clearance distance of each section. Breakdown voltages were plotted using the average of their max and min values. Breakdown does not always occur at the minimum separation within a pattern section. Average breakdown voltage decreases nonlinearly with the length of conductor exposed to the voltage. The different slope for the coated SNLA set 2 measurements could be related to the 5 kV limit on the test equipment.

A limited number of breakdown measurements made at room conditions (23 $\pm$ 3°C, 10-30 percent RH, 0.88 kPa) showed breakdown levels 1.7 to 2 times higher than those for the worst case environment. Individual temperature, pressure, and humidity changes showed pressure to have the greatest effect on breakdown levels as one would expect. Temperature and humidity increases caused, at most, variations in the 10 percent range. These same temperature and humidity increases cause order of magnitude decreases in insulation resistance.

After conditioning for 7 days at 75°C and 100 percent RH, the first set of boards tested at SNLA showed extensive measling and a white crystalline-like residue on the conductors as illustrated in Figure 5. In a few regions of the 0.17 pattern, the white crystalline material bridged the conductors as illustrated in Figure 6. Electron microprobe examination indicated the white material to be a lead oxide or hydroxide. It could be cleaned from the board with an

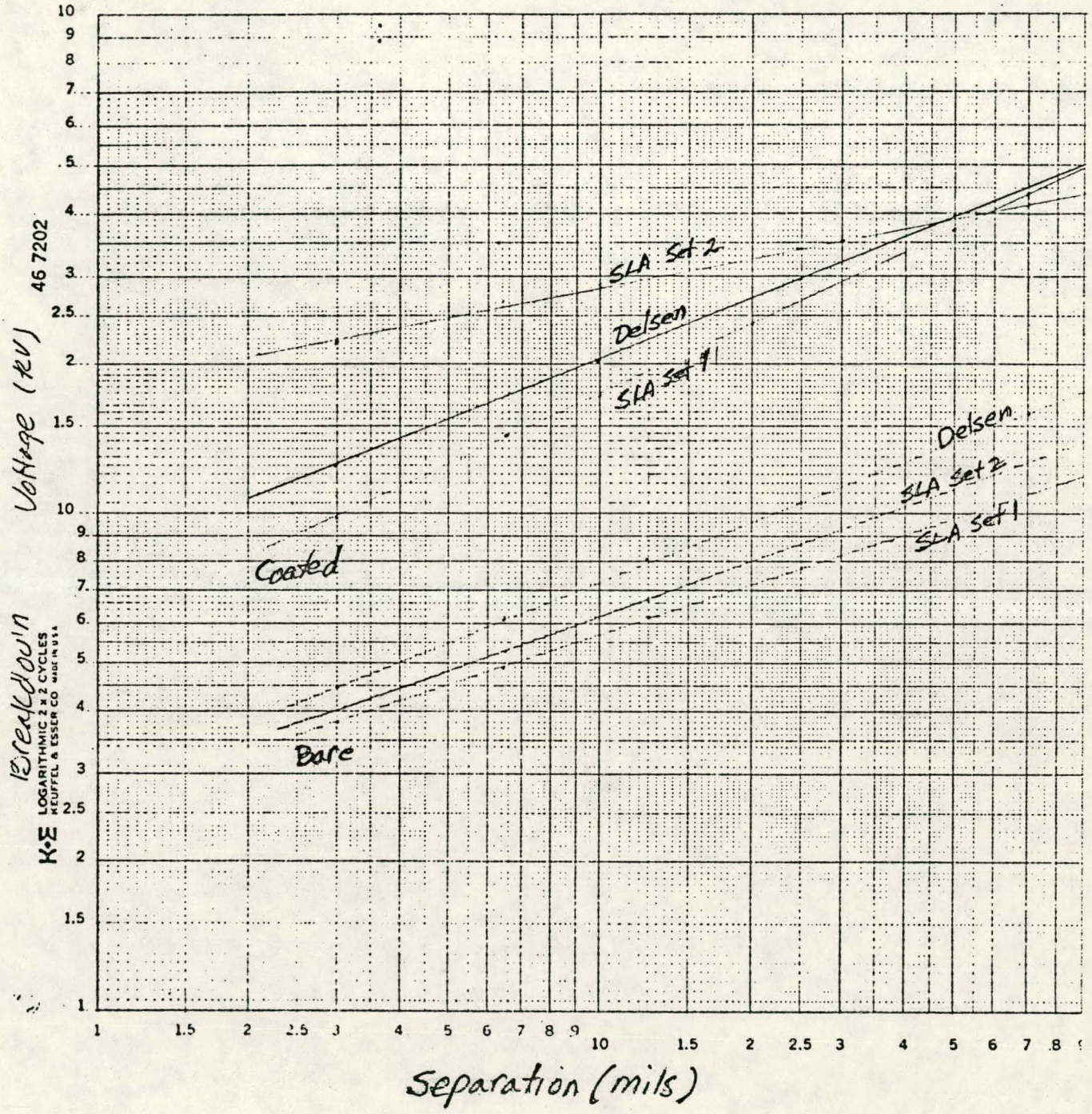

Figure 4. Comparison of least squares curves of test data from different testers.

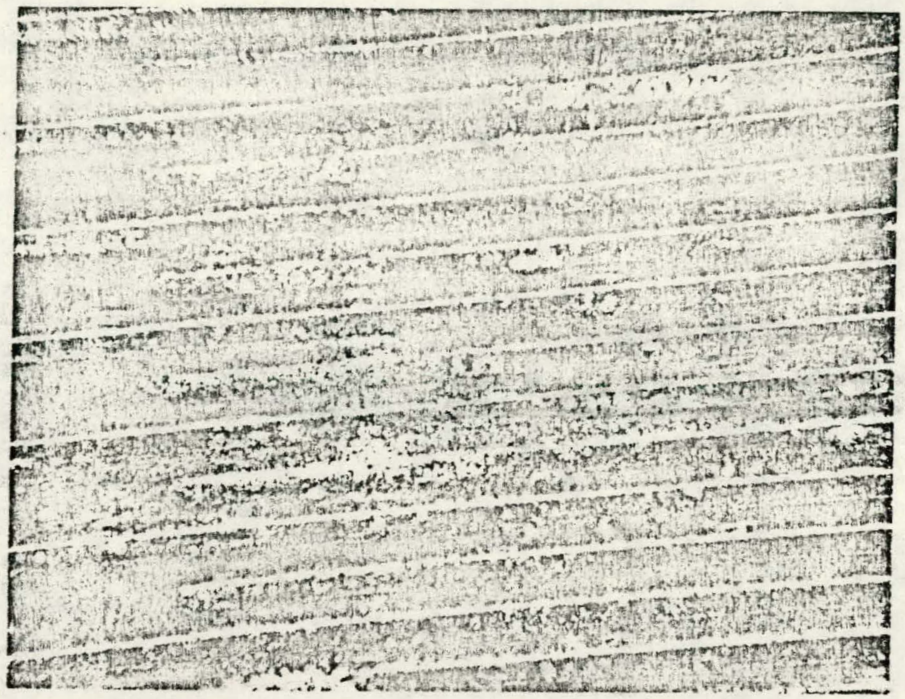

Figure 5. White corrosion product observed on SNLA test boards after conditioning at 75°C and 100 percent RH for 7 days.

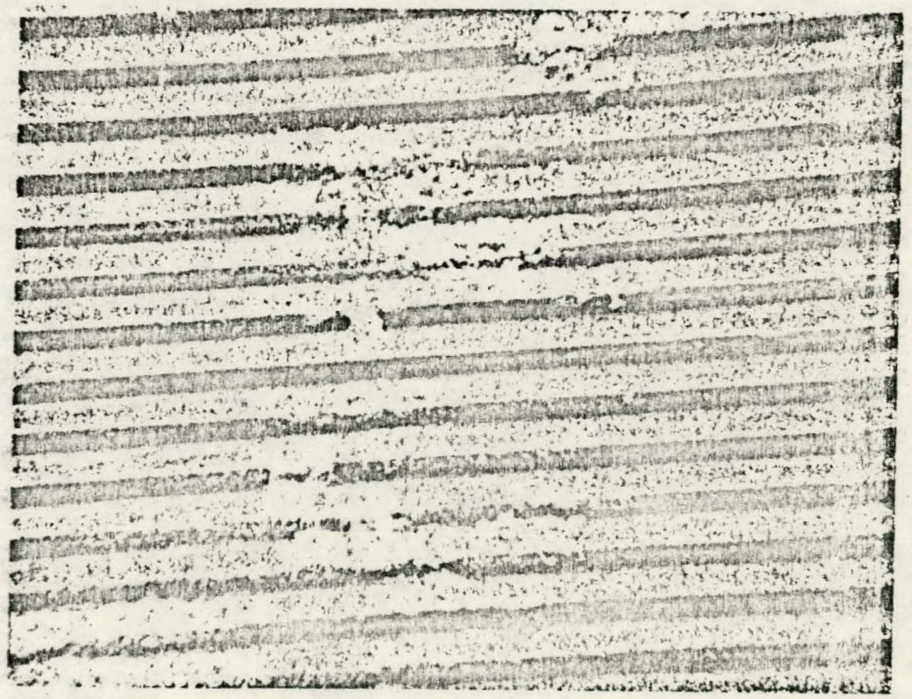

Figure 6. White corrosion product observed on a test pattern from a previous study after conditioning at 75°C and 100 percent RH for 1 week.

aqueous 20 percent by weight solution of ammonium acetate. Boards so cleaned and rinsed with deionized water, followed with 2 propanol, had breakdown voltages about 10 percent higher than the values obtained with the original corroded boards.

When boards from an earlier study[5] were given the same 75°C/100 percent RH/room pressure conditioning for 1 week, the conductor encrustation varied from none to heavy, which suggests that the corrosion is associated with the laminate material and processing which it receives in fabrication.

When Rockwell-Collins was informed of the corrosion and measling observed on the first set, they tested some of the laminate stock from which the boards were fabricated and found evidence of what D. R. Witherell described as the "Soft Resin Problem."[9]

When the second set of boards was conditioned at SNLA about 6 months after the first, the degree of measling and corrosion was very much less than the first set. Voltage breakdown was higher for the second than for the first set. Boards tested at Delsen and the other tester did not show the typical corrosion of the first set after the conditioning. These were tested a few months after the first set at SNLA.

Conductor Spacings Specified in Existing Documents

Figure 7 shows minimum clearances specified for various voltages in MIL-STD-275 and IPC-ML-910A for altitudes up to 3000 meters (10,000 feet). The step format came about from the application of different safety factors to the measured data for the different clearance intervals. Also plotted are the proposed VDE 0110 clearances assuming an inhomogeneous field, material group 2 and pollution degree 2. In the definition of pollution degree 2, normally only nonconductive pollution is anticipated. Occasionally, however, a temporary conductivity caused by condensation must be expected. As can be seen, there are significant differences shown in recommended clearances, especially in the low-voltage range.

There are some apparent inconsistencies which should be corrected with regard to requirements for dielectric withstanding voltage in IPC and MIL Specifications. For example, the Conformal Coating Specification, MIL-I-46058C, Section 4.8.7, specifies that a test separation of 0.76 ± 0.08 (0.030 ± 0.003) shall be capable of withstanding 1500 volts ac rms or 2100 volts peak at 60 Hertz for 60 seconds. As shown in Figure 3, a significant number of breakdowns can be predicted at or below this peak voltage. The voltage specified for this clearance in MIL-STD-275D, Section 5.1.4, Table 1, as shown in Figure 7, is 101 to 300 volts, that is, the voltage required in MIL-I-46058 is seven or more times that in MIL-STD-275.

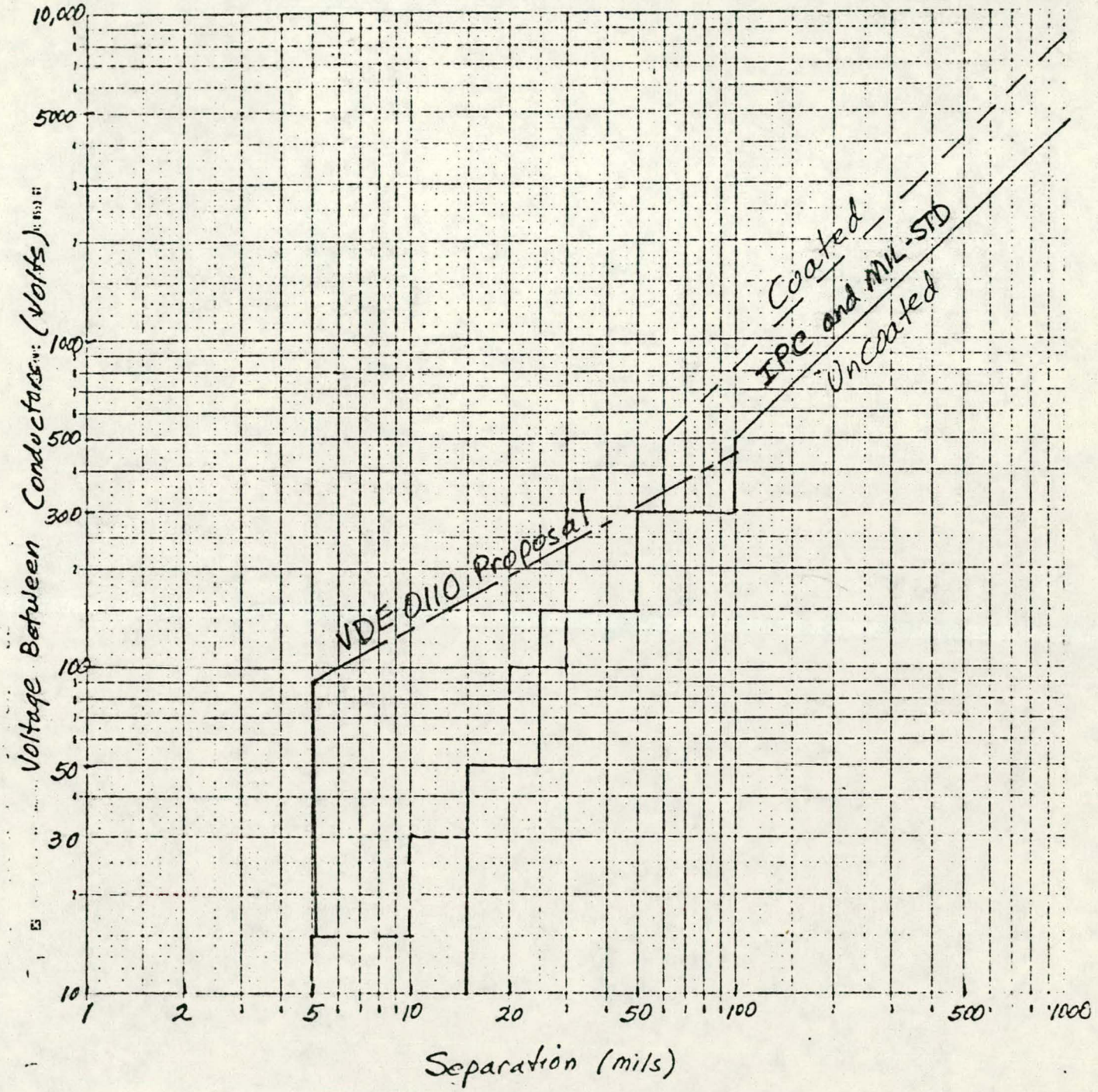

Figure 7. Clearance recommendations in MIL-STD-275D and IPC-ML-910A along with those recommended in VDE110b proposal for altitude to 3000 meters (10,000 ft). The VDE0110b proposal refers to a dc working voltage for material group 2, pollution degree 2.

Another instance is the requirement in MIL-P-55110C that the B pattern of IPC-B-25, i.e., 0.32 (0.0125) separation, be required to withstand without flashover 1000 volts dc for 30 seconds in accordance with Method 301 of MIL-STD-202. Figure 7 shows that the maximum recommended voltage for this separation in MIL-STD-275 is 30 volts, which is considerably less than the 1000-volt test voltage.

Recommendations

The voltage-clearance recommendations of this Task Group for both coated and uncoated boards for altitudes to 3000 meters (or 10,000 feet) are shown in Figure 8. These are based on voltage breakdown measurements from this study and from those previously reported, particularly the Lehner, Safran, Schau, and Weise study, with safety factors. This curve is essentially the same as the VDE 0110b curve in Figure 7. Also shown are least squares average and 99.9 percent (95 percent Confidence) limit curves for the data generated in this study. Voltage is shown as a continuous function of clearance in Figure 8 in contrast to the discrete step values in IPC-ML-910A and MIL-STD-275. For convenience, minimum clearances corresponding to some typical voltages are given in Table 2. A comparison of the worst case voltage level, 99.9 percent (95 percent confidence) curve, with the recommended voltage curve shows the safety factor to range from 2.6 for 0.13 (0.005) to 1.8 for 2.5 (0.100) separation.

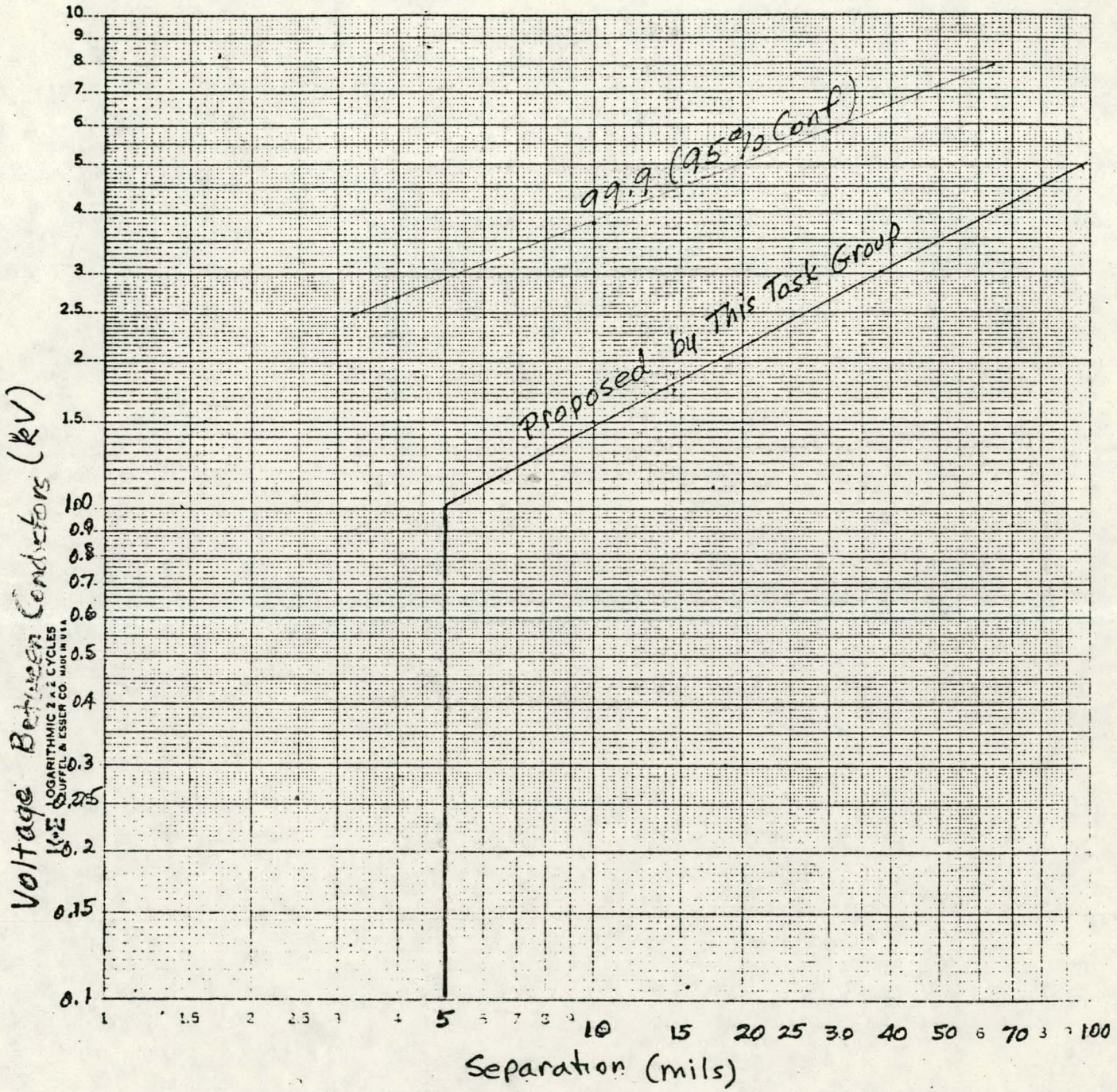

Figure 8. Voltage-Clearance recommendations of this Task Group for coated and uncoated boards to altitudes of 3000 meters (10,000 feet).

TABLE 2

Specified Minimum Clearances for
Different Voltage Levels Between Conductors

Voltage	Minimum Clearance
0-100 Volts	0.13 (0.005)
150	0.25 (0.010)
200	0.44 (0.018)
300	0.97 (0.038)
400	1.65 (0.065)
500	2.54 (0.100)

The clearances represent expected minimum or actual separations rather than nominal or design values; that is, the designer should apply the growth or positive conductor width tolerance expected in fabrication to determine minimum clearance.

Attempts made to determine corona effects at voltage levels just below expected breakdown levels were unsuccessful. Corona effects are not expected to be appreciable at the voltage levels given in this recommendation. For a few of the comb patterns the voltage was

maintained at 90 to 95 percent of expected breakdown level without breakdown or any appreciable rise in current level.

In view of the higher breakdown voltages for coated boards, it may appear strange that the spacing requirements for coated boards are the same as for uncoated boards; i.e., Figure 8 applies to both types. There were, however, sufficient breakdowns on coated boards in the voltage range at which bare boards broke down that caused both types to be included together. Breakdowns typically occur at coating defects on coated boards and do not reflect the inherent breakdown strength of the coating material. There is a reasonable probability that defects could occur in close proximity such that breakdowns would be observed in the voltage range for uncoated boards. Breakdown levels for coated boards appear to be a function of the adequacy of the coating process. Once breakdown occurs on a coated board, there is sufficient coating degradation that upon repeated voltage applications the breakdown level is typically much lower than the initial value. This is not true for uncoated boards, the breakdown levels for repeated voltage applications are generally within a few volts of each other.

Dielectric withstanding test voltages, which are used to determine the adequacy of insulation materials and spacings, should be selected on the basis of the pattern tested and the test environment in

accordance with the information of this report and other reported information, notably the Lehner, Safran, Schau, and Weise study.

As conductor separations have become smaller on board designs, there is increasing concern for the possibility of forming electromigratory filament shorts and low-insulation resistance paths between conductors. While the Task Group recognizes this concern, it has not directly addressed the problem. For boards that are to be used in humid environments the designer should refer to IPC-TR-468 and IPC-TR-476 for information and recommendations relating to these problems. However, because there is an increasing probability for insulation resistance problems and short formation from filaments, slivers, or particles at clearances of less than 0.17 (0.005), the minimum recommended clearance is limited to 0.17 (0.005).

A conformal or solder mask polymer coating will generally, but not always provide some protection against low resistance paths or shorts in addition to generally increasing the breakdown voltage levels. The use of such coatings or masks is recommended.

Breakdown voltage is a function of atmospheric pressure or altitude as well as separation, and a designer should apply a correction factor whenever the board is to be used at an altitude beyond the recommendations for this report or within a narrow altitude range. Correction factors which are based on the Paschen curve for air are given in Table 3 or can be obtained from Figure 9.

TABLE 3

Altitude Correction Factors for Clearance Distances

Altitude		Pressure		Multiplication Factor
Meters	Feet	Pascals	Torr	for Clearance Distance
0	0	1.013×10^5	760	0.69
2,000	6,560	0.800	600	0.87
3,000	9,840	0.700	525	1.00
7,600	24,930	0.385	289	1.82
10,000	32,810	0.265	199	2.64
25,000	82,020	0.027	20	26
30,000	98,420	0.013	10	54

The emphasis of this report has been on board conductor separations such as line-to-line, line-to-land, and land-to-land; however, it is equally important that recommended clearances be applied to connector elements, component leads, and other conductive parts of a board assembly. In a previous study, voltages for land-to-land breakdowns were found to be about 20 percent higher than line-to-line breakdowns.[6] Much of this difference could be attributed to smaller exposure of conductor length in the land-to-land measurements. Conductor edges in the line-to-line patterns were microscopically rough, presenting many sites for breakdown initiation.

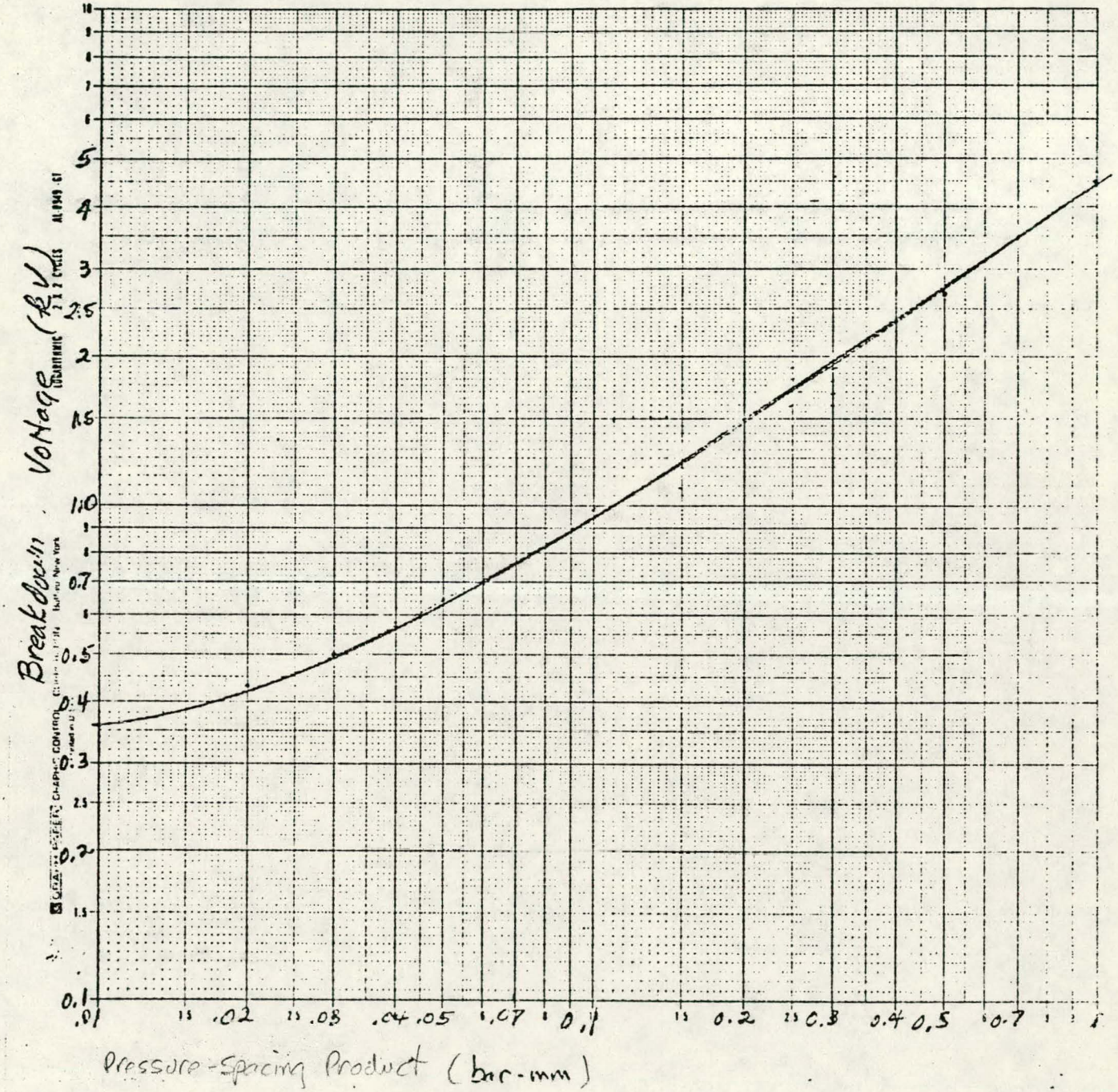

Figure 9. Paschen curve for voltage breakdown for air in a homogeneous field.

SUMMARY

1. Present clearance recommendations for different voltage levels between conductors on a printed board such as those in IPC-ML-910 are very conservative with respect to measured values, especially for the low-voltage range because of the large safety factors which were applied.

2. New clearance guidelines are proposed based on measurements made by this Task Group and on other published data. Voltage-clearance recommendations are presented as a continuous curve rather than in discrete steps as in current documents. The degree of risk assumed can be assessed by comparing this curve with the measured data for the worst case environment.

3. Recognizing the increasing tendency for electromigratory filaments and low-insulation resistance paths to form as conductor spacings narrow, a limit of 0.13 (.005) is recommended as the minimum conductor clearance. This limit will also reduce possible effects from particulate contamination and conductor edge slivers. For means of controlling or minimizing filaments and low-resistance paths, reference is made to other IPC Task Group publications addressing these problems.

4. Altitude or air pressure is the most important of the environmental factors affecting voltage breakdown. For instances in which there is a specific or unusual pressure environment, clearance correction factors are listed for different pressures. The effect of moisture and temperature variations on breakdown voltage appears to be minimal. This is in contrast to the appreciable effect they have on insulation resistance. Although corrosion products were seen on some of the conductors after exposure to the high humidity environment, even bridging the conductors in a few regions, there was only a minor reduction in breakdown voltage for these boards.

5. The large spread in breakdown voltages for coated boards reflects the quality of the coating process rather than the variability in inherent breakdown strength of the coating material. Despite the fact that no distinction is made between coated and bare boards in the clearance recommendations, a coating will, in most instances, provide higher breakdown levels than bare boards. In addition, a coating will offer protection from contaminates and abrasive or other mechanical handling damage, and its use is recommended whenever a board is exposed to an uncontrolled or degrading environment, unless restricted by mounting or other considerations.

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