DATA HANDLING FOR THE LEPTON DETECTOR *

D. Cutts, Brown University
T.F. Droege, Fermilab
H. Kasha, Yale University
L.E. Kirsch, Brandeis University
L. Littenberg, BNL
J.A.J. Matthews, Johns Hopkins University
M.S.Z. Rabin, University of Massachusetts
J. Scharenguivel, BNL

I. INTRODUCTION

The lepton detector group was charged with evaluating the data acquisition and processing needs of a "typical" lepton-oriented large-solid-angle detector. Motivated by recent developments from several groups,[1-4] we suggested a configuration of the data readout systems (including microprocessors), the control computer(s), and the local intersection computer substantially different from that in previous ISABELLE studies.

II. DESCRIPTION OF THE DETECTOR

As a "canonical" lepton detector, we have chosen essentially the 1975 design of Burnstein et al.[5] (Fig. 1); however, our group

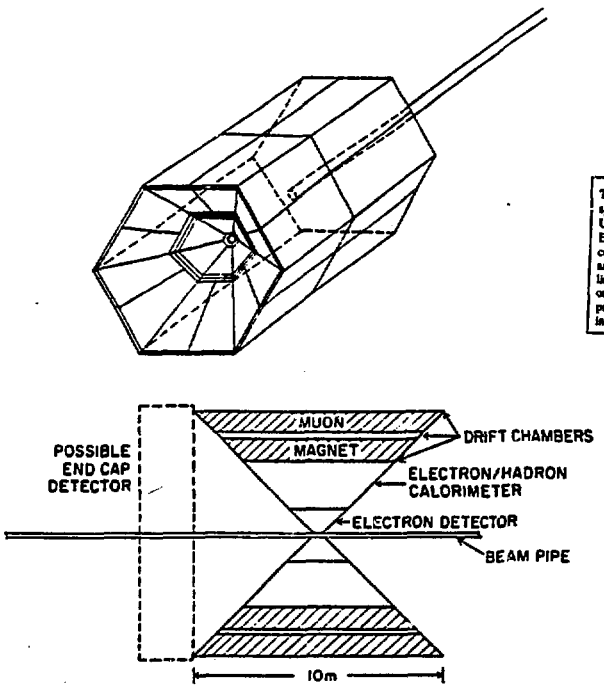

Fig. 1. Schematic drawing of a lepton detector. (From 1975 ISABELLE Summer Study, p. 20, BNL 20550.)

*Supported in part by the United States Department of Energy.

in no way wishes to endorse this design. This choice was motivated by the familiarity of this design (see also Imlay et al.[6] and Cutts[7]) and, most importantly, by its remarkable similarity (in concept and in experimental acceptance) with the BNL-CERN-Syracuse-Yale detector[8] at the CERN ISR. Consequently, the CERN experience[8,9] was extremely useful in estimating backgrounds, trigger problems, and computer requirements for the ISABELLE detector.

In detail, the detector was composed of six "sextants" (Figs. 1 and 2) and involves ~14,000 channels of readout, as enumerated in Table 1. It was envisioned that all data would be retained in

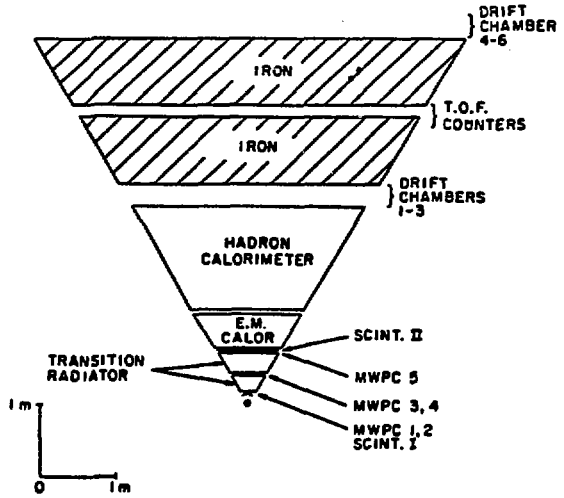

Fig. 2. End view of one sextant of the lepton detector.

deadtimeless storage while the event trigger (see Fig. 3) was being formed. This suggested the use of CCDs (analogue shift registers)[7,10] or digital shift register schemes.[11]

III. TRIGGERING AND DATA RATES

Typical single-particle triggers for the lepton detector would include electron (e), muon (μ), and momentum imbalance ($\vec{p}_{net}$) triggers.* Triggers would evolve in at least two steps: a pretrigger (utilizing fast logic, programmable gates, or hardwired logic) that takes ~200 nsec, followed by a full trigger (utilizing PRAMs,[13] analogue,[6] and/or digital processors[3] taking ~20 μsec. Examples of pretriggers and triggers are given in Table 2.

Typically transverse momentum thresholds or two-body transverse energy thresholds are adjusted to yield trigger rates of

*The total number of absorption lengths in the hadron calorimeter (1 m of steel) may be inadequate at ISABELLE.[12]

Table 1

Lepton Detector Elements

Component	Comparison: Willis' ISR Detector	Lepton detector[5,6]
1. MWPC 1,2	720 wires	600 wires x 2 ADC/wire = 1200 channels (1975 Study)
2. Scint. I, II	64 channels	15/sextant (I) 30/sextant (II) = 270 channels (1975 Study)
3. Transition radiation detectors (TRD)	496 wires	(a) 220 wires/sextant (b) 220 " " (c) 385 " " } Av 1 ADC/wire ~5000 channels (1975 Study)
4. Electromagnetic (em) calorimeter	704 channels	300 channels/sextant = 1800 channels (strip readout)
5. Hadron calorimeter	---	(a) 150 channels/sextant = 900 channels (strip readout)
	---	(b) ~772 phototube channels (1976 Study)
6. Muon drift chambers	---	. . . . . 4000 channels (~6000 channels if 10-m chambers impractical)
7. Muon TOF scint.	---	. . . . . 96 channels
		Total 14,000 channels

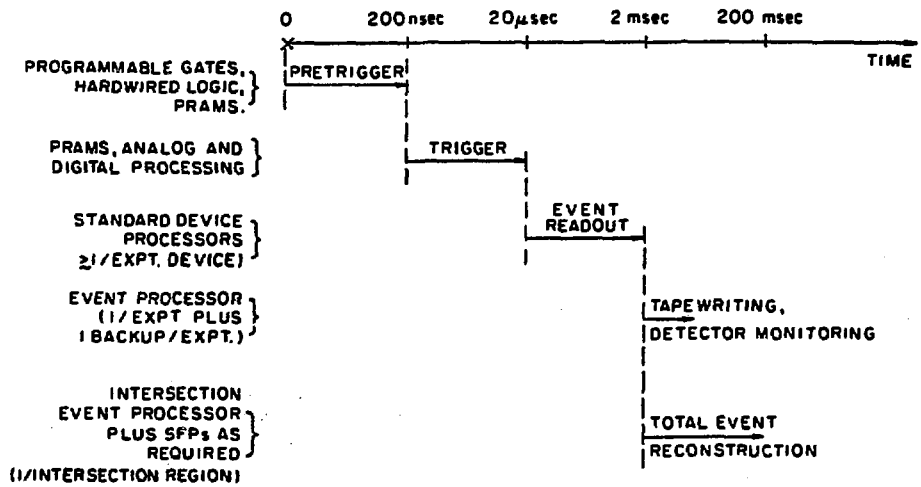

Fig. 3. Time flow of data for the lepton detector.

Table 2

Typical Triggers and Pretriggers

	Electron (e)	Muon (μ)	Momentum imbalance ($\vec{p}_{net}$)
Pretrigger $\geq 10^3$ rate reduction	Large localized electronmagnetic (em) calorimeter pulse.	Tight time coincidence between TOF counters and scint. I and II counters in the same sextant.	Weighted sums of em and hadronic calorimeter energies: $p_x = \sum_i \cos\phi_i$, $p_y = \sum_i \sin\phi_i$.
Trigger $\geq 10^3$ rate reduction	(a) Em calorimeter shower "narrow" Charged track extends into MWPC 1,2 (suppress γ conversions). Cuts result in ~100:1 enhancement of e/π.[8,9]	Correlate drift chamber "tracks" with TOF counters hadron calorimeter φ cells, em calorimeter φ cells, inner MWPCs. Impose $p_\perp$ threshold using inner and outer drift chambers. N.B.: $p_{\perp_{min}} \sim 4$ GeV/c just to penetrate to the outer drift chambers.	Correlate $\vec{p}_{net}$ with e,μ triggers for 2-body triggers.
	(b) Include prescalers for single-track triggers.		
	(c) Establish ≥2-body triggers: ee, μμ, eμ, ≥3 leptons, $e\vec{p}_{net}$, etc.		

≤10 per second. Even at a luminosity of $L = 10^{33}$ cm^{-2} sec^{-1}, the direct lepton rates for $p_{\perp lepton} > 4$ GeV are < 1 sec.[5,14] Hadron cross sections are 10^4 to 10^6 times as great, and jet cross sections 10^6 to 10^8 times as great. We note that recent theoretical models[15] predict hadronic cross sections ~100 times as great as cross sections used in previous Summer Studies.[16] This implies that single lepton rates (dominated by π's faking e's or μ's) are at the ~1/sec level only for $p_\perp$ thresholds ~8 to 10 GeV/c, and would have to be prescaled for lower minimum $p_\perp$ thresholds. Di-lepton trigger rates (ee, μμ) at the ~1/sec level should be possible with mass thresholds ~8 to 9 GeV.

The assumptions that the average charged plus neutral multiplicity is 8 in the detector,* that 5 CCD buckets are digitized per chamber pluse,[17] and that inactive elements are not read out, yield ~1300 16-bit words of chamber data per event (see Table 1). To this must be appended analogue data and bit patterns relevant to the pretrigger and trigger logic, plus adequate monitors of the pretrigger and trigger logic. Additionally there are fast scalers, beam luminosity information, etc., yielding a final total of ≤1000 32-bit words per event. At ≤10 events/sec this implies that a 6250-bpi tape is completed in ≥1 h.

IV. DATA READOUT AND MONITORING

The lepton detector data acquisition and monitoring system, schematically represented in Figs. 4, 5, and 6 and represented in time in Fig. 3, we designed to realize a number of specific goals.

a. The requirement of fast (~1 to 2-msec) event readout. This demands a priority encoding/decoding scheme to recognize only active detector elements[17] plus a high degree of parallelism in the readout. Thus typically one standard device processor (SDP) (Fig. 5) is associated with a physical device, e.g., MWPCs, transition radiation detectors, etc. This allows each subsystem of the detector to be operated independently in a stand-alone mode for debugging purposes.

b. Detector monitoring, alarming, calibration, detector performance histograms, data reordering, etc., should be done in parallel in the SDPs. This substantially reduces the work load for all following processors.

c. Data communications between all experimental computers and data processors should be via a standardized communications protocol, for which we utilize the FAST BUS.[18]

d. The experimental control computer termed the event processor (EP) is a mini- or microcomputer plus peripherals sufficiently inexpensive to have a backup for reliability.

e. Full-event reconstruction must be done on line on ≥10% of the data. This is done on the intersection event processor (IEP) which additionally utilizes specialized function processors[1-4] (SFPs) to enhance substantially the computing power of the IEP. Note that the only expensive computer (which cannot easily be duplicated), the IEP, is not essential for data acquisition.

Features of each of these systems are presented below in more detail.

---

*That is,

$$\left(\frac{dN}{dy}_{\text{charged}}\right) \sim 2\ (\Delta y_{\text{detector}} \sim 2)(1.5 \text{ for } \pi^0\text{'s}) + (2 \text{ lepton pairs})$$

totals to 8 particles. We note that the ISR ee pair data had less than the average track multiplicity.[9]

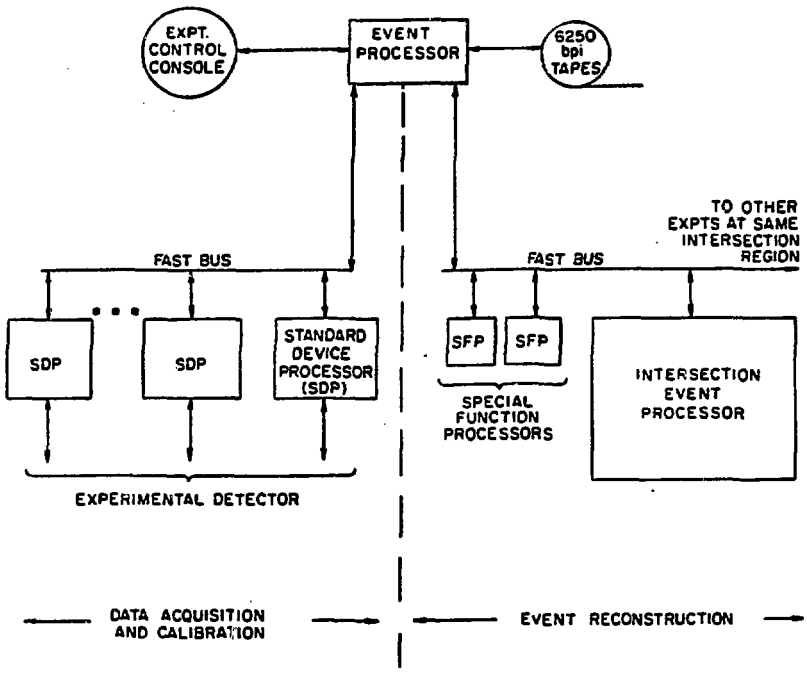

Fig. 4. Lepton detector processor "chain of command."

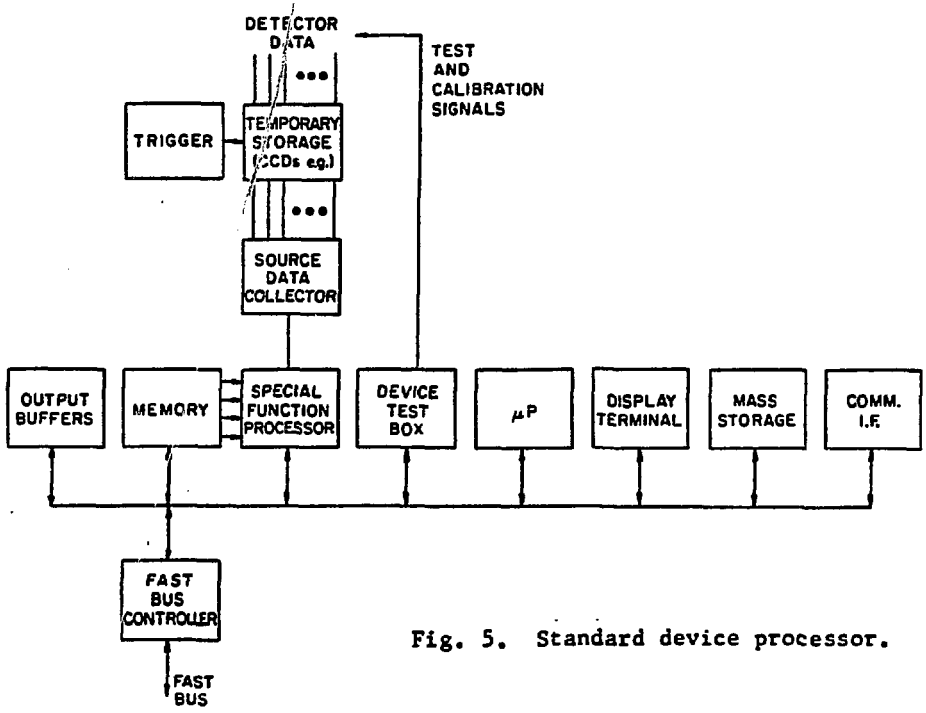

Fig. 5. Standard device processor.

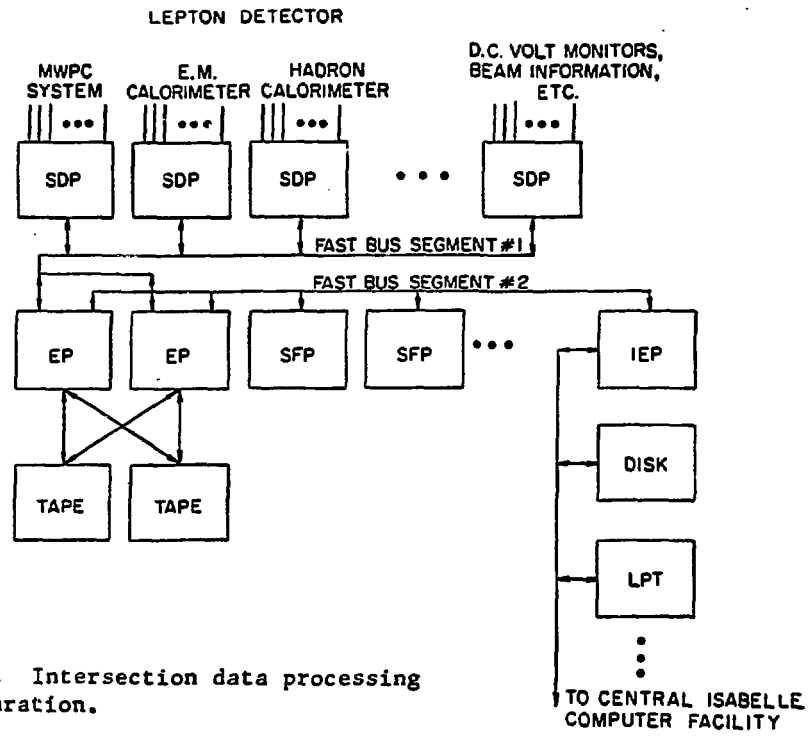

Fig. 6. Intersection data processing configuration.

A. Standard Device Processor

The SDP is the data collecting element of the system. It will be composed of a number of fairly standard building blocks that will evolve as hardware becomes faster and cheaper* (see Fig. 5). Long-term system compatibility will be maintained by adherence to the FAST BUS hardware and software protocol.[18]

The lepton detector readout is expected to proceed at a rate of 1 to 10 MHz, depending on the device. Each subsystem of the detector would typically be handled by a separate SDP, e.g., MWPCs; drift chambers; em calorimeter; hadron calorimeter; transition radiation detector; scintillators and trigger logic monitors; general dc voltage (etc.) monitor. A scan would be initiated by the controlling event processor by a "broadcast" command on the FAST BUS.

The source data collector (Fig. 5) is hardware specalized for the particular device being read out. It selects only active elements and passes the appropriate digitized data and address to the special function processor. The SFP then removes pedestals, applies linearity corrections, converts channel number to energy

*We estimate that a system consisting of a Z8000-like processor, a 64,000-byte memory, a 5-megabyte mass store, and a graphics terminal will soon be available for $5000.

(calorimetry) or distance (drift chamber) etc., reorders the data (if desired), and fills an output buffer in the local memory.

The microprocessor (μP), an "11/45 on a chip," is expected to do all the work required for monitoring, alarming, and calibration of the detectors. Standard device test circuits will generate charge, time, etc., calibration signals. Initiation of a SDP calibration and/or trigger checkout sequence in the responsibility of the event processor.

We note that a particularly good feature of this scheme is the early association and integration of the microprocessor SDP with the device it is handling. That is, the majority of the SDP is acquired and used for data acquisition even on the earliest detector prototype tests. This will result in the development of a library of test programs, resident in the SDP mass store, that are available for all later testing and debugging of the detector.

Preferably all SDPs are identical for maintenance purposes, software compatibility, etc. However this is not essential as long as all SDPs obey the FAST BUS hardware and software protocols.

B. Event Processor

The event processor (EP) is the control point of the experiment (see Fig. 4) and initiates all communications with the SDPs or the IEP via FAST BUS broadcast commands. Event processors are similar in structure to SDPs without SFPs and other data-collecting hardware. The event buffers in the EP would be adequate for at least two 10-event buffers, allowing efficient 6250-bpi tape operation. Since an EP plus peripherals is relatively inexpensive, it is suggested that for reliability a backup system be provided for the experiment, as shown in Fig. 6.

Typical responsibilities of the EP are to read/write 6250-bpi tape, to read output buffers of the SDPs, to pass (selected) events for full analysis to the IEP, to initiate all "begin run," "end run," "calibration," and "testing" procedures, and to display detector monitor histograms (from the SDPs or the IEP) as required.

C. Intersection Event Processor

The IEP is thought of as a computer similar in computing speed to a VAX11/780 or CDC6600. It should analyze $\geq$10% of the lepton detector data in real time and provide physics histograms of statistical significance, detailed studies of detector performance, and event displays.

By requiring the IEP to interface to the EP via the FAST BUS, we gain the capability of simply adding SFPs to the IEP to enhance its event reconstruction speed.[3,4] This is expected to enable the IEP to be at least as effective as a current CDC7600. Based on the ISR experience of Willis,[8,9] the time required for reconstruction of a lepton detector may be ~200 to 250 msec on a CDC7600. With SFPs, an IEP at ISABELLE would therefore be able to monitor $\geq$50% of the data in real time.

V. OFF-LINE COMPUTING

It was our opinion that the lepton experiment did not require a large central computer for event reconstruction. The data could all be analyzed on a dedicated IEP plus SFPs for track finding, shower pattern recognition, etc. Experimenters would also require access to an IEP before and after running the experiment for software development. This experience thus suggests that ISABELLE be provided with a number of IEP class systems at a central ISABELLE computing facility for the following uses:

a. Program and SFP development for the "on-line" reconstruction program.

b. Interactive/graphics facility for event displays.

c. Backup of the IEPs at the six interaction regions.

d. Final event reconstruction for all experiments, like the lepton experiment, that could be readily handled by an IEP plus SFPs.

Other facilities that should be supplied by the ISABELLE computing facility include the following:

a. Communications at high speed ($\gtrsim$4800 baud) and at low speed ($\sim$300 baud) for remote batch job entry or remote access to experimental data, detector constants, etc., stored in the "large mass store."

b. A "large mass store" for archival storage of the $\gtrsim 10^3$ tapes generated by the lepton (typical) experiment.

c. Software support for commonly used software on IEP, EP, and SDP systems (e.g., jet Monte Carlos, data-fitting packages, graphics).

d. Logic design and software design for development of the invaluable SFPs.

REFERENCES

1. T. Droege, Talk at this Workshop.
2. J. Dorfan, Talk at this Workshop.
3. G. Benenson et al., A hardware architecture for processing detector data in real time, in this volume.
4. P. Kunz, The LASS Hardware Processor, SLAC-PUB-1723, 1976.
5. R. Burnstein et al., in 1975 ISABELLE Summer Study, p. 9, BNL 20550.
6. R. Imlay et al., in 1976 ISABELLE Workshops, p. 24, BNL 50611.
7. D. Cutts, in ISABELLE 1977 Summer Workshop, p. 134, BNL 50721.
8. C. Kourkoumelis, Thesis, CERN 77-06, 1977; A.J. Lankford Thesis, CERN 78-3, 1978; J. Cobb et al., Nucl. Instrum. Methods 140, 413 (1977).
9. W. Willis, Private communication.
10. M. Zeller, in ISABELLE 1977 Summer Workshop, p. 140, BNL 50721.
11. E. Platner, MPS improvement plan, To be published.
12. M. Holder et al., Nucl. Instrum. Methods 151, 69 (1978). ← date
13. E. Platner et al., Nucl. Instrum. Methods 140, 549 (1977); A. Fucci et al., A new fast and programmable trigger logic, CERN preprint, 1977.

14. R. Peierls et al., Phys. Rev. D 16, 1397 (1977); C. Quigg, Rev. Mod. Phys. 49, 297 (1977); R. Palmer et al., Phys. Rev. D 14, 11[illegible] (1976).
15. R. Field et al., CALT-68-651, 1978; F. Halzen, Phys. Rev. D 15, 1929 (1977).
16. K. McDonald and J. Thaler, in ISABELLE 1977 Summer Workshop, p. 160, BNL 50721.
17. M. Zeller, Talk at this Workshop.
18. L. Leipuner, Some notes on the FAST BUS system, in this volume.