SLAC-PUB-3464
October 1984
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VERSATILE CAMAC POWER SUPPLY CONTROLLER-MONITOR WITH BUILT-IN RAMPING AND RIPPLE MONITOR*

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SLAC-PUB--3464

DE85 002686

Abstract

An integrated power supply controller-monitor has been designed and is in use to control "large" power supplies for SLC DC magnets. This single-width CAMAC module contains a 14-bit DAC, a 14-bit ADC, and several channels of optically coupled digital status and control signals. Additional features include built-in selectable ramping rates, self-test capabilities, and a ripple monitor circuit to measure AC ripple in the power supply current.

Introduction

For control and monitoring of large current regulated power supplies for SLC magnets, the following philosophy was adopted: the current set point would be transmitted from CAMAC to the power supply as an analog voltage in the range 0 to +10 V, and the actual current would be monitored with a transductor which delivers a DC signal in the range 0 to +10 V to CAMAC, proportional to the DC current. Digital control of power supply "on-off" would be provided by optically coupled signals from the module, and status of relevant signals (such as interlocks) would likewise be monitored by the CAMAC module.

An integrated function CAMAC module (PSC, Power Supply Controller) was designed based upon these ground rules unifying current control, current monitoring, digital control and status in a single "standard" module. (See Fig. 1, PSC photograph.) This module is connected to each large power supply via an interface chassis, thereby permitting customizing to the particular supply characteristics, and in addition eliminating any high voltages from the CAMAC crate for safety.

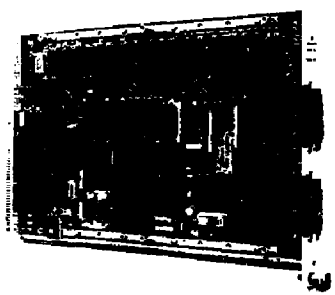

Fig. 1. PSC Photograph

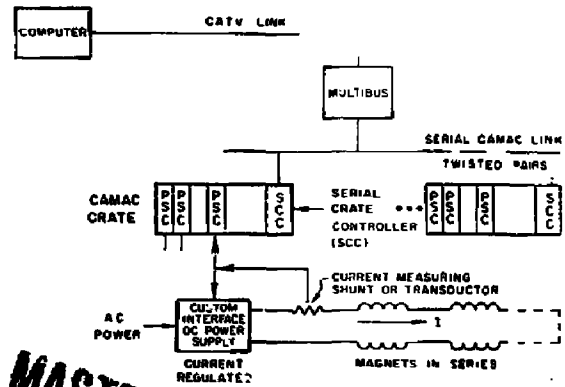

Fig. 2. Application Block Diagram

A block diagram of the position of this module in the SLC control system application is shown in Fig. 2. As a result of the general architecture of this system, it was decided to include power supply "ramping" at the module level to simplify software, reliably standardise magnets, limit current overshoot, and most importantly, reduce traffic on the serial links.

Note that in this system the computer(s) can be used to close the current control loop, at least for slow drifts of current. In other words the *long term* stability is determined primarily by the stability of the transductor and ADC, and not the power supply itself.

Overall Description of the Module

A simplified block diagram of the unit is shown in Fig. 3.

The key elements are the 14-bit DAC for the analog output, and the 14-bit integrating ADC for measuring the DC voltage from the transductor. The latter is preceded by a differential amplifier for true differential voltage measurements.

Normally the DAC is driven from a counter with program selectable ramp rates in the range 0.5 s to 134 s full scale. The ADC is of the slow (1/30 s) integrating type to reject ripple, and a register is provided so that the current can be read asychronously from CAMAC. A common crystal clock supplies pulses for the ramping circuits and the ADC.

Solid state multiplexers are included to permit connection of the DAC to the ADC internally for self-test and calibration. For more rapid self-test, ramping may be eliminated.

A ripple-monitor circuit converts the AC ripple to DC, and is AC coupled to the input current monitor. Using the same solid state switching, the output of this circuit can be read by the ADC to measure magnet current ripple. All of these operations are under direct CAMAC control for versatility and simplicity of the unit.

* Work supported by the Department of Energy, contract DE-AC03-76SF00515.

Presented at a Poster Session of the Nuclear Science Symposium, Orlando, Florida, October 31 - November 2, 1984.

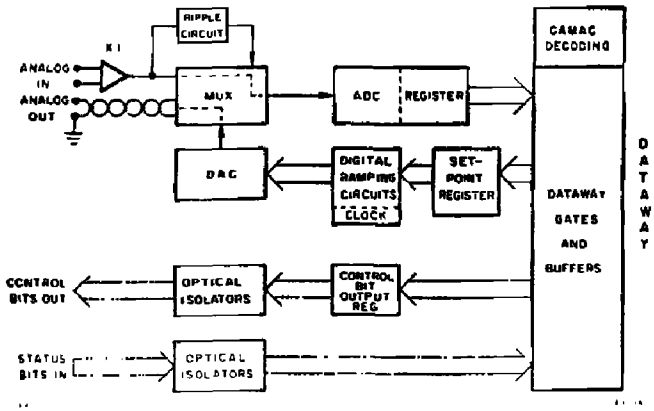

Fig. 3. Simplified Block Diagram

For control of the power supply, six optically isolated digital outputs are provided, two pulsed and four latched. Likewise for monitoring of supply/magnet status, eight optically isolated digital inputs are provided.

Linear Front End Switching and Ripple Circuit

A simplified block diagram of the front end of the module is shown in Fig. 4. The analog input is fed into the 14-bit integrating ADC through a differential instrumentation amplifier (AD3630) of ultra high temperature stability with gain one, and an analog solid-state switch of SPST (PMI SW-01BQ). The input impedance to the differential amplifier circuit has been chosen at 10 MΩ. Input voltage protection for over ± 15 V inputs is provided.

The output of the differential amplifier is also coupled into the Ripple Detection circuit which converts analog input signals in the range 10 Hz to 1 kHz into DC by a full-wave precision rectifier circuit which converts average ripple in the range of 10 mV to 100 mV peak-to-peak with 10% accuracy.

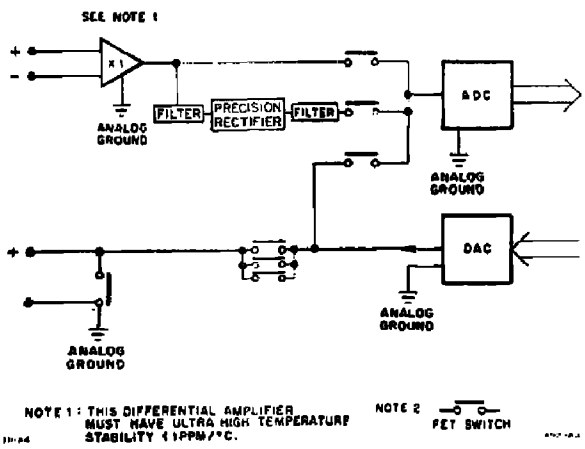

Fig. 4. Front End Switching

A single-ended DC analog output (0 to +10 V) is transmitted from the 14-bit DAC to the power supply through three SPST analog switches. These switches are connected together in parallel to maintain less than 30 Ω on-resistance of the multiplexer. In the special case of self-test mode in which the DAC output is connected to the ADC input for self calibration, the DAC output is disconnected and the front panel analog output is analog-grounded in the PSC with another solid-state switch.

Module Electrical Specifications

Summary specifications are shown in Table 1. Linearity and temperature stability tolerances for the analog output and input are quite tight.

Table 1. Specifications

- **Analog Output**
  - 14-bit DAC
  - 0 to +10 V range
  - ± 0.003% integral linearity
  - Stability ± 5 PPM/°C
- **Analog Input**
  - 14-bit Integrating ADC
  - Differential Input
  - 0 to +10 V range
  - ± .005% integral linearity
  - Stability ± 5 PPM/°C
- **Digital Output (Control)**
  - Six bits: two pulsed, four latched
  - Optically coupled
- **Digital Input (Status)**
  - Eight bits
  - Optically coupled
- **Ramping Rates (Full Scale)**
  - .532 s to 136.3 s (seven settings)
- **Ripple Measurement**
  - 10 Hz to 1 kHz range
  - 10 mV to 100 mV peak-to-peak
  - ± 10% accuracy

Component Descriptions

Intersil ICL7104-14 with ICL7668 with 14-bit resolution forms a precise Auto-Zero and true dual slope integration ADC. The conversion timing with 150 kHz internal clock frequency takes 0.15 s maximum in three phases: Phase 1 (auto-zero, 33 ms), Phase 2 (integration, 33 ms) and Phase 3 (deintegration, 66 ms).

Key components are summarized in Table 2.

Table 2. Key Components

- DAC — Hybrid Systems DAC 9377-16-4
  14 bits, 10 V full scale
- ADC — Intersil ICL7104-14, ICL8068
  14 bits, 10 V full scale
  Integrating, 33.33 ms
  .15 s conversion time
- Optical Couplers — Motorola MOC119, HP HCPL-2731

For the ADC the half-point voltage reference (+5 V) of PSR is achieved by a +5 V Precision Voltage Reference (PMI REF-02AZ). It has 3 PPM/°C typical temperature stability and provides an ultrastable output.

The DAC (Hybrid Systems DAC 9377-16-4) used in the PSC is a 16-bit version, used in 14-bit application with offset and gain adjustments of less than ± 1% around the nominal value. Both the ADC and DAC are monotonic.

The six bits of the digital control voltage outputs are transmitted to the power supply through opto-isolators (Motorola MOC119) of excellent frequency response (30 kHz typical) and isolation resistance of 10^{11} Ω. The devices are used for the case I = 30 mA at V = 1 V.

The digital status inputs (eight bits) from the power supply are coupled to the PSC through opto-couplers (HP HCPL-2731) of low input current (0.5 mA) and low output saturation voltage (1 V typical).

Digital Control and Status

Typical assignments for the control and status bits are shown in Table 3 for the SLC application. All interlocks are independent of the PSC module, which is used to monitor *summary* interlock status. The power supply can of course be controlled locally as well as via the computer. Bit 6 indicates local control to the computer. The power supply "off" function is inherent in removing ENABLE (Bit 3).

Table 3.
Typical Example of Control and Status Bit Assignments

	Control Bits (6)		Monitor Bits (8)
1.	DC ON	(Pulsed)	Power Supply Interlocks
2.	--		Magnet Interlocks
3.	Enable	(Latched)	System Ready
4.	Polarity Set	(Latched)	DC ON
5.	--		Polarity
6.	--		Local/Remote
7.			--
8.			--

CAMAC Operations

The operation of the PSC is condensed in Table 4. F(16)A(0) loads the set point register and initiates ramping at the rate previously set by F(17)A(0). F(17)A(1) gives direct control over the analog multiplexer to select one of several ADC modes: 1) Normal, 2) DAC Monitor, 3) Self-Test, 4) Ripple Monitor. This operation is of course normally followed by F(0)A(1), Read ADC, after a short delay to allow for the ADC to cycle (about .15 s).

Table 4. CAMAC Coding (Condensed)

F(16) A(0)	:	Write set point register
F(17) A(0)	:	Write ramping rate register; .532 to 136.3 s, or no ramp
F(17) A(1)	:	Select ADC mode; Input, Ripple, DAC Monitor, Self-Test
F(0) A(1)	:	Read ADC
F(16) A(2)	:	Write Digital Out, 6 bits
F(0) A(2)	:	Read Digital Input, 8 bits (Read Digital Output Registers, 6 bits)

Special Provisions

At the request of power supply and software engineers, several interlocking features were built-in to the module to prevent damage to power supplies/magnets. For example it is not permissible to set a ramping time of zero (no ramping) except when the unit is in Self-Test mode. In this mode the analog output to the power supply is zero, and the supply cannot be damaged by excessive ramp rates.

Acknowledgments

The authors wish to acknowledge the important contributions of R. Melen and M. Breidenbach, who conceived and supported the development of the PSC, M. Berndt who emphasized the importance of "ramping," and E. Cisneros who designed the ripple monitor circuit.