2

A HIGH-SPEED NONVOLATILE CMOS/MNOS RAM

G. F. Derbenwick, W. D. Dodson, and
R. J. Sokel

Sandia Laboratories
Albuquerque, NM 87185

ABSTRACT

A bulk silicon technology for a high-speed static CMOS/MNOS RAM has been developed. Radiation-hardened, high voltage CMOS circuits have been fabricated for the memory array driving circuits and the enhancement-mode p-channel MNOS memory transistors have been fabricated using a native tunneling oxide with a 45 nm CVD Si_3N_4 insulator deposited at 750° C. Read cycle times less than 350 ns and write cycle times of 1 μs are projected for the final 1Kx1 design. The CMOS circuits provide adequate speed for the write and read cycles and minimize the standby power dissipation. Retention times well in excess of 30 min are projected. The design provides for CMOS compatible operation and bit write and erase operations. Power supply requirements are 0, +12.5, and +25 V. Write and read speeds are maximized by using two differentially-sensed transistors per bit, performing simultaneous write and erase operations on each pair of transistors, and inhibiting the write-erase pulses if the bit is already written in the desired state.

Previously, the major obstacle in fabricating high-speed MNOS circuits has been the development of a reliable high-voltage

CMOS technology which provides the required memory array isolation for performing the write and erase operations. The circuits discussed here utilize the structure shown in Figure 1. N-wells are diffused into p-type substrates rather than the more conventional p-wells into n-type substrates. High drain breakdown voltages in the n-well are obtained since lower well doping densities are required to get -2V p-channel threshold voltages than to get +2V n-channel thresholds. A shallow boron threshold adjust implant provides for full enhancement mode operation. The p-channel memory array is automatically isolated in an n-well without having to resort to epi or SOS material.

The write characteristics of a discrete memory transistor are shown in Figure 2. Adequate differences between the two threshold voltage states are obtained for 500 ns, ±25V write pulses.

The circuit design uses separate bit line decoders to permit the simultaneous write-erase operations, and separate word line drivers are used for the two transistors per bit. A clock provides the timing for both the read and write cycles. This same design can function as an EAROM if the memory transistor native oxide is replaced with an intentionally grown oxide.

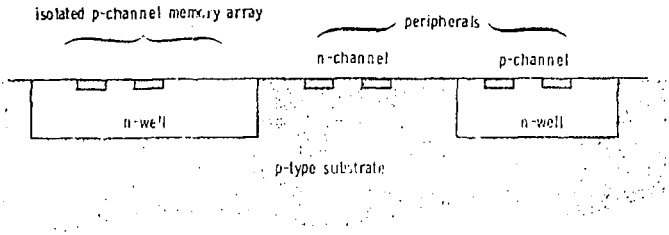

Figure 1. Cross section of high-voltage CMOS structure. The oxide and metallization are not shown.

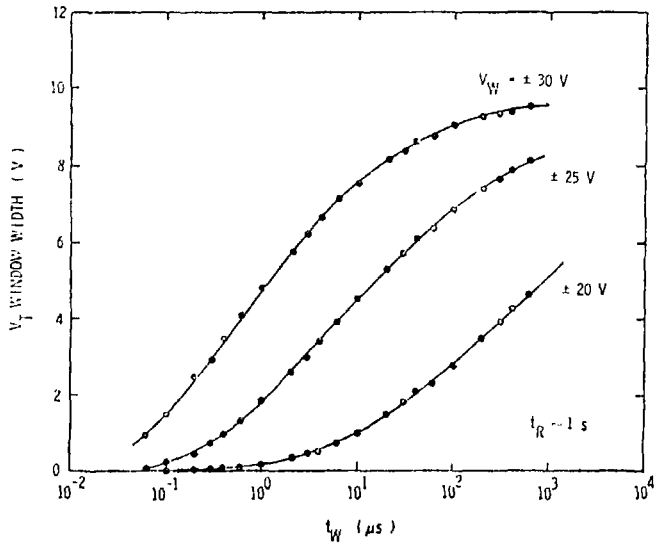

Figure 2. Typical MNOS memory transistor write characteristics.