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THE BROOKHAVEN SEGMENT INTERCONNECT

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ABSTRACT

We have performed a high-energy-physics experiment using a multisegment Brookhaven FASTBUS system. The system was composed of three crate segments and two cable segments. We discuss the segment interconnect module which permits communication between the various segments.

INTRODUCTION

This paper describes the Brookhaven Segment Interconnect which we are presently using in AGS experiment 749[1]. The segment interconnect permits communication between the various FASTBUS segments. This experiment uses three crate segments and two cable segments. Our first experiment which used FASTBUS, E735[2], utilized only one crate segment.

The segment interconnect comes in two types--one with the cable segment as the upper segment and the crate segment as the lower segment, and one with the crate segment as the upper segment. If the address on the upper segment is inside the address range of the segment interconnect, it will assert WAIT in reply to AS and request control of the lower segment. This address range is set within the module with wire jumpers. WAIT simply inhibits AS timeout. When it has control of the lower segment, it asserts the address on the lower segment and a deskew time later it asserts AS. If it does not receive AK or WAIT within the timeout period it negates WAIT on the upper segment. However, in a normal transaction it will receive AK which it passes on to the upper segment. The data part of the FASTBUS cycle then takes place. A similar transaction from lower to upper segment takes place if the address on the lower segment is outside the address range of the segment interconnect. Except for the WAIT line which inhibits timeout, the master follows the same protocol whether the slave is on his segment, or another segment above or below him. Thus the segment interconnect is transparent to the master.

A serious problem could occur if a master with control of the upper segment asserts an address which lies on a lower segment while simultaneously a master with control of the lower segment asserts an address which lies on an upper segment. In this situation, both segments are hung. The segment interconnect then asserts BK and negates WAIT on the lower segment. This informs this master to relinquish control of the bus and "try again later". The "winning" master then gains control of the lower segment and completes his transaction.

CABLE SEGMENT

Data transfers on the cable segment follow the standard FASTBUS protocol. Thus any number of FASTBUS modules, beside the segment interconnect may reside on the cable segment. This experiment uses two cable segments, one seventy-five foot long and one fifteen foot long. The segment interconnect has front panel connectors for the cable segment. There are eight twenty conductor connectors placed four high and two wide for the eighty FASTBUS lines. If the segment interconnect is placed at the end of the segment, a termination card is inserted into four of the connectors.

It is not possible to use a wire-OR on a long cable segment. Most FASTBUS lines are driven by only one master at a time. The six arbitration AL lines are an exception. We have expanded these lines such that each logical AL signal now consists of two physical lines which transmit the signal in opposite directions. Each master then has two drivers and two receivers for each logical AL line. The physical AL line is terminated (100 Ω to - 2V) at the receiver. A master asserts an AL line by driving it in both directions and receives it as the OR of the signals from the two receivers.

BROADCAST

Broadcast is initiated when a master writes into the broadcast register of the segment interconntect. The broadcast register address is set within the module with wire jumpers. There are two types of broadcast. Only the lower segment of the segment interconnect receives a local broadcast, while all segments below the segment interconnect receive a global broadcast. The global bit is the most significant bit of the broadcast word. Following a local broadcast request, the segment interconnect attempts to gain control of the lower segment. Once it has control it enables the broadcast register onto the A/D lines and asserts BC and AK and drops GK allowing arbitration for the next cycle to begin. It is necessary to assert AK because the next "winner" of the arbitration process is allowed to take control of the segment when AK is low. A deskew time later it asserts DS. The modules on that segment latch the A/D lines on the coincidence BC•DS. After 100 nsec. the segment interconnect drops BC and DS and a deskew time later AK and the A/D lines.

The global broadcast uses two lines not otherwise used. One is the last segment (LS) line. The segment interconnect pulls this line high (with a diode to ground for example) on its upper segment. With no such segment interconnect the line will be low. Thus if the LS is low on the lower segment the segment interconnect "knows" where are no segments below. The other is the broadcast wait (BW) line. This line is necessary to avoid the wire OR problem on cable segments.

When a segment interconnect receives a global broadcast on its upper segment it asserts the BW line (or WAIT line on a crate segment) and attempts to gain control of the lower segment. When it has control it asserts BC, AK and the A/D lines. If it is the last segment (LS line is low) it also drops the BW line. When the segment interconnect that originated the broadcast sees the BW (or WAIT) line go low it asserts DS for 100 nsec and then drops BC and DS and a deskew time later AK and the A/D lines. Arbitration for the next cycle begins after the BW (or WAIT) line goes low.

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REFERENCES

[1] AGS Proposal #749 (unpublished).
[2] S. Blatt, et al., Phys. Rev. D27, 1056 (1983).

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