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THE VERNIER DELAY UNIT*

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Abstract

This module will accept differential ECL pulses from the auxiliary rear panel or NIM level pulses from the front panel. The pulses are produced at the output with a fixed delay that is software programmable in steps of 0.1 ns over the range of 0.1 to 10.5 ns. Multiple outputs are available at the front panel. Minimum delay through the module is 9 ns.

Introduction

One of the most critical timing specifications for the SLC machine occurs at the injector and ejector magnets for the Damping Ring. It has been determined that the trigger pulses to the magnets must be controlled to 0.1 ns. The primary source for all trigger pulses for the SLC machine is the Programmable Delay Unit (PDU). The PDU generates a 67.2 ns wide pulse with delay increments of 8.7 ns. The gap between the required accuracy and that available from the PDU requires the design of a new module that is called the Vernier Delay Unit (VDU). This module accepts the 67.2 ns pulse from the PDU and is capable of increasing the delay in steps of 0.1 ns from 0 to 10.7 ns plus the minimum 9 ns delay.

The module has two totally independent channels. The pulse input to the module is software selectable from either the auxiliary backplane or a front panel Lemo connector. The auxiliary backplane pulses are to be the 67 ns differential ECL pulses from the PDU. The front panel input is to be a NIM level (-0.7 V 50 Ω termination).

With the exception of the Pos 5 V signal, all output pulse widths will track the input pulse widths. The following outputs are available on the front panel:

1. Differential ECL
2. NIM level
3. Pos 5 V, 500 ns wide pulse

The delays for the two channels are independently software programmable over the range of 0 to 10.7 ns. The delay is achieved by utilizing the PECLDL Programmable Delay Lines that are available from Engineered Components Company of San Luis Obispo, California. Two units were used per channel: the PECLDL 2.8-0.1 and the PECLDL 2.8-0.6.

These delay lines are connected in series, and both are 4 bit programmable. The 2.8-0.6 model produces stepped delays in increments of 0.6 ns from 0 to 9.0 ns. The model 2.8-0.1 has increments of 0.1 ns and is programmable from 0 to 1.5 ns. Each unit presents a minimum of 2.8 ns delay. Added to this 5.6 ns delay is the VDU internal delay of approximately 3 ns, giving a minimum delay of approximately 9 ns. For all of the testing and calibration, this fixed delay is measured by programming 0 delay to the module and measuring the delay between input and output pulse. All subsequent delay measurements made during calibration and testing were corrected to present incremental delays that do not include this fixed value.

The two programmable delays in series [0.6 ns and 0.1 ns] will have the condition that some delays which are to be requested could be requested by several different programs. For example: If we wish to request a delay of 1.5 ns, there are three possible choices:

	0.6 Program	0.1 Program		Total Delay
1.	2 = 1.2	3 = 0.3	=	1.5 ns
2.	1 = 0.6	9 = 0.9	=	1.5 ns
3.	0 = 0	15 = 1.5	=	1.5 ns

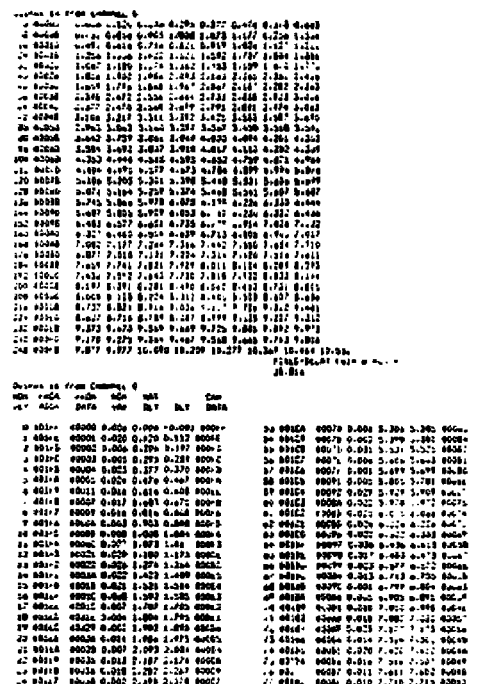

Fig. 1. PROM Programming

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In theory any of these programs should produce the requested delay. In practice we are looking for the best fit to the ideal requested value. In the example, that value would be 1.500 ns. Another requirement is that the value of the incremental delay increase monotonically as the requested delay is increased. To obtain the addresses for a best fit, a computer program was written that cycles through all possible delay address combinations, measures and records the delay, and address, and stores these values in RAM. The computer then looks for the best fit to the ideal curve. When it finds this best fit, it prints out the ideal value, address of the closest available delay, and does a second measurement of the delay and prints this value.

At the completion of this program, the printout will contain the delay addresses that will produce the most linear monotonically increasing delay. These delay addresses are stored in a PROM that is addressed by the software requested delay. The PROM is acting as a program director, insuring best fit of the requested delay.

The computer printout is shown in Fig. 1 for the programming of a specific PROM. Each of the units will have a unique PROM program. The upper portion of the printout lists the delay at each address. The lower portion shows how to program the PROM to get the best fit available.

The result of a final test of the module is shown in Fig. 2. The PROM has been programmed and the module is functional and ready for delivery. Fig. 3 is a system diagram, Fig. 4 is a VDU-1 channel block diagram and Fig. 5 is a schematic of the module.

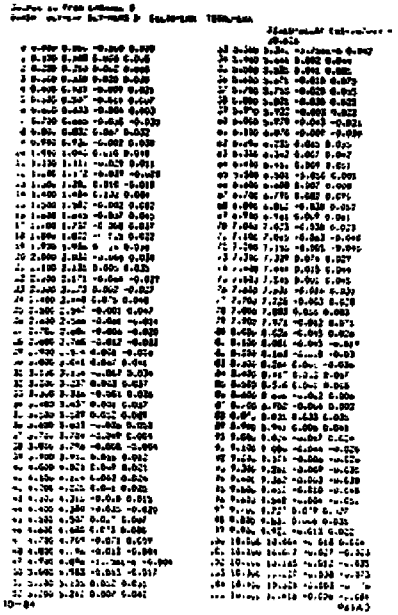

Fig. 2. Final Test Printout

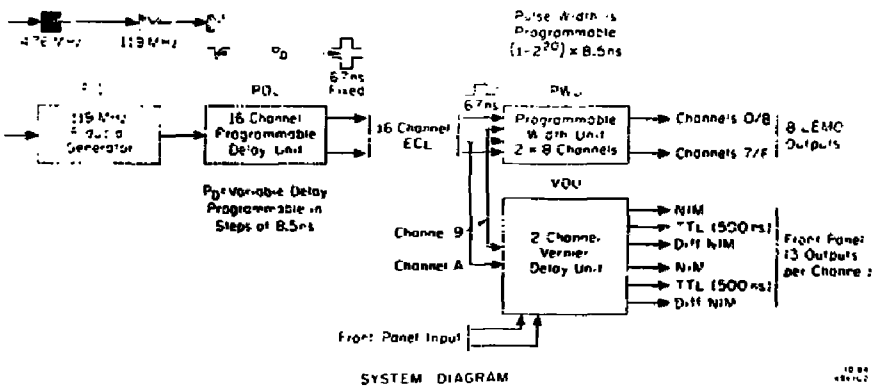

Fig. 3. System Diagram

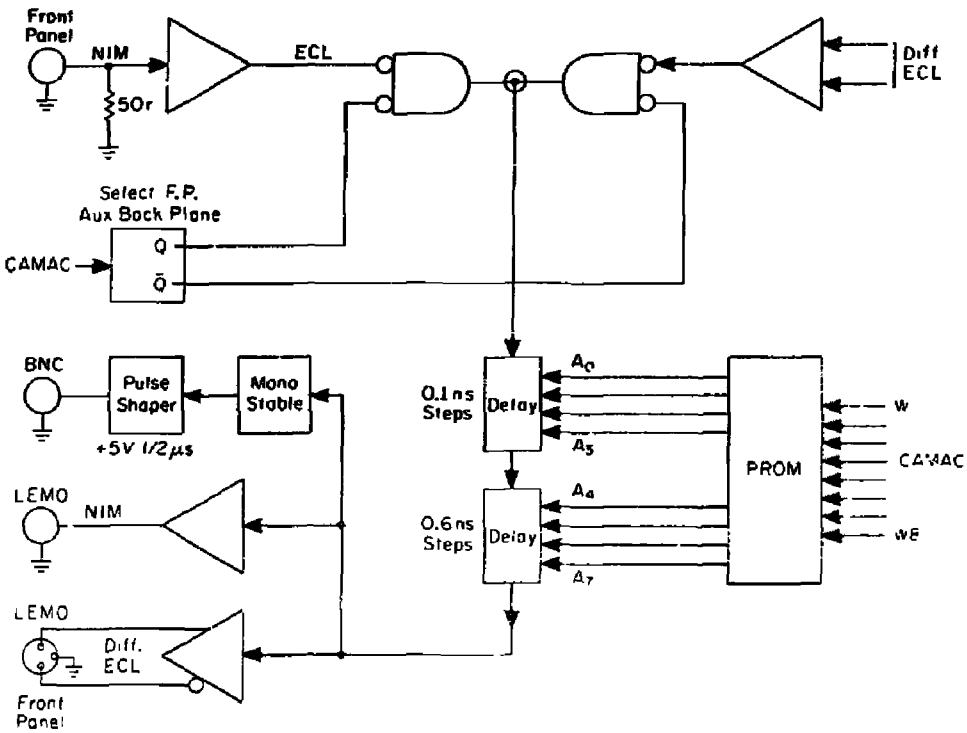

Fig. 4. VDU–1 Channel Block Diagram

The following discussion refers to Fig. 5 [Schematic Drawing DS-135-756-01-R2], and is an effort to describe the circuit function of the chips utilized. U14, U17 are ECL line receivers that present proper terminations to the driving circuits. U16 and U15 are ECL gates that ultimately determine which condition is selected, i.e., rear panel, front panel or channel disabled. U11 and U12 are the programmable TTL registers that dictate which condition the gates will be in. (*Again*: front/rear panel select or disable) U18, 19, 20, 21 are the ECL programmable delays. U19, 21 are programmable delays of 15 steps of 0.1 ns per step. U18, 20 are programmable in 15 steps of 0.6 ns per step.) U22, 24 are ECL line drivers that condition the output signal to the desired levels. U23 and U25 are ECL monostables that generate the fixed 500 ns output pulse width and Q4, Q5 and Q6, Q7 are discrete transistors that generate the +5 V amplitude of this 500 ns pulse. U1, U2 are latches that hold the requested delay that is on the CAMAC write lines. U7, U8 are PROMs that are programmed to get the optimum incremental delay response. U3, U4, U5 are TTL circuits used to read back the information as to what delay has been programmed into the circuit. U3 and U4 act as a multiplexer selecting between Ch1 and 0. U5 is the CAMAC READ line driver. U13 is the "1" light driver.

DISCLAIMER

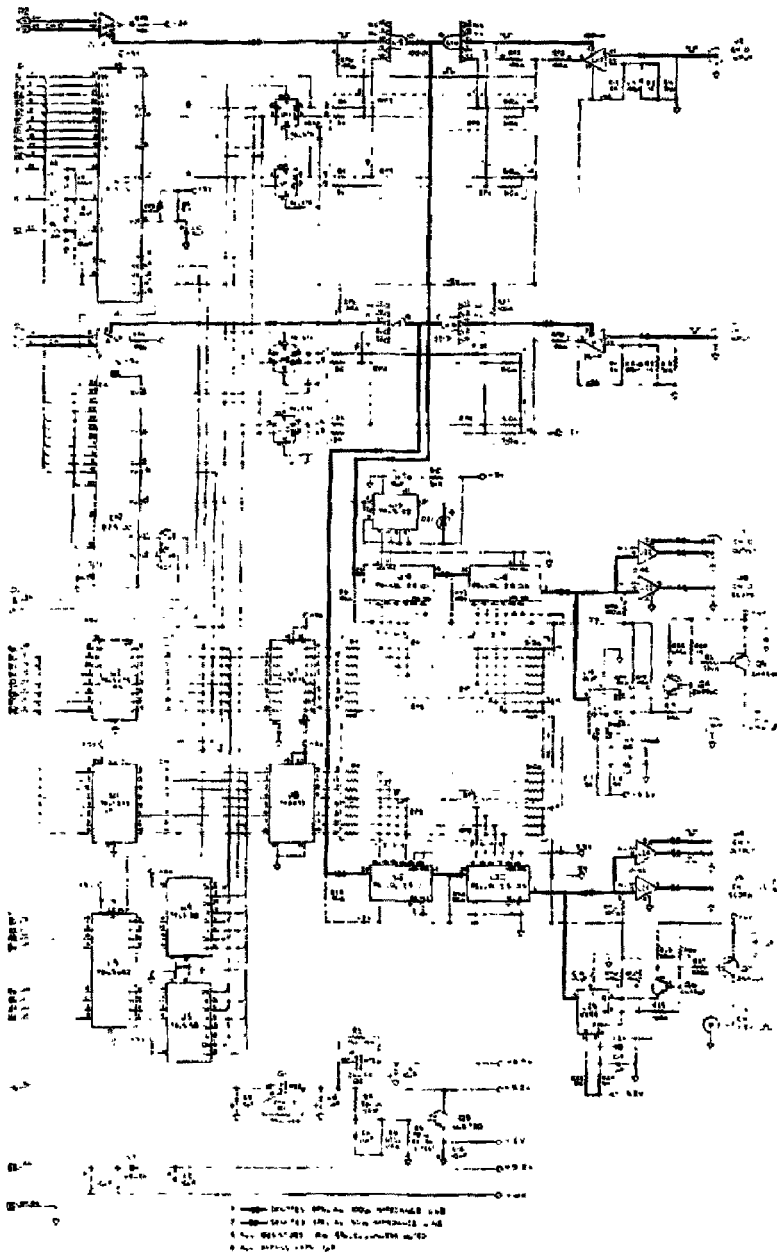

Fig. 5. Module Schematic

The VDU module is a single width CAMAC module. Figure 6 is a photo of the module.

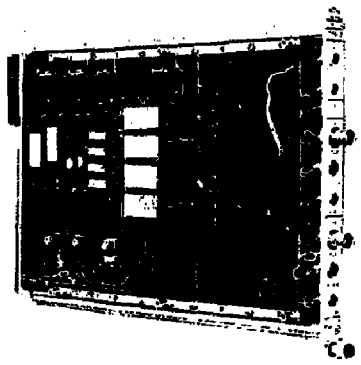

Fig. 6. VDU Module

The CAMAC commands utilized for this module are as follows:

CAMAC CODES

- Power On, F9•AX•S2, Z•S2 will disable all outputs and clear all channels.
- F0 A0/A1 : Read the contents of the delay register. Q=1 implies that the auxiliary backplane is selected AND channel (0/1) is enabled.
- F1 A0/A1 : Read the contents of the delay register. Q=1 implies that the front panel is selected AND channel (0-1) is enabled.
- F10 A0/A1 : Disable channel (0/1).
- F16 A0/A1 : WRITE W1-W7 into channel 0 or 1, in straight binary. This command also selects the auxiliary backplane, and enables the output.
- F17 A0/A1 : Same as F16 A(0/1) except that the inputs are selected from the front panel.
- F25 A0/A1 : Enable channel (0/1). Enable rear panel input.
- F26 A0/A1 : Enable channel (0/1). Enable front panel input.
- F27 A0/A1 : Q=1 implies that channel (0/1) is enabled.