LATCH-UP CONTROL IN CMOS INTEGRATED CIRCUITS*

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The potential for latch-up, a pnpn self-sustaining low impedance state, is inherent in standard bulk CMOS structures. Under normal bias, the parasitic SCR is in its blocking state, but if subjected to a high-voltage spike or if exposed to an ionizing environment, triggering may occur. This may result in device burn-out or loss of state. The problem has been extensively studied for space and weapons applications. Prevention of latch-up has been achieved by lifetime control methods such as gold doping or neutron irradiation and by modifying the structure with buried layers. Smaller, next-generation CMOS designs will enhance parasitic action making the problem a concern for other than military or space applications alone. This paper will survey latch-up control methods presently employed and indicate their adaptability to VLSI designs.

Gain Control Methods

Bulk CMOS integrated circuits have the cross-section shown in Figure 1. The indicated bipolar transistors are cross-coupled in a fashion capable of four-layer SCR action. Standard analysis[1] reveals latch-up is impossible if the β product is less than 1 ($\beta_{npn} \cdot \beta_{pnp} < 1$). Because current gain varies directly to first order[1,2] with lifetime, a generic solution is found in minority lifetime reduction. Au doping and high-energy neutron damage have been successfully employed for this purpose.[3,4] β products less than 1 have been obtained for a 9 μm p-well process with 5×10^{16} cm^{-3} surface concentration on a 1 Ω-cm substrate.

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[1]Sze, S. M., Physics of Semiconductor Devices, Wiley-Interscience, 1969.

[2]Grove, A., Physics and Technology of Semiconductor Devices, John Wiley & Sons, 1967.

[3]Dawes, W. R., Jr. and Derbenwick, G. F., "Prevention of CMOS Latch-up by Gold doping," IEEE Trans. on Nuclear Science, Vol. NS-23 6, pp. 2027-2030, December 1976.

[4]Adams, J. and Sokel, R., "Neutron Irradiation for the Prevention of Latch-up in MOS Integrated Circuits," this conference.

Reduction of the vertical npn's current gain can also be achieved by using a buried layer as shown in Figure 2. The current gain is reduced by increasing the Gummel number of the base and, at the same time, providing a retarding electric field near the emitter. Current gains for the vertical device of ~1 have been obtained.[5]

Holding Current and its Consequences

From the cross-section of Figure 1, it can be seen that the first-order SCR model has shunt base-emitter resistors, R_s and R_w, as shown in Figure 3. The holding current, I_H, can be obtained as a function of these shunt resistors and the transistor current gains,

$$I_H = \frac{I_{Rs}\,\beta_p\,(\beta_n + 1) + I_{Rw}\,\beta_n(\beta_p + 1)}{\beta_n\,\beta_p - 1} \qquad (1)$$

where I_H = holding current
I_{Rs} = current through shunt resistor R_s
I_{Rw} = current through shunt resistor R_w.

If the maximum available supply current is less than the holding current given above, latch-up is prevented. A simple epi-layer structure consisting of n on an n^+ substrate has been shown to prevent latch-up by decreasing R_s sufficiently so that a high-holding current results. Indeed, the holding current required by using a .001 Ω-cm substrate in Sandia's standard process exceeded the burn-out current, and device destruction was obtained and not latch-up. The buried layer structure of Figure 2 also will raise I_H.

It had been observed that a β product greater than one was required with the shunt resistors of Figure 3,[6] but this had not been quantified until recently. This statement, in view of Eq. (1), is true if modified as follows: If the available supply current is finite and equal to I_{DD}, the β product required for latch-up to occur is greater than one and given by

$$\beta_n \cdot \beta_p \geq \frac{I_{DD} + \beta_n I_{Rw}}{I_{DD} - I_{Rw} - I_{Rs}\left(\frac{\beta_n+1}{\beta_n}\right)} \qquad (2)$$

[5]Estreich, D., Ochoa, A., and Dutton, R., "An Analysis of Latch-up Prevention in CMOS ICs using an Epitaxial-Buried Layer Process," IEDM, p. 230-234, 1978.

[6]Barnes, C. E., et al., "Latch-up Prevention in CMOS," SAND76-0048, Sandia Laboratories, Albuquerque, NM, March 1976.

Thus operating a shunted structure with a current limited supply allows the β products to exceed unity and, since all supplies deliver only a finite current, a built-in safety margin is obtained for unity product designs.

Small Geometry Structures

VLSI technology is producing such high-gain vertical devices that latch-up has been observed initiated by microscope lights during device probe for functionality. If scaling design rules are followed, lower vertical βs are obtained as the Gummel number is increased. However, the gain due to the reduction of base width in the parasitic devices can exceed the loss due to the increased doping. VLSI designs will require further structure changes for latch-up control. Combinations of past methods and innovations will be required. The use of arsenic implants for the n channel source/drains with an incomplete anneal has been suggested to produce an inefficient injection emitter for the vertical npn.[7] Implants such that the p-well profile peaks beyond the source/drain depth, to parallel the buried layer structure also hold promise.

Summary

Latch-up control for 5-7 μm geometry is understood, reliable and readily available. Lifetime control produced by heavy metal doping or neutron irradiation results in latch-up free devices. Buried layers and epi-structures avoid latch-up by increasing the required β product, and by increasing the holding current beyond that available or beyond that which the device can withstand. These latter methods have appeal as they avoid the introduction of Au in the process and/or the cost and maintenance of a neutron source. The next-generation structures will enhance the problem significantly making it of concern to a wider audience. Solutions will almost certainly require tailored profiles and emitter efficiency reduction along with a combination of previous efforts.

[7]Dawes, W., private communication.

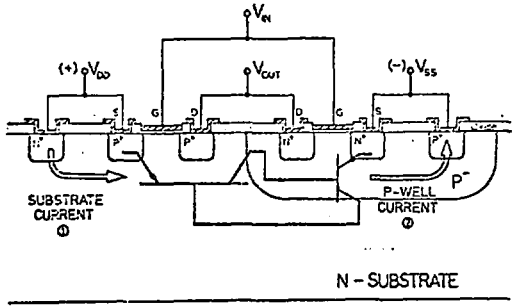

Figure 1. Standard bulk CMOS cross-section showing parasitic bipolar devices involved in SCR action.

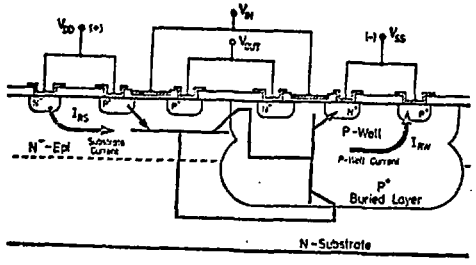

Figure 2. Cross-section of epi-buried-layer structure showing parasitic bipolar devices.

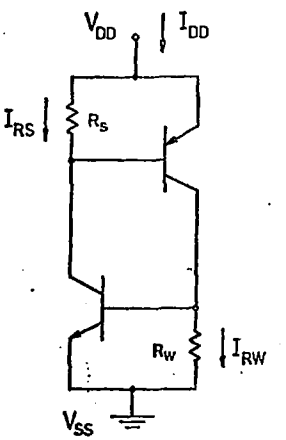

Figure 3. First-order equivalent circuit of the pnpn latch-up path in a bulk CMOS structure.