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What's New with FASTBUS and What's it Done in the Particle Accelerator Laboratories[1]

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Abstract

The FASTBUS modular high-speed data acquisition and control system has been described in earlier papers [1,2]. Implementations have since been made in accelerator laboratories world-wide resulting in clarifications, modifications and extensions. Of tremendous benefit to users have been FASTBUS Standard Routines. The availability of such standard software is unique for high speed bus systems and resulted from the involvement of hardware and software specialists in all aspects of the development. FASTBUS is the highest performance instrumentation and data acquisition bus in existence and its development was essential to handle the outputs of detectors used with high energy accelerators now in operation. It has been an important factor in recent experiments, including the Z^0 measurements at CERN, Fermilab and SLAC. Also among numerous FASTBUS implementations are those for TPC systems at KEK and BNL.

I. INTRODUCTION

The initial version of FASTBUS was published as U.S. Department of Energy Report DOE/ER-0189 in 1983. Later, with some modifications, it was issued as a standard of the Institute of Electrical and Electrical Engineers (IEEE) and the American National Standards Institute (ANSI) as ANSI/IEEE Std 960-1986, "FASTBUS Modular High-Speed Data Acquisition and Control System." As experience was gained in the laboratories with the system, additional modifications were instituted and the ANSI/IEEE standard reissued in 1989. The supplementary software document, "FASTBUS Standard Routines," was initially issued in 1987 as Department of Energy Report DOE/ER-0325. It was revised and reissued the following year as DOE/ER-0367 and, with clarifications and minor additions, was published as ANSI/IEEE Std 1177-1989. FASTBUS has also been adopted as an international standard by the International Electrotechnical Commission (IEC) as IEC Publication 935-1990 and the FASTBUS Standard Routines as IEC Publication 1073-1991. FASTBUS Newsletters are distributed to a large mailing list of users and producers alerting them as to any additional modifications, extensions or clarifications found to be desirable.

II. SOME LABORATORY IMPLEMENTATIONS

FASTBUS has been an important factor in recent successful experiments, including the Z^0 measurements at CERN, Fermilab and SLAC. It has also been utilized in many other experimental programs in numerous major laboratories worldwide. Several hundred FASTBUS Module designs have been registered and an estimated 20,000-30,000 FASTBUS Modules produced and placed in service. Installations at a few of the laboratories are described briefly below.

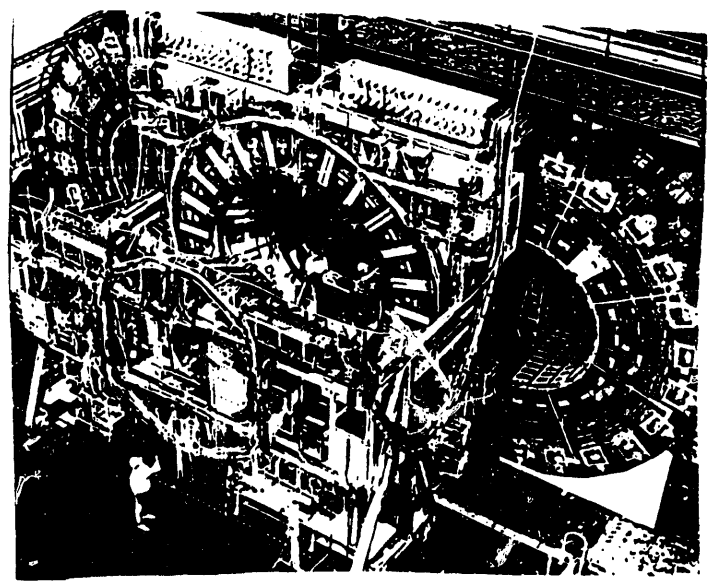

Fig. 1. Fermilab Collider Detector

[1]Work supported by U.S. Department of Energy.

Brookhaven National Laboratory (BNL)

Probably the first FASTBUS system ever used in high energy physics was that installed at the Multi-Particle Spectrometer (MPS) by BNL in 1980. (Since the system was then in the early stages of development, some of the device dimensions are not in accordance with the current specifications.) There are now five on-going AGS experiments as listed below utilizing FASTBUS at BNL.

E810 - A search for quark matter (QGP) and other new phenomena utilizing heavy collisions. This is an ion experiment using time projection chambers in the MPS to explore strangeness production with large acceptance.

E814 - The study of peripheral collisions and the transition from peripheral to central collisions using relativistic heavy ions. This experiment uses calorimetry and a small solid angle spectrometer.

E859 - Studies of particle production at extreme baryon densities in nuclear collisions. Uses a movable spectrometer with particle identification.

E787 - A study of the decay of K plus into pion plus, neutrino, antineutrino. This is a rare K decay experiment using the AGS as a proton accelerator.

E850 EVA - A solenoidal detector for large angle exclusive reactions: Phase I - Determining color transparency at 22 GEV/c.

Los Alamos National Laboratory (LANL)

At LANL there are two organizations currently using FASTBUS for data acquisition in physics experiments. Both use the 800-MeV proton beam from the Los Alamos Meson Physics Facility (LAMPF).

The MEGA experiment is a nuclear physics measurement that will attempt to measure the branching ratio (not yet observed) for the decay of the muon to an electron and a gamma-ray with a sensitivity of about 10^{-13}. There are nine crates of FASTBUS, interconnected with FASTBUS Segment Extenders and Segment Interconnects. The detector includes approximately 12000 analog and digital channels. A hardware trigger strobes event data from the front-end electronics into more than 150 multiple-event buffered FASTBUS ADCs, TDCs, and latches. A single event is expected to be about 1400 bytes long. About 20 events will be acquired during each LAMPF 500 microsecond beam spill. At the end of the beam spill all data is moved into a set of high performance work stations for further processing and event filtering. This transfer must occur in the 8 millisecond interval between beam spills. The average data rate is about 3.3 Mbytes/second and about 14 Mbytes/second peak.

The Los Alamos Neutron Scattering Center (LANSCE) engages in a wide spectrum of condensed matter measurements. There are eight single-crate experiments, each relying on the measurement of the time interval between the arrival of the pulsed proton beam from LAMPF at the LANSCE spallation target and the subsequent arrival of the secondary neutrons at the detector in the instrument. Position information is derived and together with the time of each event, is listed in a memory buffer until all events for a single burst of protons at the target are recorded. Processing then begins such that each event is translated to a channel number and the contents incremented to form a large histogram. Processing to this point is accomplished within the FASTBUS environment.

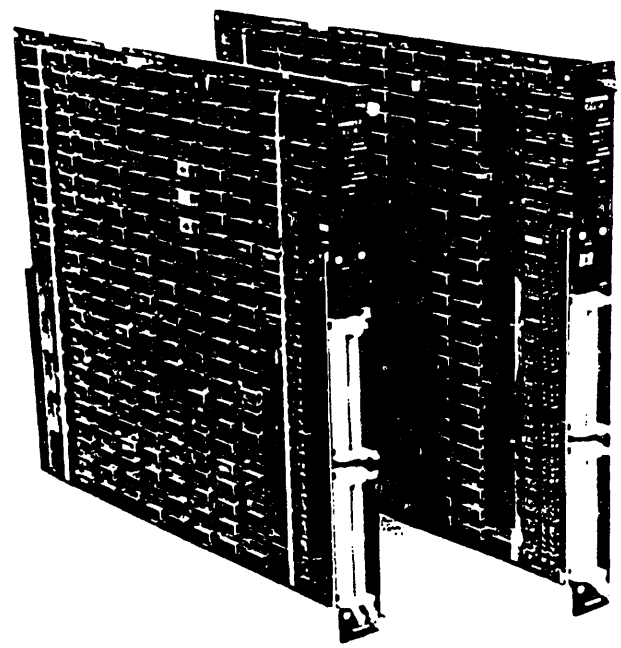

Fig. 2. Typical FASTBUS Modules

European Center for Nuclear Research (CERN)

At CERN the first experiments exploiting FASTBUS included UA2, the study of pbarb interactions at the proton-antiproton collider, and NA31, a fixed target experiment studying CP violation. These early experiments were essentially CAMAC oriented and the role of FASTBUS was to improve performance in dedicated areas. Although UA2 had a relatively small system of 14 Crates, the operational requirements were such that 15 Aleph Event Builders were employed, distributed through four Cable Segment networks. The

concept of pairs of Crates clustered to optimize data flow and processing power proved to be both effective and economical.

In three of the current enormous LEP experiments FASTBUS was adopted almost exclusively for front-end electronics, trigger logic and data acquisition. The fourth, OPAL, applies FASTBUS only to the readout of the central detector. Well over 400 Crates of FASTBUS electronics have been installed in the four experiments. Both the LEP machine and these experiments are now being upgraded; many more years of success are anticipated.

New experiments planning to use FASTBUS are currently at the specification, setting up, and test phases. An example is that of PS195, CPLEAR, at the Low Energy Antiproton Ring (LEAR) facility. An experiment where installation of the electronics, including about 50 Crates of FASTBUS, is scheduled for completion in 1991.

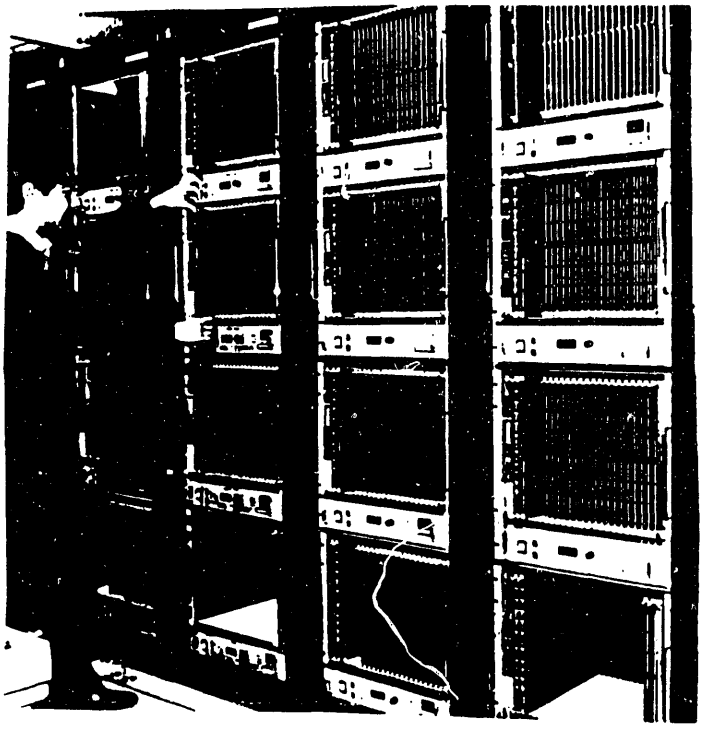

Fig. 3. CERN FASTBUS Racks

Fermi National Accelerator Laboratory (FNAL)

At the Fermilab a number of Collider Detector Facility (CDF) experiments as well as fixed target experiments have used or are using FASTBUS. These include approximately 1500 modules in over 150 Crates. These include the equipment for the "in development" silicon strip readout system for E771 that will use FASTBUS Smart Crate Controllers daisy-chained together to read data from FASTBUS crates and transfer the data via VME buffers to an on-line VME processor array.

Japan National Laboratory for High Energy Physics (KEK)

The electron-positron colliding beam detector, TRISTAN, at KEK was constructed in pace with the development of the FASTBUS system. This simultaneous development was an important factor in the role that FASTBUS played in the successful operation of the TOPAZ Time Projection (TPC) system. In the VENUS drift chamber experiment the FASTBUS data acquisition system has been in operation since the first collision in November of 1986 at the TRISTAN accelerator.

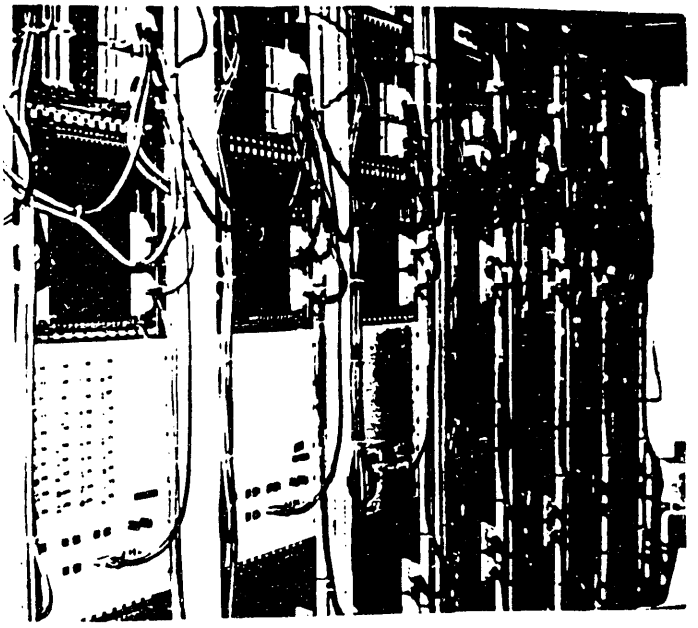

Fig. 4. FASTBUS Installation at KEK

Dubna Joint Institute for Nuclear Research (JINR)

At the Laboratory of High Energies, JINR, in Dubna, U.S.S.R., a FASTBUS system has been developed to measure time intervals and fast analog signals for the 4π-geometry spectrometer for heavy ion research. The system provides communication between a FASTBUS Segment and an IBM PC. To date eight module designs have been completed and a readout processor is being developed with data transfer rates of up to 30 Mbytes per second.

Stanford Linear Accelerator Center (SLAC)

At the Stanford Linear Accelerator Center two detector facilities are equipped with data acquisition systems utilizing FASTBUS. In November 1990 an experiment involving the Mark 2 Detector was completed that explored the Z^0

resonance utilizing electron-positron colliding beams with a center-of-mass energy of approximately 92 GeV from the Stanford Linear Collider (SLC). Its data acquisition hardware consists of CAMAC and FASTBUS subsystems with the FASTBUS subsystems containing 27 Crate Segments and 6 Cable Segments. System architecture is based on the SLAC Scanner Processor Modules as master system controllers, event builders, intelligent crate controllers and local data processors, and Cable Segment interconnects.

Installation of the new Stanford Large Detector (SLD) was completed in May 1991. It replaces the Mark 2 as the detector at SLC to study Z^0 physics. This detector is undergoing colliding beam checkout in preparation for obtaining physics data in late 1991. A data acquisition system for approximately 180,000 analog and digital data channels has been implemented with 18 FASTBUS Crate Segments.

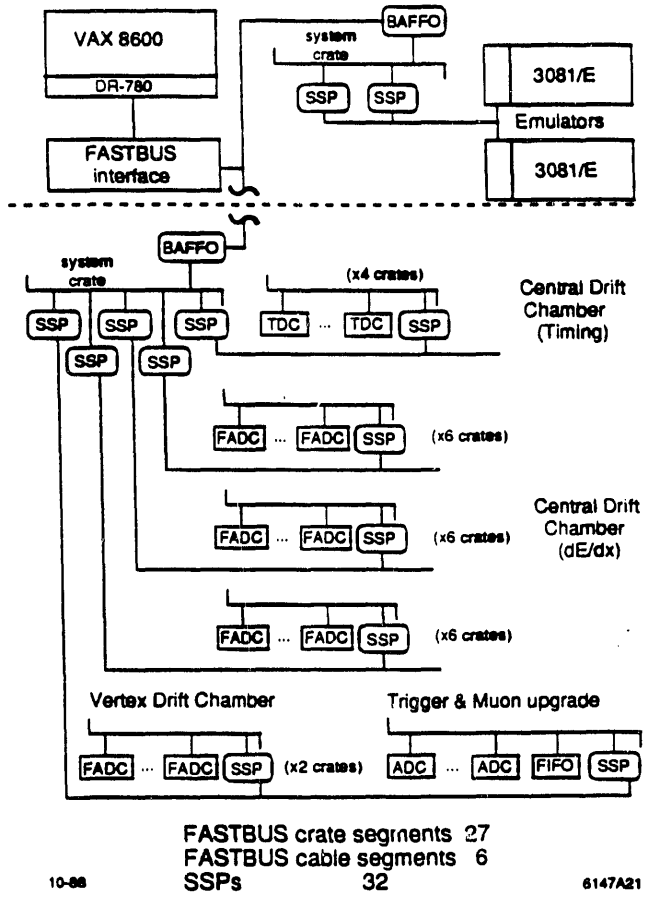

Fig. 5. FASTBUS System used with SLAC Mark 2 Detector

III. DESIGN CHANGES

Recent developments in the FASTBUS program include the issuance of the IEEE and IEC FASTBUS and Standard Routines documents identified in the Introduction section of this paper as well as the 4 December 1990 addenda and errata distributed to the FASTBUS mailing list with the NIM/FASTBUS Newsletter of the same date.[2] The principal changes presented in the 4 December 1990 A&E are:

Clarification of the Broadcast operation, including the addition of state diagrams.

Addition of CSR Registers 18 and 19 to be used, as appropriate, instead of CSR#5 because of ambiguity that had existed with regard to CSR#5 as a Word Count register.

Clarification of the NIM standard logic levels to correspond to the levels given in the latest issue of the "Standard NIM Instrumentation System," DOE/ER-0457T dated May 1990.

Attention is also directed to the modifications in the Mode Select (MS) codes that occurred earlier and are included in the 1989 specification, ANSI/IEEE Std 960-1989.

Though the 10114 receiver currently in use is satisfactory when loaded with a limited number of connected devices, alternatives are desirable for systems in which a large number of devices are connected to a single Cable Segment. A five-channel differential transceiver (CSX-E), based on device specifications developed at SLAC, has been designed for that purpose. It is being implemented as a full-custom integrated circuit. Besides providing superior performance, it is intended to reduce the cost of the necessary interface. Additionally, work is underway on pin-compatible retrofits for the 10114, including an assembly of three TL721's that has proved to be suitable, though slower than the 10114. Performance and availability information can be expected in January or February 1992.

IV. COST

A study of the economics of bus systems with a large number of channels was made by CERN and gives comparative costs of a component in FASTBUS of $4.50, VME $7.50., and CAMAC $9.00. More than 90% of front-end module board area is available for user electronics and, making allowances for Masters, Interconnects and Interfaces, only 20% of the total system space is lost to the user. These real estate figures are a component in the cost comparisons.

[2]To be added to the NIM/FASTBUS mailing list or to obtain copies of the Newsletter, write to Louis Costrell, Chairman NIM Committee, National Institute of Standards and Technology, Gaithersburg, Maryland 20899.

V. SPIN-OFFS TO OTHER SYSTEMS

FASTBUS has made contributions to the design of several other industry standard busses. The FASTBUS arbitration scheme was adapted to the S-100 bus by the IEEE 696 working group and subsequently adopted, with variations (particularly in the timing control) by IEEE 896 (Futurebus), IEEE 1196 (NuBus), and IEEE 1296 (Multibus-II).

The FASTBUS data transfer protocols were used as a starting point by IEEE 896 (Futurebus), which modified them to support cache coherence, distributed control of broadcast timing, and skew-free block transfers. FASTBUS was also a leading influence with its concepts of "no DIP switches or jumpers," Geographic Addressing, standard Control and Status Register architecture, and a serial diagnostic network.

The contemporary development of these other standard busses also benefitted FASTBUS, which for example added an arbitration fairness mechanism ("assured access" protocol) as a result of Futurebus influence.

VI. REFERENCES

[1] L. Costrell and W.K. Dawson, FASTBUS For Data Acquisition and Control, IEEE Trans on Nucl. Sci. NS-30, No. 4, Aug. 1983. (A brief and simple description).

[2] W.K. Dawson, L. Costrell, Hirokazu Ikeda, P.J. Ponting, and H.V. Walz, FASTBUS for the Particle Accelerator Laboratories, IEEE Trans. Nucl. Sci. NS-32, No. 5, October 1985, p. 2089-2091.

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