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THE DATA ACQUISITION SYSTEM FOR SLD*

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ABSTRACT

This paper describes the data acquisition system planned for the SLD detector, which is being constructed for use with the SLAC Linear Collider (SLC). Analog electronics, heavily incorporating hybrid and custom VLSI circuitry, is mounted on the detector itself. Extensive use is made of multiplexing through optical fibers to a FASTBUS readout system. The low repetition rate of the SLC allows a relatively simple software-based trigger. Hardware and software processors within the acquisition modules are used to reduce the large volume of data per event and to calibrate the electronics. A farm of microprocessors is used for full reconstruction of a sample of events prior to transmission to the host.

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1. INTRODUCTION

The SLD[1] is a large solenoidal detector being constructed for use with the SLAC Linear Collider (SLC), and is expected to begin operation in 1989. The detector will be used to study e^+e^- collisions at energies up to 100 GeV, and is being designed to give 97% of full solid angle coverage with good tracking resolution, particle identification, and electromagnetic and hadronic calorimetry. A schematic cross section of one quadrant of the detector is shown in Fig. 1. The principal elements of the detector include:

- A vertex detector at a radius of 1–3 cm from the beam, consisting of 260 CCD chips, and a total of 58 million pixels with 22 μm spacing.
- A drift chamber system with approximately 8000 wires and an azimuthal resolution of less than 100 μm. Third coordinate readout is obtained using charge division and 50 mrad stereo.
- A Čerenkov Ring Imaging Detector (CRID) with both gas and liquid radiators. The axial coordinate of converted photons is obtained from the drift time of the photoelectrons to an array of proportional wires at the ends of the detector; the radial coordinate is determined using charge division on the highly resistive carbon filament wires; the azimuthal coordinate is determined by which of the approximately 12,000 wires detected the electron.
- A lead-liquid argon calorimeter with two electromagnetic and two hadronic sections arranged in projective towers, containing a total of approximately 45,000 channels.
- An iron calorimeter used to supplement the 3-interaction-length liquid argon calorimeter, and to identify muons. The iron calorimeter uses streamer tubes with approximately 10,000 channels of pad analog readouts, and 100,000 channels of strip digital readouts.
- A tungsten calorimeter containing 1280 channels of silicon detector readout at small polar angles for luminosity measurement.

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The data acquisition system exploits the low 180 Hz repetition rate of the SLC. During the synchronous 5.6 msec between beam crossings, data from the calorimeter and drift chambers are used by a programmable processor in the FASTBUS system to reject or accept the beam crossing as an event, reducing the trigger rate from 180 Hz to an anticipated 1–2 Hz. This low trigger rate then allows approximately 50 msec for readout of the full detector system by the FASTBUS acquisition modules, producing a deadtime of less than 10%. The long readout time, in turn, allows a high degree of multiplexing in the readout system, thus minimizing both the cable plant and the number of acquisition modules required in the FASTBUS system.

2. System Architecture

With minor variations, the electronics for each of the subsystems of SLD share the following common approach:

- For each beam crossing, analog signals from the detector are stored in electronics mounted on the detector itself. Analog outputs from these circuits are multiplexed together in large groups of channels onto optical fibers to the FASTBUS system. While this approach[2] presents potential problems in space management, power dissipaton, and accessibility, it minimizes an otherwise massive cable plant with its associated problems of space management and reliability, and significantly reduces the required electronics in the FASTBUS system. Throughout the detector electronics heavy reliance is placed upon custom integrated circuits and hybrid packaging techniques.
- Fiber optic receiver boards mounted on the auxiliary backplane of the FASTBUS acquisition crates receive and digitize the analog signals.
- The FASTBUS acquisition modules perform a first stage of hardware processing, typically involving the application of calibration constants and a first stage of compaction of the digitized data. Table 1A summarizes the hardware processing of a typical event. For each subsystem the first column shows the volume of data per event which is digitized; the second

column shows the number of calibration constants which must be maintained; the third column shows the volume of compacted data output to the software processors.

- The FASTBUS acquisition modules also contain Motorola 68020 microprocessors which perform a second stage of data reduction, and are also used heavily in the calibration of the system. Table 1B summarizes the software processing power and data compaction functions for a typical event. For each subsystem the first column shows the total processing power available in millions of instructions per second (MIPS); the second column shows the number of instructions available per word of input data for an average trigger rate of 2 Hz; the third column shows the resulting volume of further compacted data after software processing.
- Each of the subsystems includes a single FASTBUS ALEPH Event Builder,[3] which serves as overall coordinator and the only FASTBUS master for the subsystem.

The FASTBUS acquisition system is shown schematically in Fig. 2. The lowest level contains the data acquisition modules briefly described above and which will be described in more detail in the following sections. The second level contains the trigger system, which will be discussed in section 7. As will be discussed in section 8, the third level contains a "farm" of approximately twelve FASTBUS MicroVAX processors[4] used to tag events of interest and to perform full reconstruction of a fraction of the events.

3. VERTEX DETECTOR

A block diagram of the vertex detector electronics is shown in Fig. 3. Analog data storage is intrinsic to the CCD detector itself, which consists of 260 CCD chips arranged in two concentric cylinders about the beam. Thus, in addition to the chips themselves, only preamplifiers are required on the detector itself.

The vertex detector is read out only for triggered events. Each of the CCD chips, containing 385 × 578 pixels, is read as a separate serial stream using

conventional wire cabling. Data are clocked out of the CCDs at a rate of 1 pixel per 200 nsec onto an integrating capacitor, resulting in a total readout time of 45 msec. A flash ADC samples the capacitor voltage 4 times per pixel at 20 nsec intervals for signal averaging, and subtracts the resulting sum from that of the previous pixel to remove the integration effect of the capacitor. These digitized signals are passed to a module which, working on several rows of data in a fast memory, applies thresholds and defines clusters of hit pixels. Addresses and pulse heights for these pixels are saved in memory for processing by the microprocessor.

The CCD chips have been used successfully in an experiment at CERN[5], and the front-end timing and preamplifiers for SLD have been designed and tested. The design of the FASTBUS modules is only beginning.

4. WAVEFORM SAMPLING SYSTEMS

A. DETECTOR ELECTRONICS

A block diagram of the drift chamber electronics is shown in Fig. 4. Both the drift chamber and Čerenkov systems use drift time and charge division of hit wires to provide three coordinate readout. To combine the functions of time digitization and charge integration, and to maintain multihit resolution, the full waveform over the maximum drift time is stored in Analog Memory Units (AMU).[6] These custom VLSI integrated circuits contain 256 sample and hold circuits, with noise performance corresponding to an eleven-bit dynamic range, and associated input and output multiplexing to allow input sampling at rates up to 200 MHz and analog readout at a rate of 700 KHz. Data from a single preamplifier are interleaved onto two AMUs to provide a total of 512 samples ("time buckets") per channel. 16 AMU chips are packaged together with associated clocking logic on a single hybrid circuit.

The AMU chips have been tested and their full production is complete. The hybrid design is complete and samples are currently under test. Fig. 5 shows

waveform data (after calibration) obtained in a test beam using a a prototype drift chamber and a prototype AMU hybrid packaged in a CAMAC module[7].

In addition to the AMUs, the drift chamber signals are passed through an analog comparator to a serial shift-register latch implemented in a gate array. This information can be read out between beam crossings and is used in forming the trigger decision, whereas the AMUs are read out only for triggered events.

Eight channels of drift chamber preamplifiers, comparator-latches and pulse calibration circuitry are packaged in a second hybrid circuit. The design of this hybrid is complete and samples are currently being tested. A similar system without latches and using different preamplifiers for the CRID system is currently being designed.

To minimize power dissipation, power to the preamplifiers and input AMU section is pulsed during each beam crossing to provide a duty cycle of less than 10%. Power to the output section of the AMU is applied only during event readout. During event readout eight AMU hybrids (64 wires, 128 AMUs, 32,768 time buckets) are multiplexed onto an analog optical fiber at 1.6 μsec per time bucket. This results in a total readout time of 52 msec.

B. FIBER-OPTIC RECEIVER BOARD

A fiber optic receiver board[8] mounted on the FASTBUS auxiliary backplane receives analog data from eight optical fibers. The multiplexed analog data from the AMU system are digitized by a sample and hold circuit followed by a twelve-bit ADC. Data from opposite ends of each wire are brought out on two separate optical fibers to the same receiver board. To provide for common processing of the two wire ends, as well as to provide further multiplexing, data from corresponding fibers are interlaced to a single holding register on the receiver board. Thus the output data rate is doubled and the number of output channels is halved. The receiver board has been designed and sample boards currently being tested.

C. WAVEFORM SAMPLING MODULE (WSM)

The four output channels of the receiver board go to a four-channel FASTBUS Waveform Sampling Module, shown schematically in Fig. 6. The high degree of multiplexing employed allows the drift chamber system to be contained in two FASTBUS crates, and the Čerenkov system to be contained in three. The principal elements of the WSM consist of a Digital Correction Unit (DCU), which applies calibration constants and zero-supresses the data, and a microprocessor used to extract leading edge times and charge integrals from the waveform data. The design of the WSM is complete, and prototype modules are currently being fabricated.

1. Digital Correction Unit (DCU)

The DCU,[8] used by both the waveform sampling and calorimetry systems, is a custom integrated circuit used for both the application of calibration constants and initial compaction of either waveform or calorimeter data. A block diagram of the DCU is shown in Fig. 7.

In order to utilize the intrinsic eleven-bit resolution of the AMUs, each of the individual sample and hold circuits in the AMUs must be calibrated, including corrections for nonlinearity. The correction scheme adopted is to store a five- or nine-point calibration curve for each time bucket of each channel in a large calibration memory. The most significant bits of the ADC reading are used to select the appropriate two points, or segment, of the calibration curve. The DCU then uses the least significant bits of the ADC reading to perform a linear interpolation between the two calibration points.

A second stage of the DCU, used only for waveform processing, employs threshold logic to supress empty channel data (*i.e.*, data with nominally zero value), as shown in Fig. 7b. This logic uses a look-ahead FIFO to transmit several additional samples before a leading threshold is crossed, and a count-down register to transmit several samples after a trailing threshold is crossed.

Thus, thresholds need not be set perilously close to the noise level. The zero-suppressed data are written to a shared memory for further processing by the microprocessor.

The DCU design is complete, and samples have been obtained for testing.

2. Software Processing

The 68020 microprocessor is used to further reduce the waveform data. The volume of data per event and the cpu power required to reduce the data, particularly in a multihit environment, are prohibitively large for handling by higher level processors, even with zero-supressed data. The primary task of the microprocessor is therefore to reduce the waveform data to leading-edge times and integrated charges. The microprocessors have sufficient data memory to buffer several events, so that this function can be performed asynchronously with close to unity duty cycle without introducing deadtime beyond the 50 msec required to read out the AMUs.

5. CALORIMETRY SYSTEM

A. DETECTOR ELECTRONICS

The electronics for the calorimetry system, consisting of the liquid argon calorimeter, the iron calorimeter pad readout, and the luminosity monitor is shown schematically in Fig. 8. The calorimetry system measures integrated charge, and full waveform sampling is unnecessary. Consequently, a slightly different analog storage device, the Calorimetry Data Unit (CDU)[10] is used. The CDU contains 128 sample and hold circuits, and is arranged to allow 32 separate input channels, each with four time buckets. SLD will use only two of the time buckets, one to sample the baseline and one to sample the peak of the integrated signal. To accurately cover the full dynamic range required, each channel is sent to two inputs of the CDU, once with unity gain and once with a gain of eight. The required postamplifiers are packaged together with a single CDU on a hybrid chip. A second hybrid circuit is used to package eight channels of

pulse calibration circuitry and preamplifiers. An average of twelve CDU hybrids (192 calorimeter channels, 768 samples) are multiplexed onto one optical fiber, giving a total readout time of 1.2 msec. The short readout time is required because the calorimeter is fully read out for every beam crossing and used in the trigger. As with the waveform sampling systems, power to the preamplifiers is pulsed to minimize power dissipation.

The CDU chips have been tested and their full production is complete. The hybrid design is complete and samples are currently under test.[11]

B. THE CALORIMETRY DATA MODULE (CDM)

The digitization of the calorimetry data is handled in a fashion very similar to that of the waveform data. The fiber-optic receiver boards are identical to those used in the waveform system, and the FASTBUS CDM also incorporates four channels of DCUs and microprocessors. The acquisition modules for the full calorimetry system are expected to fit in two FASTBUS crates.

Because the receiver module interlaces the data from pairs of fibers which, in the calorimetry case, are not related, demultiplexing logic is placed on the CDM before the DCU. This logic maintains the single serial stream of data, but reorders it to keep data from a single CDU sequential.

The same linearity correction (using a seventeen-point calibration curve) is made in the DCU as for the WSM. However, a separate "personality" section of the DCU is used to compact the data. As previously discussed, for each channel of the calorimeter four samples are made: a baseline measurement and a peak measurement for each of two gains. For calorimetry data, the DCU performs the gain selection and baseline subtraction, thus reducing the volume of data by a factor of four. Because the look-ahead feature used by the WSM is more difficult to apply in three dimensions, and because the quantity of data digitized is smaller, supression of empty channels is not done by the DCU but instead is handled by the microprocessor.

In contrast to the WSMs, the CDMs participate in the trigger. For each beam crossing, the compacted data from the DCUs are directly read by the CDM microprocessors, and used to form a set of "super-tower" energy sums. These data are stored in the FASTBUS accessable processor memory for readout by the trigger processor. For triggered events, the CDM processor further forms a bit map of channels above threshold. Bit maps from each of the CDM processors are read, combined across CDMs, and slightly expanded by the subsystem Event Builder (see below), in order to perform the supression of empty channel data. The Event Builder may then selectively read the fully digitized data from the CDMs.

The CDM has not yet been designed, but is expected to follow as a modification of the WSM design.

6. IRON CALORIMETER STRIP READOUT

The electronics for the iron calorimeter streamer tube strip readout is shown in Fig. 9. Signals from the strips are stored digitally on the detector using a system consisting of preamplifier, discriminator, and shift-register latch for each channel. Four channels of discriminator—latches latches are packaged in a custom VLSI chip[12]. These chips also provide a fast output signal which is used to form a cosmic ray trigger. Eight channels of preamplifiers and discriminator - latches are packaged in a single hybrid. Approximately 200 channels are serially transferred to an intermediate board, where they are further multiplexed onto an optical fiber in groups of approximately 3500 channels. The intermediate board provides for the fanout of timing signals, and also contains switching logic to allow the individual groups of 200 channels to be bypassed in case of a failure in the serial readout. Data are clocked out at 1.6 MHz, resulting a total readout time of 2.2 msec.

Supression of empty channel data is performed by the microprocessor in the FASTBUS acquisition module as the data are read in. Four FASTBUS modules are used for the system. Design of the acquisition modules is complete.

7. EVENT TRIGGER

The principal elements of the trigger system (see Fig. 2), operating at the 180 Hz beam crossing rate, include:

- The Trigger Processor (TP) serves as intelligent master for the trigger system. An ALEPH Event Builder,[3] containing a Motorola 68020 processor, is used for this purpose. On the basis of drift chamber hit wire data and calorimeter energy data, the trigger processor decides whether or not stored beam crossing data should be fully read out as an event. The trigger processor is further responsible for the coordination of timing signals to the storage elements in the detector electronics and the acquisition modules.
- A set of Timing and Control Modules (TCM), controlled by the trigger processor, is used to provide timing signals to the detector electronics and to the acquisition modules. All timing signals are derived from a 119 Mhz clock which, in turn, is derived from the 2856 MHz rf frequency of the accelerator. A variety of pulse trains may be programmably generated, and, on a pulse to pulse basis, may be transmitted or inhibited by the trigger processor. In addition to the timing signals, all control signals to the detector electronics are sent from the TCM. Both timing and control signals are encoded onto a minimum number of fiber optic cables. The TCM is in a preliminary stage of design.
- The Drift Chamber Trigger Module (DCTM) performs the serial readout of the latched 1 bit per wire drift chamber data. These data are read out at 10 MHz, on 8 optical fibers, requiring 200 μsec for complete transmission. The DCTM combines the signals from the two ends of the drift chamber wires, and further combines the eight wires per drift chamber cell using programmable pattern matching. The total amount of drift chamber trigger information is thus reduced from approximately 12,000 to 1,000 bits. A list of hit cells is stored and read by the trigger processor. Using table driven pattern matching techniques, the trigger processor searches for tracks in

the detector. This process requires less than 1 msec. The design of the DCTM is complete.

In parallel with the readout and analysis of the DCTM data, the CDMs read the calorimeter data and form the supertower energy subsums. Upon completion of the calorimeter readout (1.2 msec after beam crossing), the supertower energies are read by the trigger processor, combined across CDMs, and, in conjunction with the track information, used to make the trigger decision within approximately 3 msec after the beam crossing. If the trigger decision is negative, the vertex CCDs must be cleared before the next beam crossing; the other detector systems need no resets. If the trigger decision is positive, the beam is supressed (because the vertex detector is continuously "live"), and the full readout of the vertex detector, the waveform sampling systems, and the iron calorimeter strips is initiated.

8. Higher Level Processing

Each of the subsystems includes a single FASTBUS ALEPH Event Builder (AEB),[3] which serves as overall coordinator and the only FASTBUS master for the subsystem. For event readout (but not for trigger functions) the subsystem AEB acts as an intermediary for communication between the trigger processor and the acquisition modules as well as for communication with the MicroVAX farm. The AEBs are responsible for the readout and formatting of data from the acquisition modules, and, to the extent possible, further processing of the subsystem data (*e.g.*, cluster finding in the calorimeter system). Overall coordination of the subsystem during calibration is also controlled by the AEB.

For each event a single MicroVAX is selected which reads the data from all of the AEBs to form a fully assembled event. The AEBs are read out through their slave port to a FASTBUS cable segment (see Fig. 2), thus minimizing FASTBUS contention between the trigger and the event readout.

The MicroVAX is first used to filter and tag physics events from the predominantly background triggers. At least initially all triggers reaching this stage of

processing will be passed to the host processor for logging. Hence the function here is not to reject triggers, but simply to tag physics event candidates for both online and offline analysis, without losing the ability to recover events if the filtering algorithms change. For a fraction of the physics events, a full reconstruction will be performed before the data are passed to the host.

9. SYSTEM CALIBRATION

Both the calorimetry and waveform sampling devices contain provision for calibration pulsing into the preamplifiers. Active laser trimming of capacitors or resistors on the hybrid circuits allows a charge accurate to approximately 0.1% to be injected into the preamplifiers. A serial shift register system is used to enable the calibration pulses, allowing a completely arbitrary pattern of preamplifiers to be pulsed.

Because each sample and hold circuit in the AMUs must be calibrated, a separate system is required to obtain the relative calibration of each of the time buckets of the waveform sampling channels. This is done by varying the bias level to the inputs of the AMUs in order to perform a DC rather than pulsed calibration of all time buckets of the AMUs.

The calibration procedure requires a cooperative effort among the acquisition modules, the subsystem AEBs, and the trigger processor. For each subsystem a Timing and Control Module is used by the subsystem AEB to set the DACs to the pulsed and/or DC calibration systems and to control the serial enables to the individual channels. Pulsing of the calibration system and initiation of readout is controlled by the trigger processor (communicating with the AEBs) through the same TCM. Calculation of the calibration constants themselves is carried out by the acquisition modules (communicating with the AEBs). A series of calibration points are taken at known DAC values. The acquisition module microprocessors interpolate these data to fixed ADC values, for which the calibration curve of each time bucket is stored in the calibration memory. Because of the large number of buckets which must be calibrated, the parallel processing power provided

by the acquisition module microprocessors is crucial in allowing the system to be calibrated in a short period of time.

10. HOST SYSTEM

The host processor system is shown schematically in Fig. 10. The central processor is expected to be a VAX 8800. The responsibilites of the host include:

- Logging of event data.
- Distribution of event data to consumer processes, resident either in the host or in graphic workstations.
- Analysis of event data and accumulation of summary statistics and displays.
- Distribution of summary display data to the graphic workstations.
- Resource allocation and control of the acquisition system.

The host processor is coupled by ethernet to a number of VAX graphic workstations used for control and display of the experiment. The workstations contain sufficient cpu power to allow parasitic analysis of event data, *e.g.*, the accumulation of data subject to different cuts from those used in the host processor. The host processor is also capable of emulating the functions of the workstations on graphic terminals, allowing uniform access to the system from remote locations as well as through the workstations.

Monitoring and control of the experimental equipment, (*e.g.*, high voltages, cryogenics) is carried out through MicroVAXes operating from uninterruptable power and interfaced through CAMAC.

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The data acquisition system for a project the size of SLD is clearly the work of many people. The following list of institutions and people is overly long but nonetheless does injustice to many who have been omitted. Electronics for the vertex detector is being developed by the Rutherford Appleton Laboratory (C. Damerell, A. Gillman, F. Wickens). Electronics for the Drift Chamber is

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12. Produced by SGS-ATES SpA, Milano, Italy.

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TABLE 1A
Digitization of typical SLD Event

Subsystem	Data Digitized (Mbytes)	Calibration Constants (Mbytes)	Data Out (Kbytes)
Vertex	58	0	1600
Drift Chamber	14	126	500
Čerenkov	24	216	100
Calorimeter	1	8	100
Total	89	350	2300

TABLE 1B
Acquisition board software processing of a typical SLD Event

Subsystem	Processing Power (MIPS)	Instructions /Word Available	Data Out (Kbytes)
Vertex	800	1000	40
Drift Chamber	300	600	50
Čerenkov	600	6000	25
Calorimeter	400	4000	20
Total	2100		135

FIGURE CAPTIONS

Fig. 1. Cross-section view of one quadrant of the detector.

Fig. 2. FASTBUS configuration.

Fig. 3. Vertex detector electronics.

Fig. 4. Drift chamber electronics.

Fig. 5. Drift chamber waveform data (after calibration) obtained from an AMU.

Fig. 6. Wave-form sampling module.

Fig. 7. Digital correction unit.

Fig. 8. Calorimetry electronics.

Fig. 9. Iron calorimeter electronics.

Fig. 10. Host computer configuration.

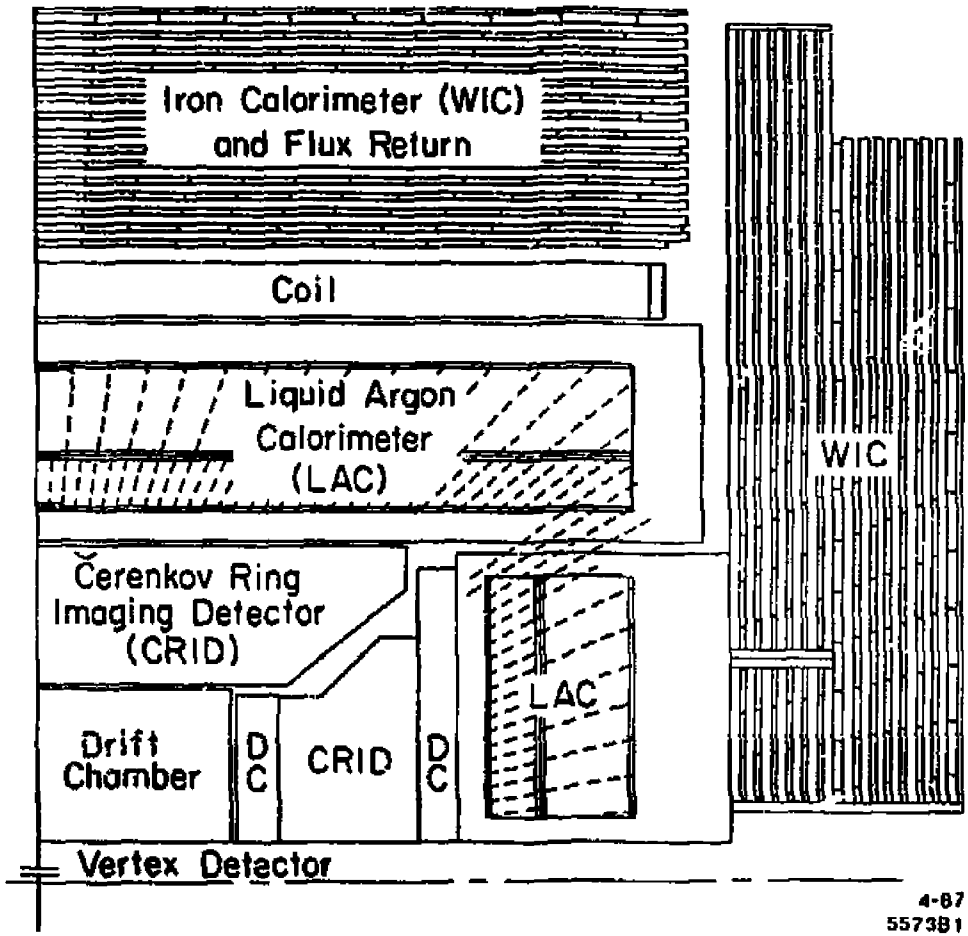
Iron Calorimeter (WIC)
and Flux Return
Coil
Liquid Argon
Calorimeter
(LAC)
WIC
Čerenkov Ring
Imaging Detector
(CRID)
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Fig. 1

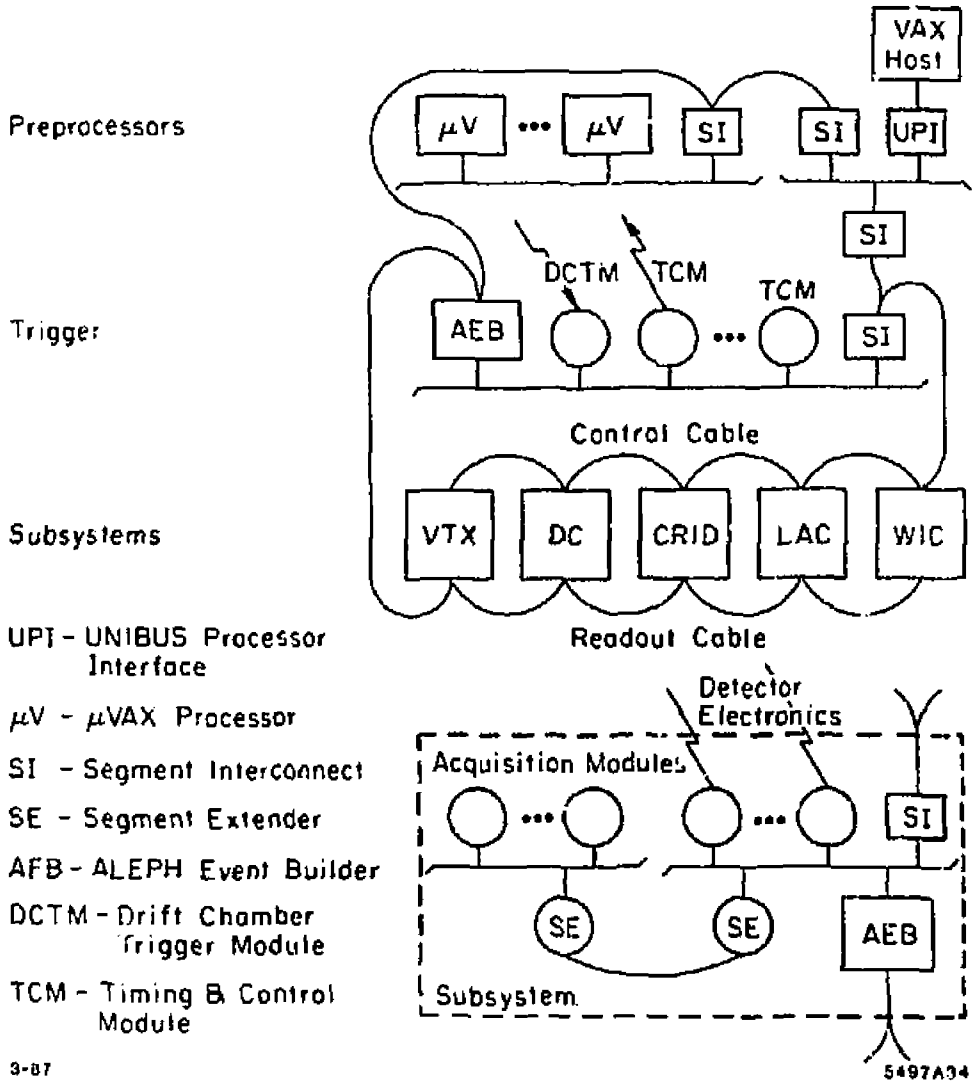
Preprocessors
Trigger
Subsystems
VAX Host
μV
μV
SI
SI
UPI
SI
DCTM
TCM
TCM
AEB
SI
Control Cable
VTX
DC
CRID
LAC
WIC
Readout Cable
Detector Electronics
Acquisition Modules
SI
SE
SE
AEB
Subsystem
UPI - UNIBUS Processor Interface
μV - μVAX Processor
SI - Segment Interconnect
SE - Segment Extender
AFB - ALEPH Event Builder
DCTM - Drift Chamber Trigger Module
TCM - Timing & Control Module
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Fig. 2

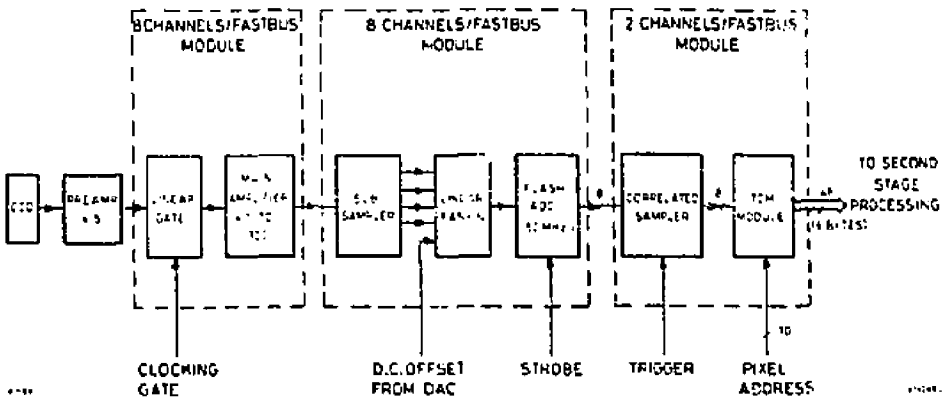

8CHANNELS/FASTBUS MODULE
8 CHANNELS/FASTBUS MODULE
2 CHANNELS/FASTBUS MODULE
CCD
CLOCKING GATE
D.C.OFFSET FROM DAC
STROBE
TRIGGER
PIXEL ADDRESS
TO SECOND STAGE PROCESSING

Fig. 3

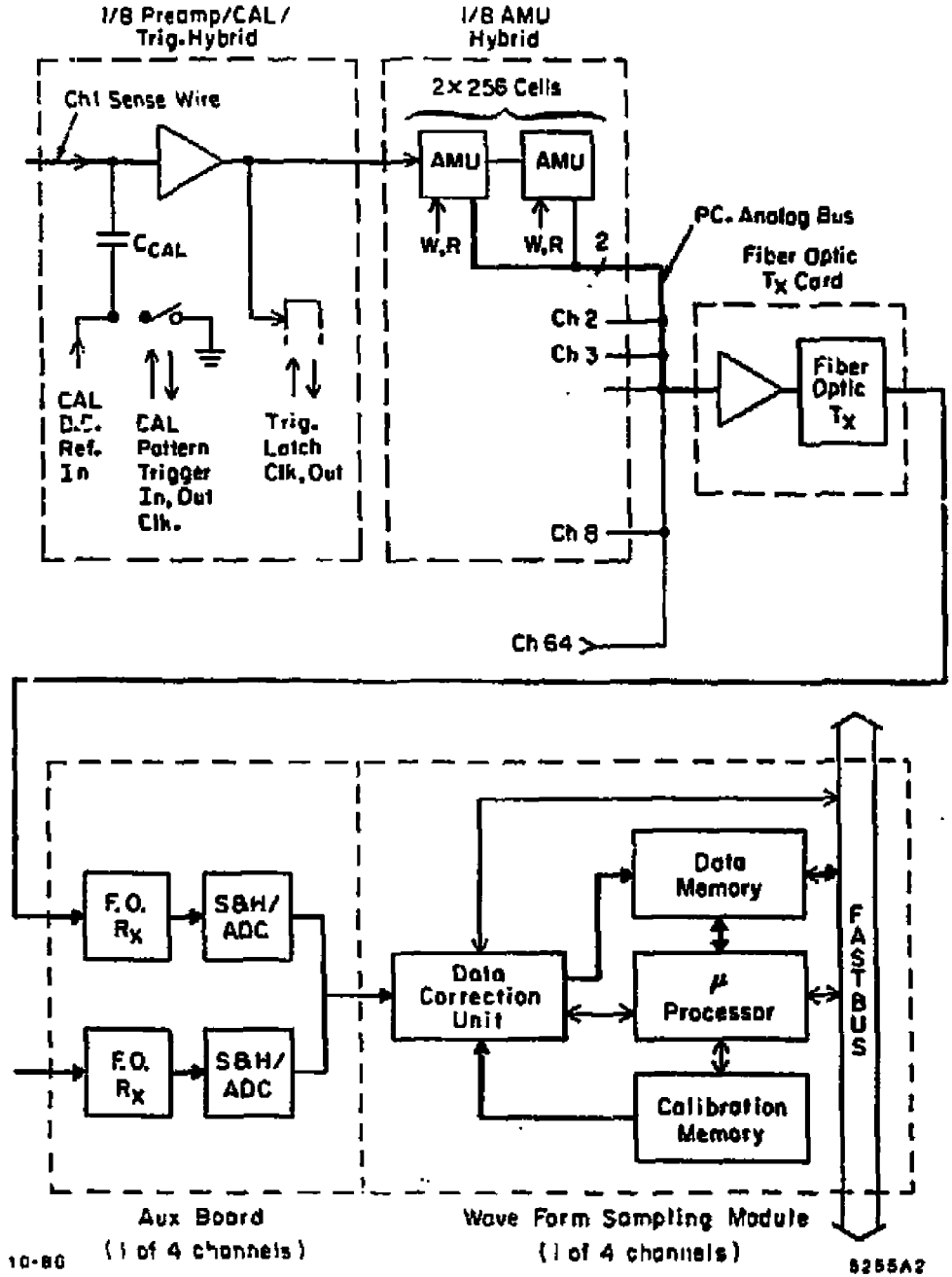

1/8 Preamp/CAL/ Trig. Hybrid
1/8 AMU Hybrid
2×256 Cells
Ch1 Sense Wire
AMU
AMU
W,R
W,R
2
PC. Analog Bus
Fiber Optic Tx Card
C_{CAL}
Ch 2
Ch 3
Ch 8
Ch 64
Fiber Optic Tx
CAL D.C. Ref. In
CAL Pattern Trigger In, Out Clk.
Trig. Latch Clk, Out
F.O. Rx
S&H/ ADC
F.O. Rx
S&H/ ADC
Data Correction Unit
Data Memory
μ Processor
Calibration Memory
FASTBUS
Aux Board (1 of 4 channels)
Wave Form Sampling Module (1 of 4 channels)
10-80
8255A2

Fig. 4

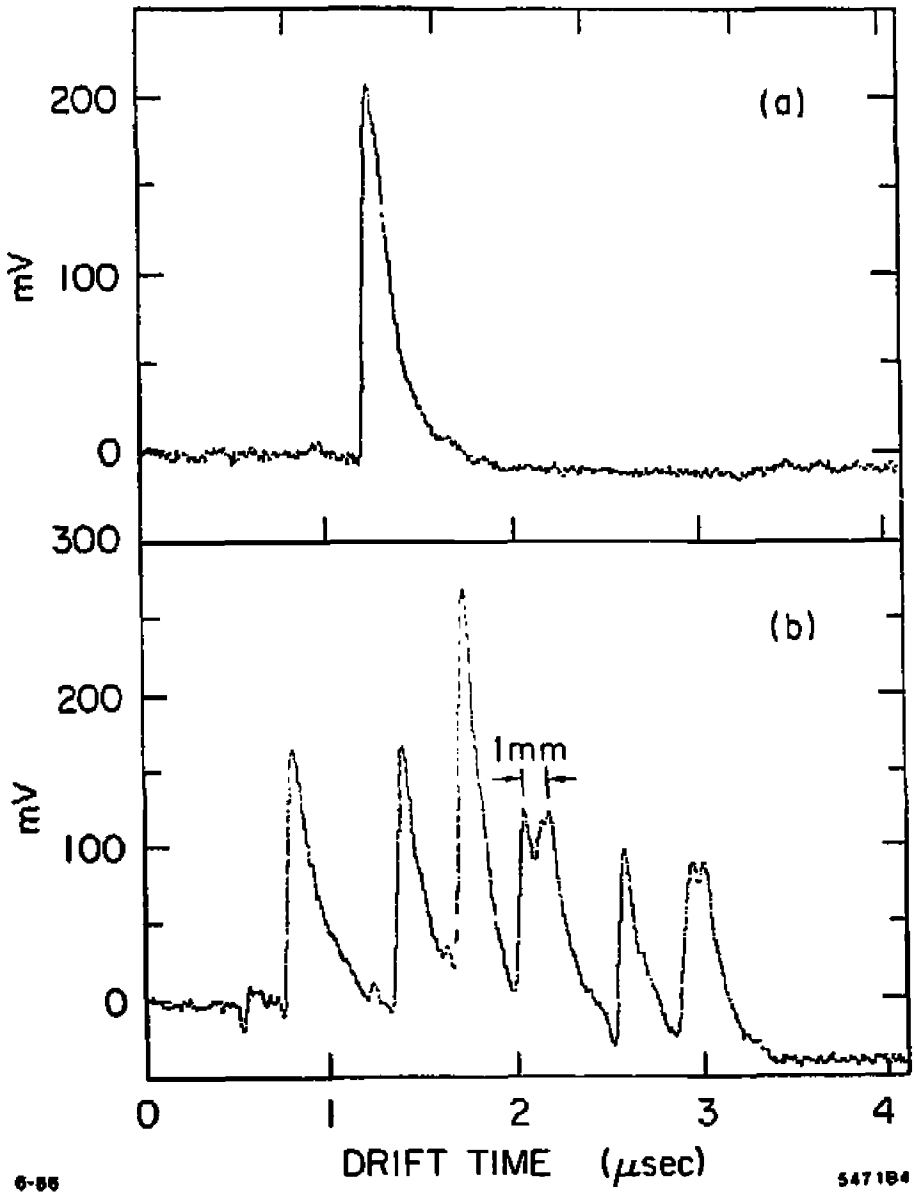

200
100
0
mV
(a)
300
200
100
0
mV
(b)
1mm
0
1
2
3
4
DRIFT TIME (μsec)
6-85
547184

Fig. 5

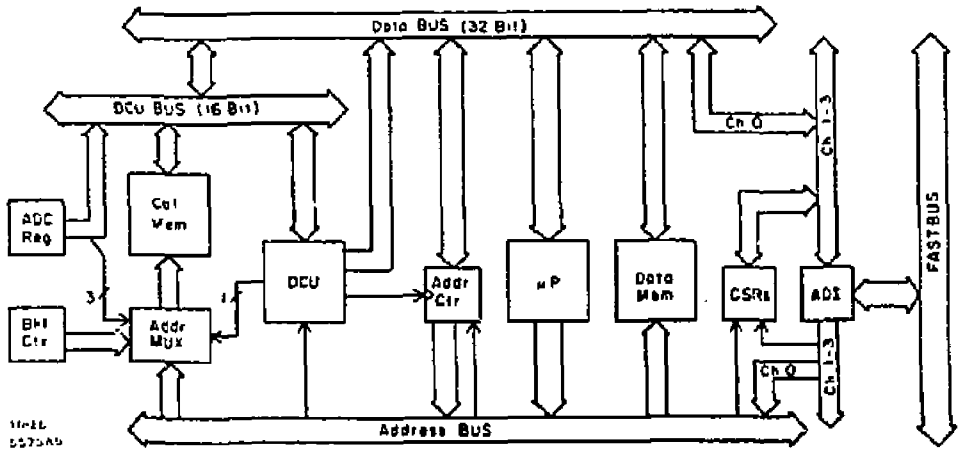
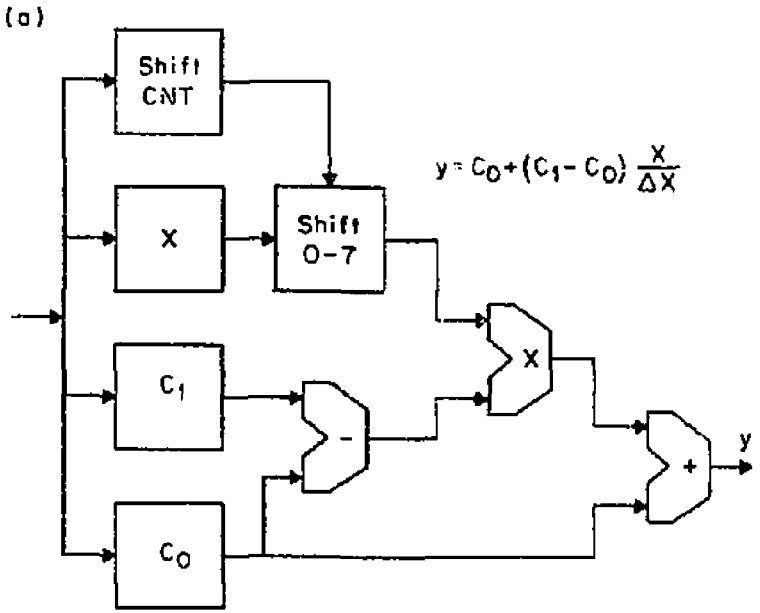

Data BUS (32 Bit)
DCu BUS (16 Bit)
ADC Reg
Cal Mem
BHI Ctr
Addr Mux
DCU
Addr Ctr
μP
Data Mem
CSRs
ADI
Ch 0
Ch 1-3
FASTBUS
Address BUS

Fig. 6


(a)
Shift CNT
X
Shift 0-7
C_1
C_0
$y = C_0 + (C_1 - C_0) \frac{X}{\Delta X}$
X
-
+
y

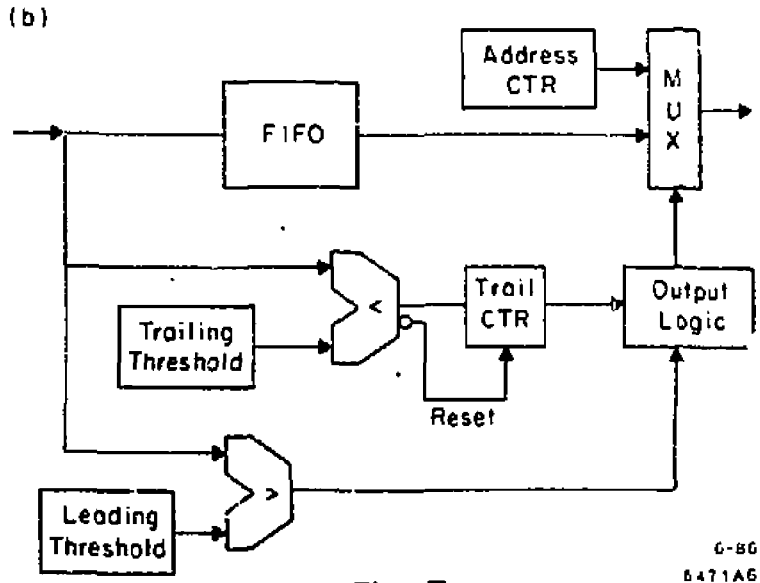
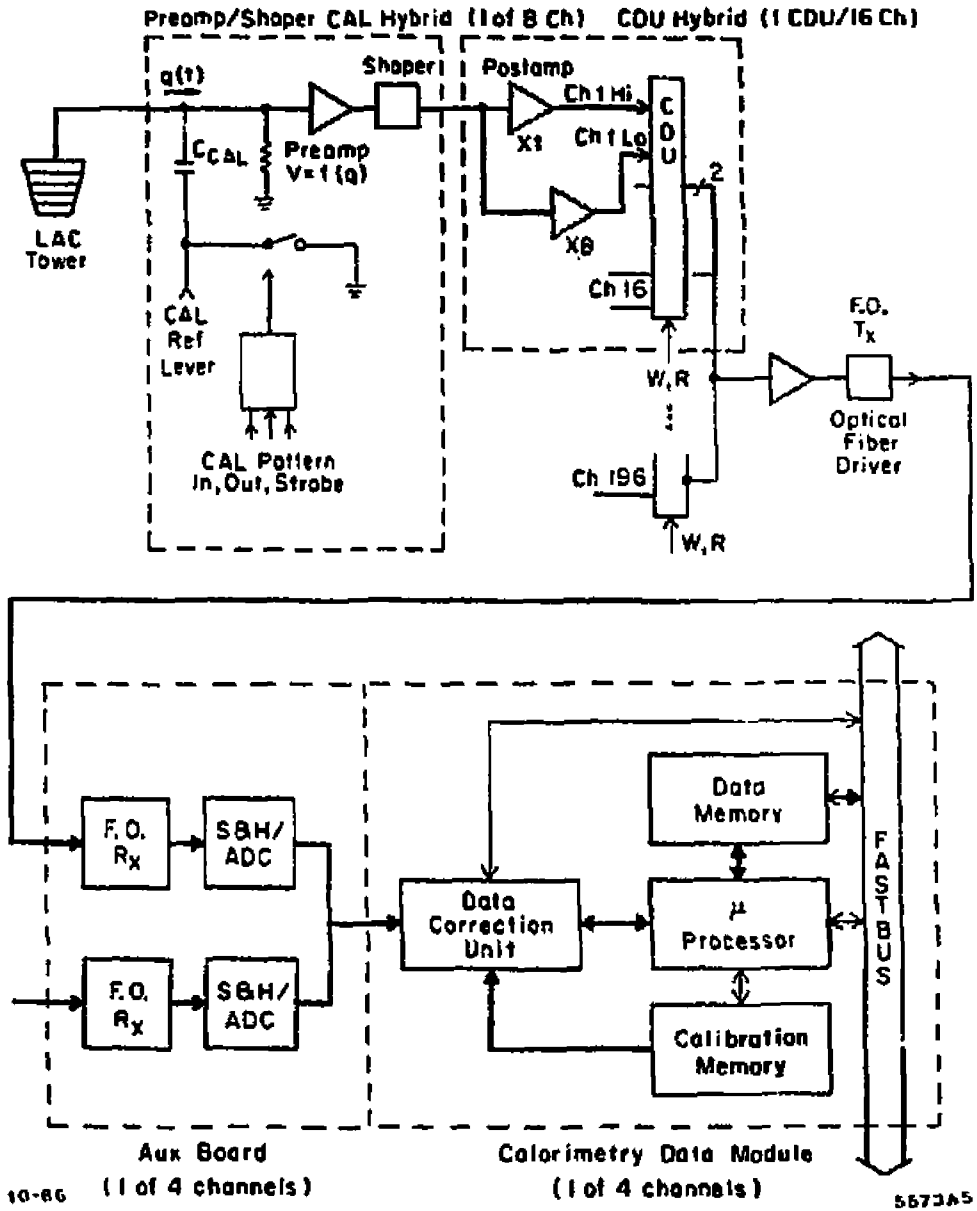

(b)
Address CTR
FIFO
M U X
Trailing Threshold
<
Trail CTR
Output Logic
Reset
Leading Threshold
>
6-86
5471A6

Fig. 7



Preamp/Shaper CAL Hybrid (1 of 8 Ch)
CDU Hybrid (1 CDU/16 Ch)
q(t)
Shaper
Postamp
Ch 1 Hi
Ch 1 Lo
Xt
XB
C D U
2
Ch 16
W, R
Ch 196
W, R
C_{CAL}
Preamp V=f(q)
LAC Tower
CAL Ref Lever
CAL Pattern In, Out, Strobe
F.O. T_x
Optical Fiber Driver
F.O. R_x
S&H/ ADC
F.O. R_x
S&H/ ADC
Data Correction Unit
Data Memory
μ Processor
Calibration Memory
FASTBUS
Aux Board (1 of 4 channels)
Calorimetry Data Module (1 of 4 channels)
10-86
5573A5

Fig. 8

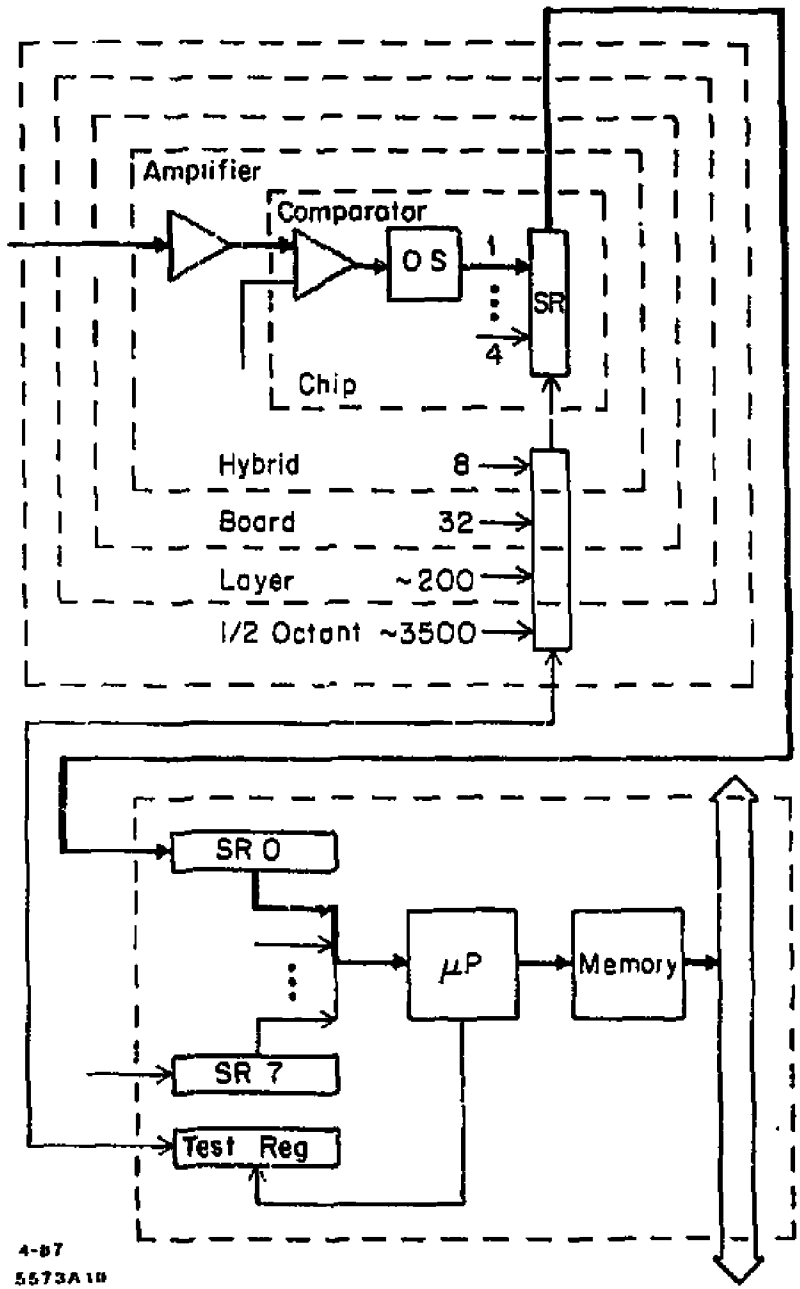

Amplifier
Comparator
OS
1
4
SR
Chip
Hybrid
8
Board
32
Layer
~200
1/2 Octant
~3500
SR 0
SR 7
Test Reg
μP
Memory
4-87
5573A18

Fig. 9

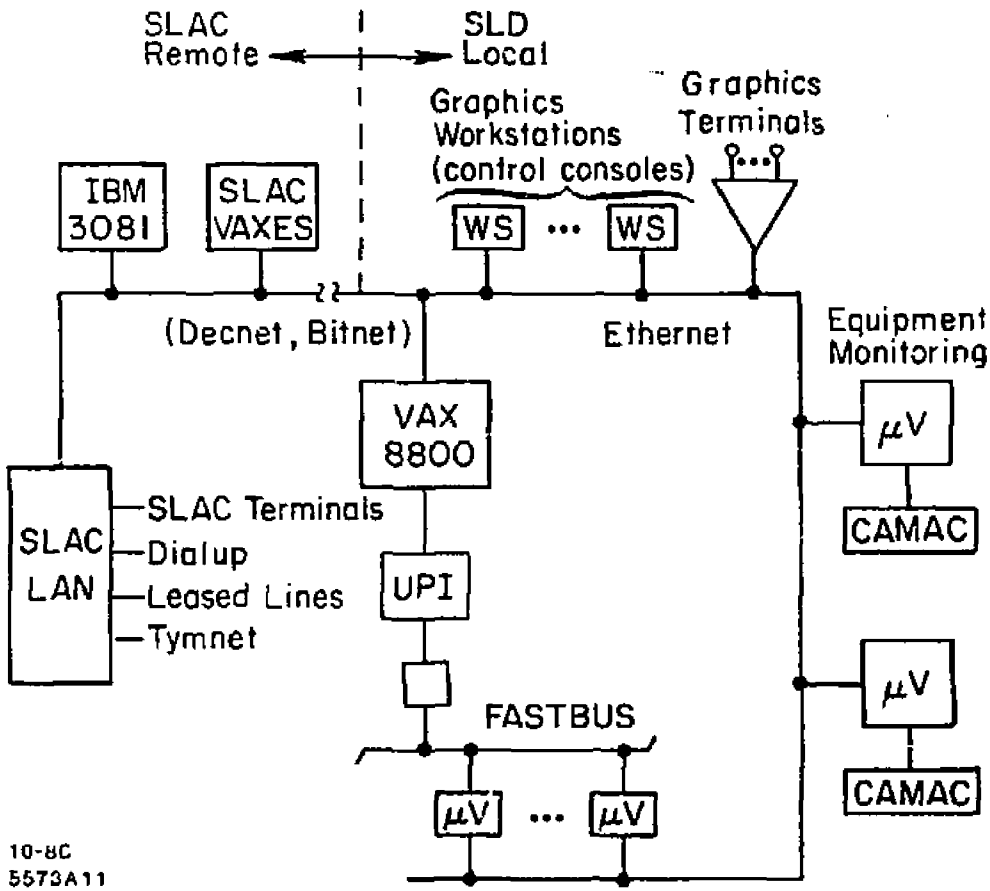

SLAC
Remote
SLD
Local
Graphics
Workstations
(control consoles)
Graphics
Terminals
IBM
3081
SLAC
VAXES
WS
WS
(Decnet, Bitnet)
Ethernet
Equipment
Monitoring
VAX
8800
μV
CAMAC
SLAC
LAN
SLAC Terminals
Dialup
Leased Lines
Tymnet
UPI
FASTBUS
μV
μV
μV
CAMAC
10-8C
5573A11

Fig. 10