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PERFORMANCE REPORT FOR STANFORD/SLAC MICROSTORE ANALOG MEMORY UNIT*

DIETRICH R. FREYTAG
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305
and
J. T. WALKER
Stanford University, Stanford, California 94305

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Abstract

Tests of a newly developed Analog Memory Unit (AMU) are described. The device contains 256 analog storage cells consisting of pass transistors, a storage capacitor and a differential read out buffer. By addressing the storage cells sequentially, the shape of the signal present at the input can be recorded in time. Fast response and good amplitude resolution were the design goals for the development. Measurements on individual devices will be presented and the status of hybridized subsystems containing eight AMU's discussed.

1. Introduction

In modern high energy experiments large numbers of rapidly changing analog signals must be recorded as a function of time and with high accuracy. This is needed in order to disentangle the partially overlapping signals from several elementary events arriving in any of the many detecting elements, e.g., sense wires in a proportional chamber. Two main approaches have been used to handle this problem on a large scale.

The most attractive solution, since it presents the shortest path to the desired result, is to digitize the signal amplitude in each channel at a high rate using flash ADCs and fast buffer memories. Large systems with 100 MHz sampling rate and six or seven bit accuracy have been realized, but any significant improvement in accuracy and, or sampling rate raises the cost of such systems to quite prohibitive levels.

The second approach that has received much support is based on the Charge Coupled Device (CCD). In this case the information is entered in analog form and at a high rate into the storage device and is subsequently retrieved more slowly for conversion into digital form. Achievable accuracies are generally higher than for flash ADCs but limited to about nine bits. The maximum frequency is generally below 100 MHz with low cost devices operating in the 20 MHz range. Higher sampling frequencies are reached by interleaving measurements in several devices.

Analog systems based on the storage of charge in a capacitor are capable of considerably higher accuracy than the two devices mentioned above. For systems constructed from discrete components, the dynamic range approaches 13 bits, whilst for a commercially produced monolithic device of the capacitive storage type[1] a dynamic range of 11 bits was measured. The device in question contained 32 analog cells in one chip, allowing a much higher packing density than with discrete components, but not competitive with flash ADCs or CCDs.

In view of the good performance of analog systems based on storage of charge in a capacitor, SLAC initiated a collaborative effort with the Integrated Circuits Laboratory of Stanford University to develop a new device of this kind, making use of the latest advances in very large scale integration. The first device resulting from this collaboration and to be described here is optimized to achieve good time resolution. (A second device with an emphasis on optimal amplitude resolution is ready for prototyping). The device uses NMOS technology with a minimum feature size of 3 μm, a process which is routinely handled by many silicon foundries. A contract for the manufacture of preproduction quantities of the device has been awarded by SLAC.

2. Description of the Analog Memory Unit (AMU)

2.1 Cell Structure

The logic structure of the storage cell for analog information is shown in Fig. 1. A storage capacitor is connected through FET switches to the signal input and disconnected when the gate voltage on one of the FETs drops below threshold. Two FET switches are used in series so that the 256 cells of the device can be addressed in the form of a 16x16 matrix. The time constant of the

Fig. 1. Circuit diagram for one storage cell of the device.

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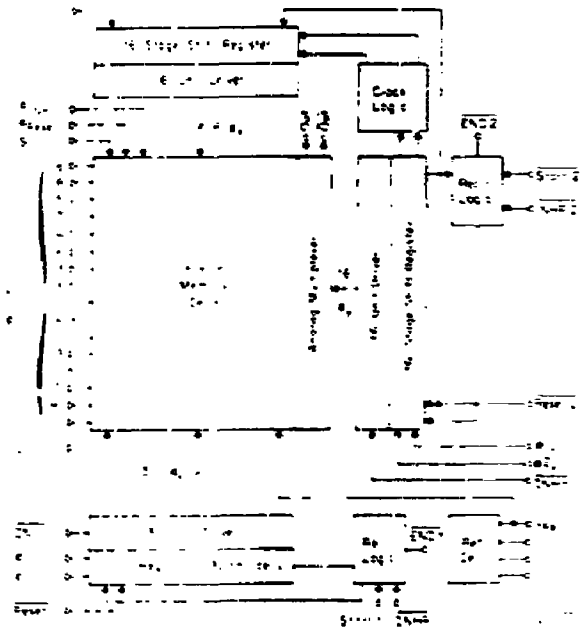

Fig. 2 Block diagram of the write and read logic of the device

input combination is approximately 1 ns (1 kΩ and 1 pF) resulting in a bandwidth of greater than 100 MHz. The first FET is controlled by one of 16 externally supplied fast strobe signals while the second FET is selected by the internally generated row select signal. More accurately, each row is broken in two giving 32 half rows alternately connected to the first or second group of eight fast strobes. As a result, the select signal can build up in a half row during one half row cycle, then there is the active cycle lasting eight fast strobe cycles, and this is followed by another half row cycle during which the select signal decays. An analog reset is provided at the storage capacitor whilst a clamping transistor near the input provides additional isolation of the storage capacitor during read out of the analog information.

The wide dynamic range of the device is basically due to the comparatively large stored charge, approximately 10^7 electrons at full scale, much more than for CCDs. The high rate capability of the AMU is achieved through the parallel access to the cells, which circumvents the difficulty of pushing charge at high rate through a single port.

Read out of the analog information proceeds through a matched pair of source followers with a reference input accessible from the outside so that suitable correction levels can be injected if required. The analog information is gated through two levels corresponding to column and row address and arrives in differential form at the two analog output pins.

The inputs of the 256 memory cells of the device are connected in two groups of 128 cells each so that two independent signals can be recorded in 128 time buckets as an alternative to one signal with 256 timing measurements.

2.2 DISCUSSION OF ON-CHIP LOGIC FOR WRITE AND READ

With the exception of the fast strobes which are externally supplied in order to achieve the highest possible speed, all other control signals are internally generated in response to external signals. The block diagram of the logic circuitry of the device is shown in Fig. 2. Row address during write is supplied by a 16-bit dynamic shift register. Both half cells of each shift register stage are used to address two sequential half rows. Each of the two non-overlapping clock pulses advances the row address by one half unit. Column select during read is controlled by a 16-stage dynamic shift register. A second 16-stage shift register sequentially addresses the 16 rows and is advanced by one for each complete cycle of the column address. The control signals needed for the write and read out shift registers are

reset	clock1	inhibit select
start	clock2	inhibit recirculate

The logic generates an end signal upon termination of the cycle, which is used as a carry signal for cascading of multiple AMU's.

The reference cell shown in the block diagram is a sampling cell identical to all other cells in the system except that it has separate signal and gate inputs and its own differential outputs. Its purpose is to serve as a monitor for any kind of drift which may be experienced by all cells. The output of the reference cell can thus be used to generate a compensation signal which can be fed back into the reference input of the device. No use of the reference cell has been made in test measurements so far and in most applications is not necessary at all.

3. Report on Tests and Measurements

The first set of measurements to be presented is the response of all the cells in one device to various DC levels at the input. Figure 3 shows the result obtained at a sampling rate of 150 MHz with input signals set to 0, 100, and then in 200 mV increments up to 1900 mV. Variations in cell response at a level of about five percent of full scale are apparent, most of which disappear when a cell by cell pedestal subtraction is made. Upon further analysis one notes a nonuniformity in gain among the cells at the 1.5 % level and a small positive curvature in the response characteristic. One must apply corrections for all these effects if a resolution of better than 10 bits is required. The RMS error for repeated samples at the same input level was 1/1000 of full scale which should be considered only as an upper limit for the performance of the device itself since no systematic search for the origin of the observed noise has been undertaken.

The data were fitted cell by cell to three parameters, offset, gain and curvature. Only eight out of 11 curves were used in the fits which thus had 5 degrees of freedom. The residuals for the three parameter fit were 3 to 4 mV, worse than the expected levels of accuracy. However, we know from experience that it takes a long time to tune an analog system to its maximum performance, particularly in this case where many internal nodes of the device are inaccessible to probing, so that the information about system behaviour must be obtained by a combination of model calculations[2] and indirect inferences. (The zero volt calibration curve is irregular because the negative step induced by gate cutoff drops the stored level below ground potential).

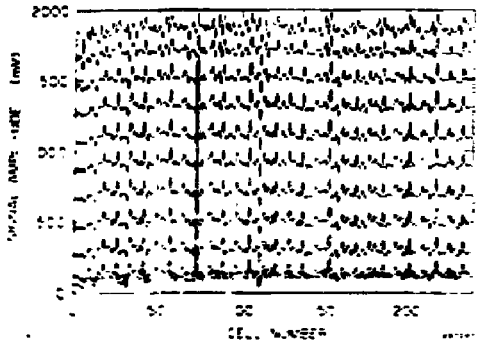

Fig 3 Calibration data taken at a 150 MHz sampling rate.

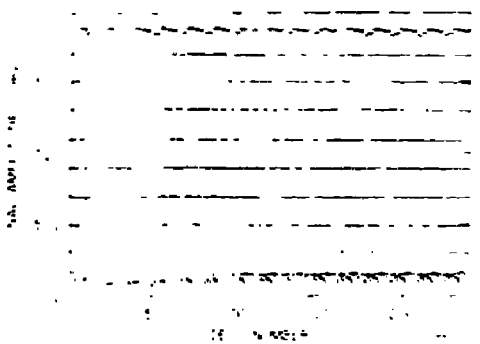

Fig 4 Same calibration data corrected cell by cell for offset, gain and curvature variations

The next set of measurements concerns the high frequency response of the analog memory. Fig. 5(a) shows a scan in 200 ps steps through the edge of a signal of 3 ns fall time. The edge shows up sharply and with no degradation of fall time. In fact the sampled fall time (2 ns) is slightly shorter than the fall time of the signal, which is due to the sampling mechanism and can be explained with the help of Fig. 5b. The pass transistor turns off when the difference between gate and signal voltage crosses threshold. As shown schematically in Fig. 5b, due to the finite fall time of the gate signal this shortens the sampled edge by approximately 1 ns. A rising edge will be measured correspondingly longer.

In order to obtain a more comprehensive picture of the high frequency behavior of all cells in the device, a 55 MHz sine wave of amplitude 1.2 V p-p with an offset of 0.9 V DC was injected into the signal input. The sampling frequency was set to 150 MHz (7 ns sampling intervals). This results in only three samples per period of the input waveform but these samples span 50 periods of the wave, which is a very rigid test of the sampling quality. A fit of the measured points to a pure sine wave with four free parameters (offset, amplitude, frequency and phase) was performed and by assigning errors of +-200 ps and +-7 mV (out of 2000 mV full scale), a χ^2 of unity per point was obtained. The quoted errors are not random in nature since each sample is reproducible to 100 ps in time and 1/1000 in amplitude. A careful study of systematic effects (variations in timing and amplitude of the seven fast strobes, distortions of the sine wave) should result in a reduction of the residuals quoted above.

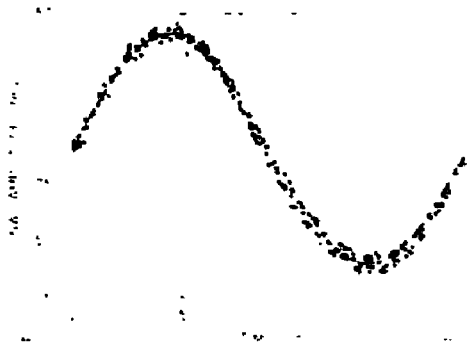

Fig 6 Superposition of 50 cycles of a 55 MHz signal sampled at a 145 MHz rate. The measured points are corrected for time walk induced by the sampling process.

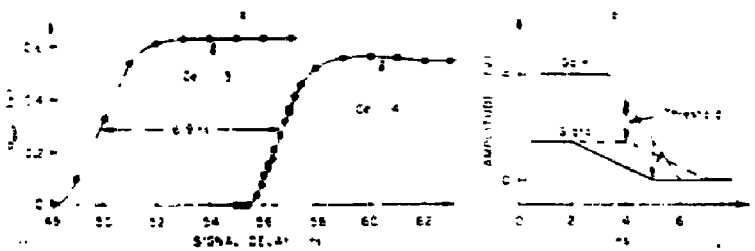

Fig 5 (a) Scanning of a signal with 3 ns fall time in 200 ps increments in signal delay. (b) Schematic representation of the effect on the timing of the sampling point caused by the variation of the signal amplitude

It is obvious from the results shown here that a waveform could be sampled effectively in much smaller steps than shown here. By interleaving measurements in 7 AMU's offset in time by 1 ns relative to each other, sampling at a 1 GHz rate could be achieved.

4. Hybrid Design

Large systems containing many thousand AMU's cannot easily be constructed from individually packaged devices because of the large number of external signals (approx. 40) needed for each unit. However many of these signals are common to groups of AMU's and others are daisy chained between devices so that it becomes advantageous to construct subunits of several AMU's which are internally connected. Fig. 7 shows the (commercially manufactured) prototype for a hybrid containing 8 AMU's, showing 108 external pins. Only about 40 of these pins need to be externally connected, the rest are brought out for diagnostic purposes. Later versions of the hybrid will incorporate logic circuitry in addition to the AMU's to further reduce the number of necessary external connections.

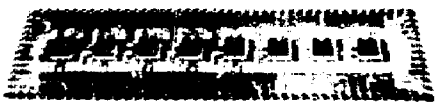

Fig. 7 Photo of prototype hybrid containing eight AMU's

Testing of the prototype hybrid has started and the calibration data presented earlier have been obtained for the group of AMU's mounted on the hybrid. The evaluation of the hybrid response to fast signals is continuing with satisfactory results so far. It is expected that prototype waveform digitizers (containing two hybrids each) running at 200 MHz sampling rate and providing 8 signal channels with 512 samples each will be available for testing by the end of the year.

Conclusion

All tests of the AMU performed so far show performance in agreement with the design parameters as far as timing accuracy and amplitude response are concerned. The determination of the true inherent noise requires a more careful investigation. However, the present result indicates that the noise level is not more than 1/1000 of the full scale range.

Acknowledgment

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At SLAC the performance goals were formulated and the technical and administrative steps for advancement of the project were undertaken by R. S. Larsen, M. Breidenbach and S. Shapiro. Many of our colleagues at SLAC helped to define and evaluate the tests.

D. Nelson of SLAC designed the module which generates the sequence of high speed control signals for the device.

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