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A FAST MULTICHANNEL ANALOG STORAGE SYSTEM*

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Summary

A Multichannel Analog Storage System based on a commercial 32-channel parallel in/serial out (PISO) analog shift register is described. The basic unit is a single width CAMAC module containing 512 analog cells and the associated logic for data storage and subsequent readout. At sampling rates of up to 30 MHz the signals are strobed directly into the PISO. At higher rates signals are strobed into a fast presampling stage and subsequently transferred in block form into an array of PISO's. Sampling rates of 300 MHz have been achieved with the present device and 1000 MHz are possible with improved signal drivers. The system is well suited for simultaneous handling of many signal channels with moderate numbers of samples in each channel. RMS noise over full scale signal has been measured as 1:3000 (≈11 bit). However, nonlinearities in the response and differences in sensitivity of the analog cells require an elaborate calibration system in order to realize 11 bit accuracy for the analog information.

Introduction

A parallel input analog storage register of width n accepts data at a mean rate at least n times the value which is possible if the data have to pass through a single serial port. The penalty for this rate increase is a greatly increased complexity of interconnections which limit the number of analog channels which can be handled with a reasonable effort. However, the high sampling rates which are possible (up to 1000 MHz) and the dynamic range of 11 bits are performance specifications which are not simultaneously available in the existing technologies of flash ADC's or fast CCD's. Moreover, since the rate boost comes from the parallel handling of the analog information and not from using advanced technology in the component circuits, one benefits from the advantages of low cost and low power consumption of the MOS devices used.

System Organization

The system organization is shown in the block diagram (Fig. 1) and the program of drive pulses in Fig. 2. For sampling at ≈30 MHz only the circuitry corresponding to the right half of the block diagram is needed. In the slow sampling mode the module can handle 32 signals in 16 time intervals of 33 nsec each (or longer) or 64 signals in 8 time intervals. Higher multiples of 32 signals with correspondingly smaller numbers of time bins are possible but the routing of signals becomes difficult.

The sampling intervals can be shortened and the number of input signals varied over a wide range by the use of the presampler shown in the left half of Fig. 1. In the tests to be described, the prototype was arranged in such a way that 256 time bins were allocated to each of two input signals. Other arrangements, e.g., 8 signals with 64 time bins each can be realized by changing patches.

The sequence of operations to acquire analog data is shown in Fig. 2. The first sample pulse of phase 1 generates a sequence of gate pulses from the sequencer to the presampler. After the last analog sample is stored in the phase 1 presampler, the block of 32 analog

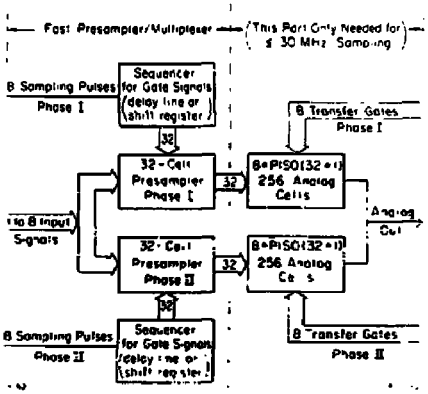

Fig. 1. Block diagram of the electronics.

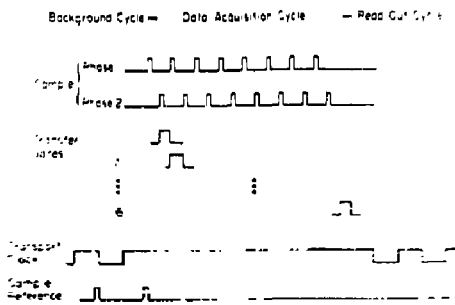

Fig. 2. Timing diagram of control signals.

samples is transferred into the first PISO register by transfer gate 1. During the transfer interval (≥ 33 nsec) a sequence of gate pulses is sent to the phase 2 presampler, and so on, for a total of sixteen sampling and transfer cycles. In this way the measurement interval is evenly covered by samples. It is also possible to release the individual sampling pulses in a triggered mode and cover only a subinterval after each trigger with measurements. During the data acquisition cycle the transport clock is held high. The readout cycle which follows is determined by the digitization time of the analog information, which in the present system takes 1.5 msec for 512 analog values of 12 bit accuracy.

During the time interval between the end of the readout cycle and the start of the next data acquisition period the transport clock continues to cycle. The output signal present at the PISO registers during this background mode is strobed into separate sample and hold stages and serves as a reference against which the active signal is measured. This approach stabilizes the system against slow variations of supply voltages or of clock amplitudes.

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Circuit Details

Figure 3 shows details of the circuitry for the acquisition of the analog samples. Each of the two presamplers is made of eight SD5000 switches through which the stray capacitances loading each data bus are charged to the instantaneous level of the signal. The sequence of gate signals for strobing are generated by a delay line made of 34-conductor mass terminated flat cable. The driver is a TTL to MOS converter 75366 (4 sections in parallel). This sampling pulse generator gives sufficiently fast trailing edges down to sampling intervals of ≈2 nsec. The signal is degraded as it passes 16 nodes with 2 gate connections on each but by providing enough amplitude one can ensure that the parts of the signal causing the switching transition are sufficiently fast. The analog signal at present comes in directly on a 50Ω coaxial cable resulting in a rise time of the signal on the data bus of ≈10 nsec, too slow for the desired sampling rates. In a smaller test system where the capacitive loading of the signal was less severe, sampling in 1 nsec steps gave a satisfactory reconstruction of a doublet of Gaussian shaped signals of 8 nsec half width and 20 nsec separation. Shorter sampling intervals should be possible with this prototype once a low impedance driver for the signal has been added. (Using a similar structure to the presampler, sampling at rates of 1 GHz and higher have been reported in the literature.[2])

Very little circuitry is needed for the readout logic since the data are already serialized in the PISO register. One noteworthy feature is the sampling and storage of a reference level from each of the PISO outputs at a time when no signal is present. The true signal is compared to this reference level in a difference amplifier. A photograph of the module is shwon in Fig. 4.

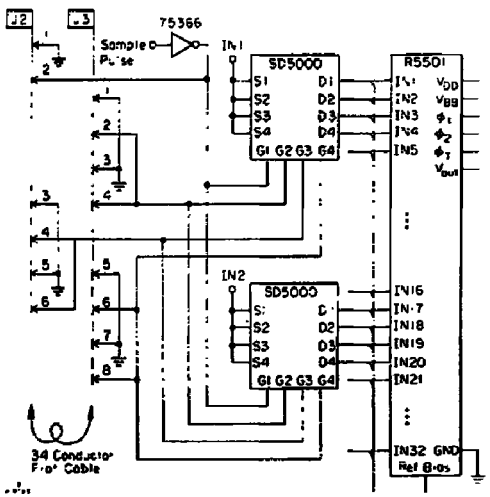

Fig. 3. Detail of the circuitry for the acquisition of the analog information.

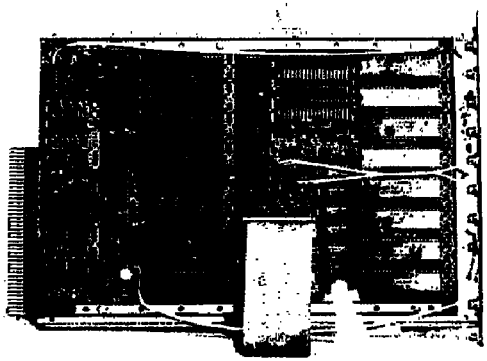

Fig. 4. Photograph of a module containing 512 analog cells. The 16 large packages are the PISO registers R5501 (EG&G Reticon). Two pairs of on-board flat cable connectors connect to the delay lines (one shown) for sequencing of the gate signals. Close by are the two blocks of SD5000 switches. Near the CAMAC connector is the circuitry to multiplex the analog information from 16 PISO registers onto the analog bus. Other sections in this region sample and store the reference signals or generate the 16 transfer clock pulses.

Results

The prototype shown here has been completed only recently and test programs to analyze and display the large amount of information generated by it are not yet sufficiently developed to fully assess its performance. The sample data of Fig. 5 have been obtained by injecting a test pulse into an arbitrary time window of the module. The sampling intervals were 2.8 ns and the digitized data were corrected for variations in the sensitivity of the analog cells. The test pulse of 6 nsec risetime is shown as a full line and is well represented by the data points.

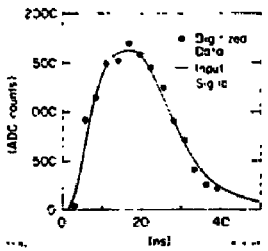

Fig. 5. Digitized data superimposed on input signal. The risetime of the input signal was 6 ns. Analog data were digitized in 2.8 ns steps and corrected for sensitivity fluctuations in the individual analog cells. A signal driver of 100Ω impedance was used for this measurement.

Applications and Future Plans

One possible application of this system considered at SLAC is in the digitization of signals from high resolution drift chambers. Such detectors installed at colliding beam facilities generate fast and often overlapping signals in a vast number of channels. These conditions are also found in large arrays of photomultipliers viewing scintillators placed in intense particle beams. The system described here promises to provide accurate information of large bandwidth at acceptable cost. It does however require an extensive calibration system to realize its full potential. The high accuracy of the analog data effectively extends the bandwidth of the system beyond the nominal limits of the components because the original signal shape can be recovered from the data by unfolding with the measured response function of the system. We will investigate the feasibility of applying such corrections using the computing power of the BADC system.[1] Of the components used here, both the SD5000 (DMOS quad linear gate) and the R550l (PMOS bucket brigade device manufactured by EG&G Reticon) are difficult to obtain due to manufacturing anamolies. However, both represent classes of devices which are relatively easy to customize. Various possibilities of achieving the equivalent performance in one or more custom devices, with multi-sourcing a prime consideration, are being investigated.

Acknowledgements

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References

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