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dE/dx ELECTRONICS FOR MARK II EXPERIMENT AT SLAC*

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Abstract

This paper describes a 100 MHz pulse digitizer for dE/dx measurements on the MARK II drift chamber at SLAC. The electronics provides the read-out of the detector's 5832 sense wires, organized in 336 wires/FASTBUS crate. The system is based on a 16-channel FASTBUS module. The basic element of the module is the TRW 6-bit Flash-ADC.

Introduction

A Flash-ADC pulse shape digitizer has been designed for use on the MARK II/SLC large volume drift chamber.[1]

The drift chamber consists of a series of cells arranged in 12 cylindrical layers with wires in the axial direction and with each cell having 6 sense wires. Figure 1 shows the geometry of each cell. The sense wires are staggered by ±380 μm from the sense wire midplane to allow calculation of which side of the cell was traversed by the track. Each wire is instrumented with a preamplifier at the chamber feed-through, 20 feet of signal cable leading to a post-amplifier with pole-zero filter, and then 80 feet of twisted-pair cable leading to FADC module.[2]

The digitized pulses will enable a dE/dx measurement for particle identification and also complement the drift time measurements of a 2 nsec time resolution TDC system. The digitization is performed at 100 MSPS using a 6-bit TRW 1029J7C converter. This selection is the result of comparing the available FADC's and CCD's on the basis of overall performance, power dissipation, cost and packaging.

The full system of 5832 channels will be instrumented with 16-channel FASTBUS modules.

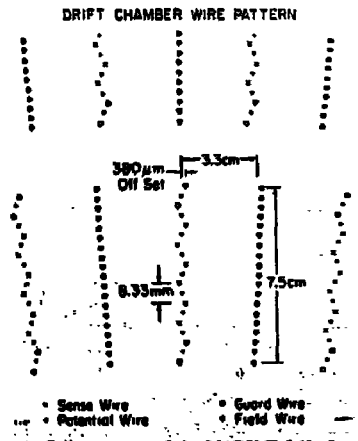

Fig. 1. Cell structure of the MARK II drift chamber.

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dE/dx System Organization

The dE/dx system consists of 365 modules in 18 FASTBUS crates. Each crate contains 21 dE/dx modules, an INTERFACE module and a SLAC SCANNING PROCESSOR (SSP).

The INTERFACE module, which accepts NIM pulses through the front panel, drives the backplane of the FASTBUS crate in differential ECL logic. It also provides — on the front panel — 21 NIM logic fanouts for 100 MHz clock.

One SYSTEM CONTROLLER supplies the required clock pulses — 100 MHz and 10 MHz — and control signals to all 18 Interface modules in the system, see Fig. 2.

The analog signals, carried by twisted-pair cables, are connected to the front panel of the dE/dx module.

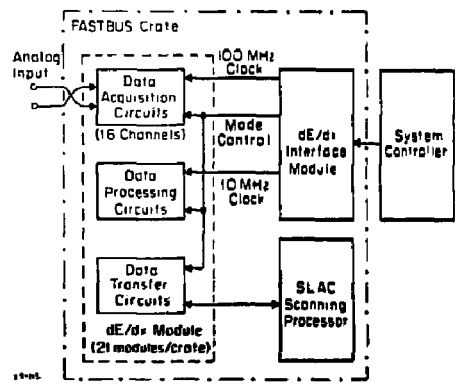

Fig. 2. dE/dx System: block diagram.

dE/dx Module

The dE/dx module is a single width FASTBUS module built on an 8-layer PC board, consisting of 4 signal-layers, 2 voltage-planes and 2 ground-planes. The module contains 16 FADC channels and associated FASTBUS readout electronics; it is a FASTBUS slave. Figure 3 shows a picture of the dE/dx module. The front-end occupies about one-third of the PC board, the conversion/storage circuitry takes another third and the rear is allocated to the FASTBUS electronics.

1. OPERATION MODE

The module is operated in three modes:

— Data Acquisition Mode

— Data Processing Mode

— Data Transfer Mode

The modes are selected by the System Controller.

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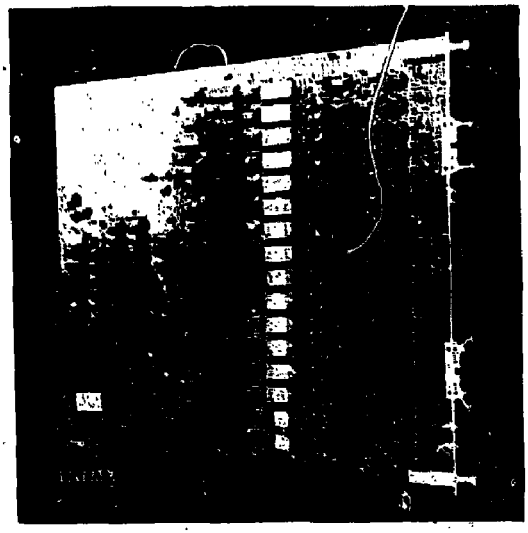

Fig. 3. View of the dE/dx module.

1.1. Data Acquisition Mode

In this mode the Data Memory for each of the 16 channels is enabled and the analog signals are digitized and stored into 256 × 4 ECL-memories. One-half of their capacity is used because, in our case, the drift time is less than 1.28 μsec. The module is clocked by an external 100 MHz clock which can be either synchronised to the beam crossing time or asynchronous for cosmic ray data acquisition.

1.2. Data Processing Mode

Zero suppression is achieved through an internal data processing cycle which records channel number and memory address for non-empty data. In this mode, 16 Data Memories are scanned at 10 MHz; a higher frequency is possible if necessary. This scanning requires 208 μsec. Each of the 128 digitized samples of a channel is compared with the channel's 4-bit threshold value stored in the Threshold Memory (16 × 4). The address corresponding to the first sample above the threshold, which marks the leading edge of the signal, and the last sample above threshold, which marks the trailing edge of the signal, are stored into the Address Memory (32 × 7). The leading edge of the first pulse and the trailing edge of the last pulse are stored for the channels with multiple hits.

The scanning leaves the data in the Data Memory unchanged.

1.3. Data Transfer Mode

All three sets of memories (Data, Threshold and Address) are accessed by the SSP, located in each crate. Random transfer and block transfer are possible. By reading the Address Memory the SSP determines which channels contain valid data and the number of corresponding samples to be read-out.

2. Circuit Description

Following is a brief description of some circuit design aspects of the dE/dx module.

A unity-gain front-end differential amplifier receives analog signals and drives through an emitter follower the input impedance of the FADC, see Fig. 4. This impedance is voltage dependent. Therefore, a 51 ohm termination provides the front-end amplifier with a constant load, independent of the fluctuations of the FADC's input impedance. It also decreases the RF pick-up.

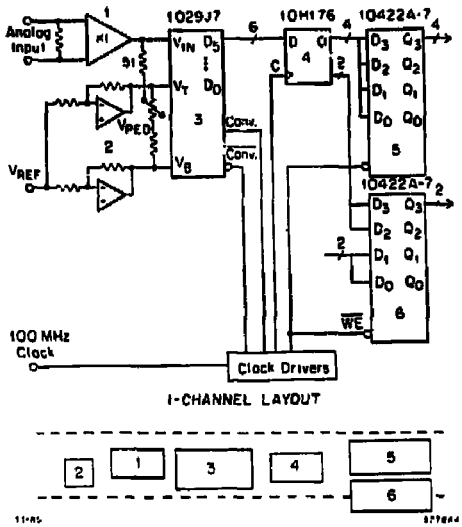

Fig. 4. Analog-to-Digital conversion: simplified block diagram.

The analog to digital conversion is linear. Each channel's FADC is biased by a dual op-amp driven by a reference voltage source in order to reduce the cross-talk between the 16 channels and the RF pick-up. One reference voltage source is provided per 8 channels. The pedestals are adjusted manually.

The design was originally based on a 10 nsec access time memory. A 6-bit fast buffer register was provided between the FADC and ECL-memory in order to guarantee the conversion at 100 MSPS. Currently the modules are equipped with 7 nsec access time ECL memory which allows conversion at rates up to 140 MSPS. A layout of the channel is also shown in Fig. 4.

Figure 5 shows a timing diagram for the conversion as seen at the IC's level; propagation delays inherent to the IC's and to the transmission lines of different lengths are not shown. These relative time delays represent the optimum condition which should be satisfied on each of the 16 channels of the module. Therefore the design was intended to avoid the necessity of delay adjustments for each individual channel. In order to achieve this goal, the 16 channels are organised in four groups with identical layout. This approach allows us:

- to ease the drive requirements,
- to reduce the length of the transmission lines for the numerous functions involved in the conversion/storage process,
- to preserve the relative time delays between the FADC's strobe (CONV & $\overline{\text{CONV}}$), Buffer Register's clock (C),

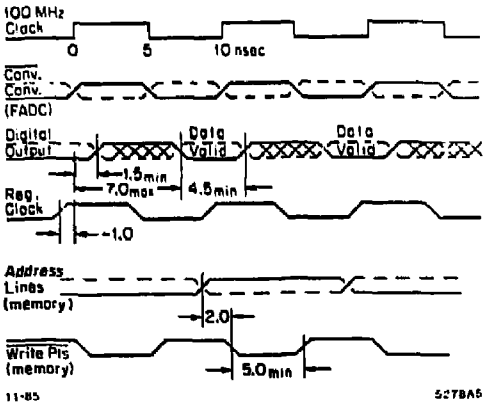

Fig. 5. Analog-to-Digital conversion: timing diagram.

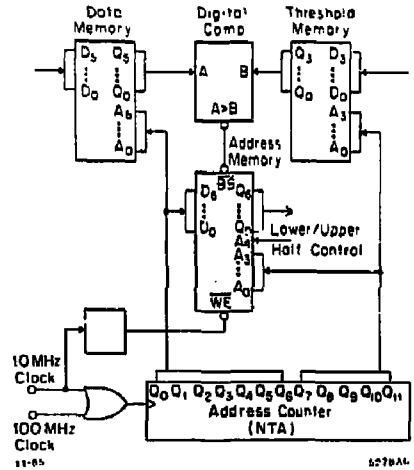

Fig. 6. Data Processing: simplified block diagram.

Memory's writing pulse (WE) and the Memory's Address-lines.

There is a provision to adjust the relative time delays between the conversion pulses (FADC), the clock pulses (Buffer Register), the Write Enable pulses and Address lines (Data Memories) which are common to all 16 channels.

Given the large size of a FASTBUS PC board, a time delay gradient across the board is unavoidable; the software should correct this for time measurements.

The Data Memory outputs are wire-ORed, buffered and connected to the FASTBUS AD-lines.

The Address Memory (32×7) is organized in a lower-half which stores the address of the first sample above the threshold and the upper-half which stores the address of the last sample above the threshold. In the Data Processing Mode, a digital comparator enables a write cycle in the Address Memory if the sample value is above the threshold value stored in the Threshold Memory. As a result, the address corresponding to this specific sample is written into the Address Memory, see Fig. 6. Before scanning any of the 16 channels the Address Memory is cleared.

As a FASTBUS slave, the module has been provided with the following functions: geographical addressing to CSR-space and DATA space, CSR#0, secondary addressing, random or block transfers.

The NTA register has a two-fold function:

- when loaded by the master, it addresses one of the three memory sets implemented in the module.
- when clocked during Data Acquisition or Data Processing it is used as the module's Address Counter.

For debugging purposes a 100 MHz-DAC, which can be plugged in the provided socket, follows the converted signal on-line. The analog signal is available on the front panel. For the same reason, a 10 MHZ clock can be plugged in the board to provide an internal source for the 10 MHz Data Processing clock.

Measurements and Performance

A full FASTBUS crate of FADC modules was recently connected to the MARK II/SLC drift chamber to be tested with cosmic rays. Two gas mixture were used in the test. One was HRS gas, a mixture of 89% Argon, 10% CO_2, and 1% Methane with a drift velocity of 52 μm/nsec and the other a slightly different mixture which gave a slower velocity of 33 μm/nsec. Some preliminary findings can be presented here:

- Pulse Shape: an average pulse shape is shown in Fig. 7. The average pulse shape was determined by adding pulses from many tracks; it has a width of about 50 nsec FWHM. Figure 8 shows actual pulses from 6 wires in one cell as recorded by the FADC system. This corresponds to a track along the middle of a cell.
- Linearity: the non-linearity in the measurement of the pulse area was found to be less than 2%.
- Track Separation: Figure 9 shows pulse trains for the 6 wires in one cell as recorded by the FADC system. This corresponds to two tracks in one cell. Two track

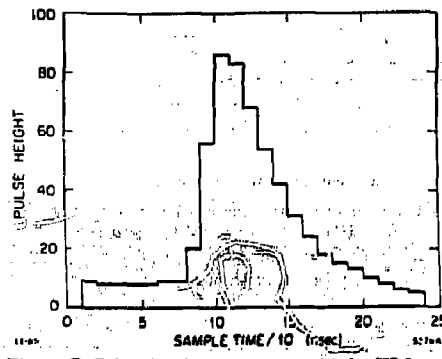

Fig. 7. FADC pulse shape: average pulse for HRS gas.

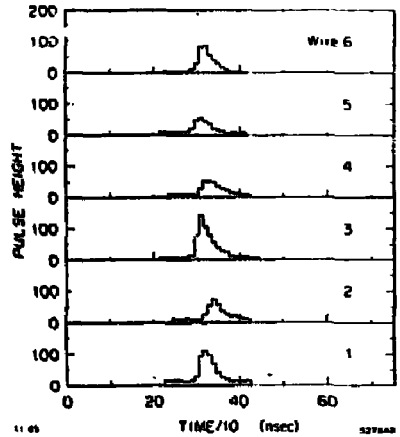

Fig. 8. FADC data: single track through one cell.

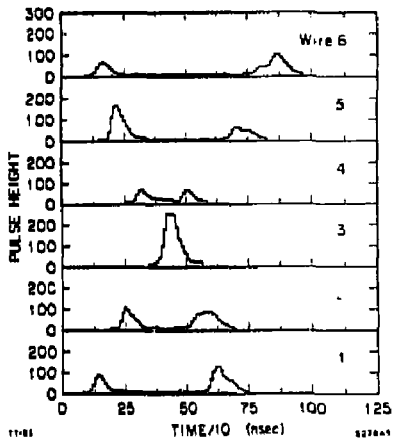

Fig. 9. FADC data: double track through one cell.

separation is still being studied but simulations suggest one should achieve separations of better than 3 mm.

— Timing studies from the FADC data have just begun. A simple algorithm which finds the leading edge by extrapolating to zero the first two bins above threshold was used for the time measurement of a pulse. The timing measurement was applied to the 6 signals from a cell over many tracks to provide timing performance for real tracks in the chamber. If $t_1, t_2, ..., t_6$ are timing measurements from the six wires, then the quantity

$$(t_1 + t_6 - 2t_2 - t_4 - t_5 + 2t_3)/8$$

gives the time to traverse the ±380 μm stagger in the sense wires. Figure 10 shows this distribution. The separation of the left and right side peaks measure the drift velocity, while the width of each peak can be used to estimate the time resolution from a single wire. A time resolution of 4.2 nsec (rms), for the whole system, is achieved. This corresponds to a spatial resolution of 120 μm (rms) per wire in the slow gas.

A second algorithm using the centroid of the first three bins above the threshold yields a similar resolution. The intrinsic resolution of the dE/dx electronics only is less than 2.9 nsec.

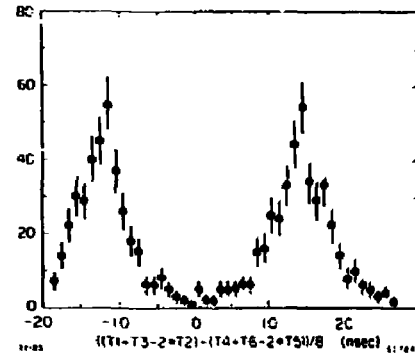

Fig. 10. Double peak distribution in slow gas.

The 16-channel FADC module has been tested. For the front end amplifier, the measurements performed on 16 channels show that gains are within ±3%, nonlinearity is less than 2% of full range and cross-talk is less than 1%. Temperature dependence of the pedestals was measured to be 0.2 LSB/10°C. The rise and fall time are 12 nsec. The specifications of the module are given in Table I.

Table I. Technical Specifications

Sampling rate	:	100 MSPS, external clock 140 MSPS maximum
Number of samples	:	128 (one-half of the memories capacity)
Resolution	:	6-bit, linear mode
Conversion	:	16 mV/LSB
Analog input	:	differential, z = 110 ohm $t_r = t_f$ = 12 nsec, $1V_{p-p}$
Sampling mode	:	synchronous, asynchronous
Pedestal	:	adjustable per channel
Noise	:	< 1/4 LSB
Data processing	:	@ 10 MHz
Data transfer rate	:	limited by the scanner
Channels per module	:	16
Power requirement	:	5.5 W/channel

Acknowledgements

We wish to acknowledge the assistance of P. Rankin and K. O'Shaughnessy in testing and evaluating the final design.

We would also like to acknowledge the efforts of D. Farwell, R. Matheson, J. Taylor, D. Andres and P. Martin in testing 140 dE/dx modules for 1/3 of the system.

References

1. "Proposal for the MARK II at SLAC," CALT-68-1015, DOE Research and Development Proposal, April 1983.
2. D. Briggs *et al.*, "The SLAC Mark II Upgrade Drift Chamber Front End Electronics," IEEE Trans. Nucl. Sci., Vol. NS-32, No. 1, February 1985.