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DESIGN OF THE AGS BOOSTER
BEAM POSITION MONITOR ELECTRONICS*

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Abstract

The operational requirements of the AGS Booster Beam Position Monitor system necessitate the use of electronics with wide dynamic range and broad instantaneous bandwidth. Bunch synchronization is provided by a remote timing sequencer coupled to the local ring electronics via digital fiber-optic links. The Sequencer and local ring circuitry work together to provide single turn trajectory or average orbit and intensity information, integrated over 1 to 255 bunches. Test capabilities are built in for the purpose of enhancing BPM system accuracy. This paper describes the design of the Booster Beam Position Monitor electronics, and presents performance details of the front end processing, acquisition and timing circuitry.

Front End Processing Module

The interface between the detector and the bunch signal integrators is the Front End Processing (FEP) module. Expected bunch widths (at half max) of from 3750 ns to 50 ns require a processing bandwidth of 40 KHz to 20 MHz. The need for wide dynamic range over this bandwidth [1,2] make the use of gain switching necessary. The module provides the frequency compensation needed to preserve the temporal profile of the bunch signals, and can supply gain or attenuation in three ranges (x 0.1, x 1 or x 10). In addition, the FEP takes the real-time sum and difference of these signals and delivers them to the integrators. Each FEP has a set of auxiliary outputs which can be configured to provide either buffered bunch signals or their sum and difference. These auxilliary outputs are currently being used as a commissioning aide, and will eventually be utilized by the Tune Meter, RF radial and phase control loops.

Each FEP input channel contains a shunt bleeder resistor whose purpose is to prevent excessive charge accumulation on the electrode and signal cable [3]. This resistor, together with the electrode and cable capacitances defines the low end of the FEP frequency response, as well as the amplitude of the bunch signals. The cables are matched to their characteristic impedance at high frequencies via series RC to prevent VSWR ripple. A series 200 ohm resistor at the detector end of the cable provides rolloff at the high end of the response as well as isolation of the PUE from signal reflections. Peaking at the top end of the response is reduced with a series RLC which shunts the input of the buffers. The center frequency and Q of this notch filter are adjusted during module alignment to maximize common mode rejection at the high end of the band.

A difference signal output which is -50 dB relative to the sum gives an FEP accuracy of ± 0.3 mm. This requires that both channels be matched to within 0.027 dB over the entire operating bandwidth. AD9610 current feedback amplifiers provide a flat response from DC to 10 MHz, lessening the tuning effort needed to meet this specification. It was found necessary, however, to match pairs of AD9610s due to small response deviations above 10 MHz. These particular wideband
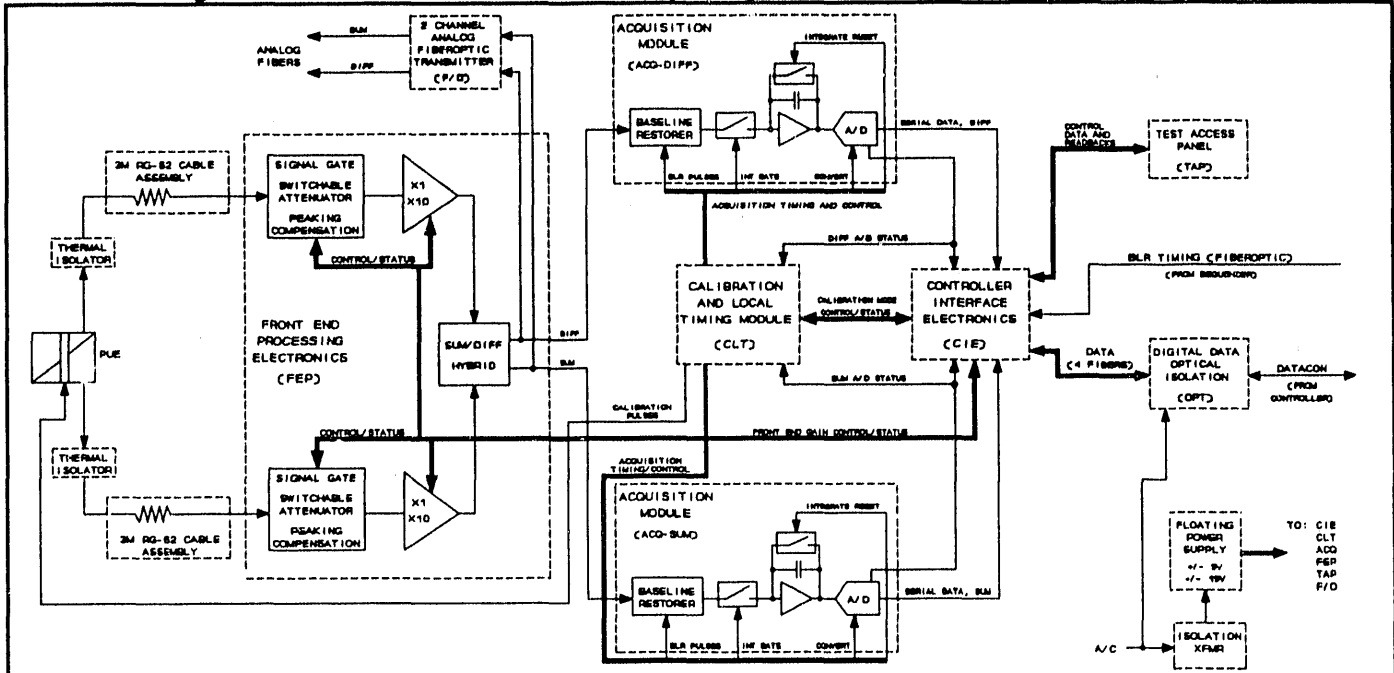

Fig. 1   Block Diagram of Local BPM Electronics.

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devices were chosen for their low input noise voltage (0.7 nV/√Hz), high non-inverting input impedance,(200 KΩ) and low input capacitance (2 pF). Since the AD9610 is a current feedback amplifier, unity non-inverting gain is obtained when its inverting input is left open. Shunting a resistor of appropriate value across this input results in a voltage gain of 20 dB.

Attenuation is accomplished by setting the AD9610 to unity gain and loading the PUE with an appropriate amount of additional capacitance. The additional capacitance also has the effect of widening the bottom end of the bandwidth, resulting in a flat frequency response of 1 KHz to 20 MHz. All of the switching which occurs in the FEP module is done using Clare DSS3105 long life expectancy (2 x 10^8 operations) relays.

A trifilar winding hybrid transformer with a common mode performance of better than -70 dB from 10 KHz to 30 MHz is used to take the sum and difference of the bunch signals. Signals out of the hybrid are buffered by HA5002 high speed video unity gain buffers, then sent to the Acquisition modules and auxilliary FEP outputs.

Figure 2 shows a network analyzer plot from a typical FEP module in the Booster. The calibration ring of a PUE detector is driven by the network analyzer, and the response measured from the AUX SUM and AUX DIFF outputs. The Sum output of all three gains are shown on the same reference line to simplify comparison of common mode performance between ranges.
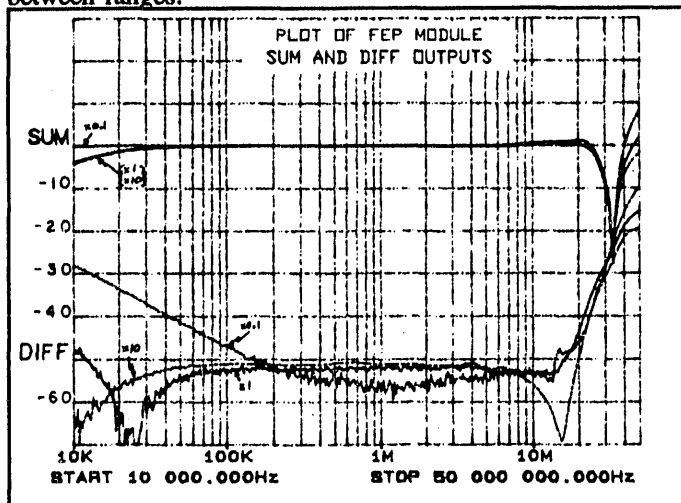

Fig. 2 FEP Module Sum and Difference Outputs.

Acquisition Module

There are two Acquisition (ACQ) modules at each BPM station in the Booster. The purpose of the ACQ is to integrate and digitize the Sum and Difference signals from the FEP module. Since they are reactively coupled in the FEP, these signals must be baseline restored before integration. The ACQ is required to accept bipolar pulses from 0 to 4.5 volts in amplitude, 50 to 3750 nsec in width (at half max) spaced from 240 to 4500 nsec, respectively. In addition, the ACQ must accommodate 75 % duty factor pulses at a 2.5 MHz repitition frequency (FEP signals due to chopped beam from the Linac).

Baseline restoration is accomplished by shorting the input signal to ground potential between bunches via a quad diode array arranged as a shunt switch. The diode bridge contains matched components to minimize offsets, and is biased on and off through a balun transformer to prevent unequal + and - bias voltages. The balun also provides a bias voltage gain of x2, since the diode bias must be larger than the amplitude of

the signal whose baseline is being restored. The pulses which drive the baseline restorer (BLR) circuitry are 60 nsec in width to accomodate the minimum spacing between Sum and Difference signals of 100 nsec. Since a 60 nsec pulse width does not allow sufficient time for complete restoration of the baseline, 12 BLR pre-conditioning pulses are received prior to the start of integration.

The baseline restored signal is fed to a high performance gated integrator with two sensitivity ranges (remotely selectable). Following receipt of 12 pre-conditioning BLR pulses, the signal is gated to the integrator for the period of time necessary to allow a pre-set number of bunches to pass through the detector. Once this time has elapsed, the gate is closed and the integrated output is held and digitized. After A/D conversion is complete, the integrator is reset. The gating and reset timing, as well as the A/D conversion start signals are all generated by the Calibration and Local Timing module. Signal gating and reset functions are accomplished with Analog Devices ADG201HS analog switches, chosen for their high switching speed and frequency independent charge injection characteristics.

System specifications require 13 bits of information (10 bits position and 3 bits dynamic range for each gain mode of the FEP module). An ADC71 digitizes the integral into a 16 bit word within 50 usec. The Sum (or Difference) information is then sent serially to the Controller Interface Electronics.

Calibration and Local Timing Module

The Calibration and Local Timing (CLT) module takes external timing bursts from the Sequencer and decodes them into the proper timing and control signals needed by the ACQ modules. A block diagram of the CLT is shown in Figure 3.
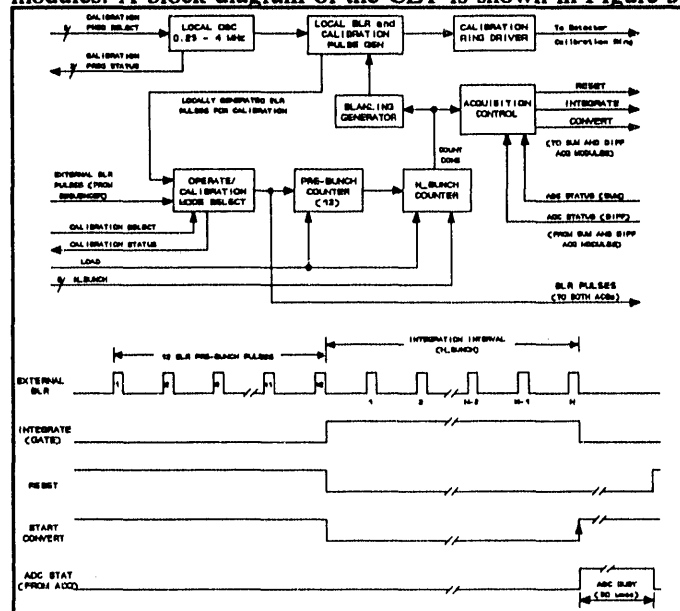

Fig. 3 Block Diagram of CLT Module.

The CLT module is initialized by loading the number of bunches over which to integrate (up to 255 bunches, or 85 turns) into the N_BUNCH counter. The arrival of a burst of 60 nsec pulses from the Sequencer initiates the measurement cycle. At the falling edge of the twelfth BLR pre-conditioning pulse, the CLT opens the integrator gates to both ACQ modules, and removes their reset signals. Analog Sum and Difference signals are integrated by the ACQ modules until N

more BLR pulses are counted. The analog signal gates are then closed and a CONVERT command is issued to the A/D converters. Only after the ADCs on both Aquisition modules have completed conversion does the CLT reset the integrators, completing the measurement cycle until the next burst from the Sequencer.

In addition to its normal mode of operation, the CLT has the ability to drive the Calibration ring of the detector with 12 volt pulses, enabling the BPM system to be tested without beam. In this mode, a 16 MHz clock is divided down to generate calibration pulses of programmable frequency. One burst of BLR and calibration pulses is generated each time the host computer sends a CAL_SEL (calibration select) command. Five possible frequencies (0.25, 0.5, 1.0, 2.0 and 4.0 MHz) are available, each with a 0.25 duty factor.

BPM Timing Sequencer

Timing for the BPM system is generated external to the ring by the Sequencer. Digital fiberoptic links enable low skew, precision timing pulses to be transmitted to each BPM station in the ring. The Sequencer divides the Booster ring into 48 equally spaced phases of the revolution frequency (f_{rev}).The
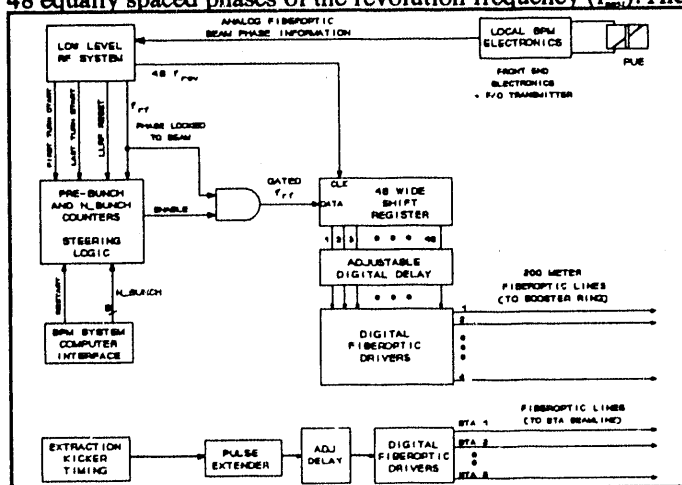

Fig. 4 Block Diagram of Sequencer.

Low Level RF (LLRF) system provides the Sequencer with the RF frequency (f_{rf}) and 48 x f_{rev}, both phase locked to the beam [4] (knowing both of these frequencies simultaneously makes operation of the Sequencer independent of harmonic number). The phase reference is sent to the LLRF system via high speed analog fiberoptic link, which sends a real-time bunch signal from an FEP module in the ring.

RF phase locked to the beam is gated into the data input of a 48 wide shift register, which is clocked by 48 x f_{rev}. Prior to a request for timing from either the BPM system computer interface (RESTART) or the LLRF (First_Turn_Start or Last_Turn_Start), logic 0 is being clocked through the SR. Upon receipt of a timing burst request, the gate opens and allows f_{rf} to be clocked through the SR. The gate is closed after counting 12 + N_BUNCH rf cycles (set by the BPM system computer), at which point the data input to the shift register is set back to a logic 0. The high speed clock to the SR continues, allowing the Sequencer output to "follow" the beam" around the Booster ring. The transit time of all fiberoptic lines from the Sequencer to the Booster ring are matched using adjustable delays.

First_Turn_Start (FTS) and Last_Turn_Start (LTS) are high resolution pulses from the LLRF system, and are timed

to occur exactly 12 rf cycles (plus transit delays) before the position measurement is to begin. RESTART is a relatively low resolution pulse originating from the BPM computer interface, and is used to make multiple position measurements within a Booster cycle.

Booster To AGS (BTA) transfer line timing is accomplished by sending an integration gate, rather than BLR pulses, through the fiberoptics. There are always three bunches traveling through the BTA line, eliminating the need for baseline restoration of the sum and difference signals before integration.

Support Electronics

As part of the effort to maximize signal to noise ratio, the local processing electronics are optically isolated from all external devices. In addition, crate power is provided by linear supplies which are isolated from true ground and allowed to float with the beampipe.

The BNL DATACON standard is used for communication between the local processing electronics and the BPM instrument controller. Bipolar DATACON signals are converted to fiberoptics at the Digital Data Optical Isolation unit (DDOI, see Fig. 1). Two transceiver pairs link the DDOI with the Controller Interface Electronics (CIE), which resides in the local processing electronics crate, and is powered by the crate supply. The CIE board fiberoptically receives and decodes commands from the controller, and transmits back status and data readbacks. In addition, the CIE board receives the fiberoptic timing signal from the Sequencer and converts it to a differential TTL signal for use by the CLT module.

The Test Access Panel (TAP) provides access to all of the backplane signals in the crate. A switch and I/O connector on the front panel of the TAP board enable the crate to be put under local control. In this mode, the CIE board is tri-stated and all commands, data and readbacks normally passing through the CIE are routed through bidirectional buffers to the front panel connector of the TAP board.

Analog fiberoptic transmitter modules are resident in several of the local electronics crates within the ring. These modules can be moved from station to station during the commissioning process, allowing real-time FEP signals to be monitored in the Main Control Room. Selectable gains of x1, x0.1, x5 and x50 are available for scaling the input signals to maximize the link SNR. Gain is realized using low noise AD9610 wideband amplifiers and is selected through the BPM system computer, with one bit slaved to the FEP gain. Low distortion transmission [5] is achievable with up to a 1 V_{pp} input. The noise floor of the link is 1 mV_{rms} for over 30 MHz.

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