Arbitrary Function Generator for APS Injector Synchrotron Correction Magnets*

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Abstract

The APS injector synchrotron has eighty correction magnets around its circumference to provide the vernier field changes required for beam orbit correction during acceleration. The arbitrary function generator (AFG) design is based on scanning out encoded data from a semi-conductor memory, a first-in-first-out (FIFO) device. The data input consists of a maximum of 20 correction values specified within the acceleration window. Additional points between these values are then linearly interpolated to create a uniformly spaced 1000 data-point function stored in the FIFO. Each point, encoded as a 3-bit value is scanned out in synchronism with the injection pulse and used to clock the up/down counter driving the DAC. The DAC produces the analog reference voltage used to control the magnet current.

I. INTRODUCTION

In order to obtain the precision of the magnetic field required for positron acceleration from 450 Mev to 7.7 Gev with low beam loss, correction magnets are used around the ring. Because of mechanical imperfections in the construction as well as installation of real magnets, the exact field correction required at each magnet location is not known until a beam is actually accelerated. It is therefore necessary to generate a correction field that is a function of the beam energy during acceleration. The fairly large number of correction magnets needed requires that the design of the AFG be as simple as possible yet provide the required performance. An important performance feature is that the function can be changed "on the fly", to provide the operator with a real-time feel during the tune-up process.

II. CONCEPTS USED IN FUNCTION GENERATION

The AFG design is based on scanning out encoded data from a first-in-first-out (FIFO) semi-conductor memory. The data input consists of a maximum of 20 correction values that are specified within the injector synchrotron acceleration window. Additional points between these values are then linearly interpolated to create a uniformly spaced 1000 data-point function stored in memory. Each point is scanned out in synchronism with the acceleration cycle and clocks an up/down counter driving the digital-to-analog converter (DAC). Since the function data is first stored before use, its effect is a feedforward correction rather than a real-time feedback action. The optimum function for each magnet is determined by an iterative process based on the beam quality during machine tune up.

The design of the AFG uses the staircase approximation of line segments to represent the desired arbitrary function correction. In the APS power supply system the DACs that generate the reference voltages to the current regulators are driven from the outputs of up/down counters. (See Fig. 1). The consequence of this design philosophy is that the control of a reference voltage is effected via pulse trains only.

The design presented here differs from other AFG designs [1]. Information derived from the points describing the arbitrary function rather than the points themselves, are stored in a FIFO memory. Each point is encoded in only a three bit value instead of the 11-bit value normally required for a number in the range of ±1000. A readout clock synchronized to the injection pulses of the injector synchrotron scans out data from each FIFO. The data are used to gate a clock to the up/down counter that drives a reference DAC. Circuitry is also provided that permits the "on the fly" update of the input function.

The simplest way to generate an arbitrary waveform for this system is to feed pulses to the counter as in Fig 1.

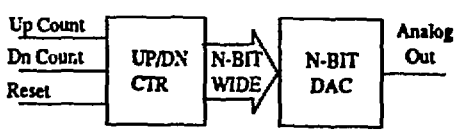

Figure 1. Analog Reference Block

If the pulse train can, in effect, be made to vary its rate, the DAC can produce any arbitrary waveform. For simplicity, the clock is fixed in rate at its maximum value and lower rates are generated by gating off a fraction of the clock pulses. Figure 2 shows an example of how a line segment AB can be approximated by incrementing or not its value at each clock time (using a fixed step size).

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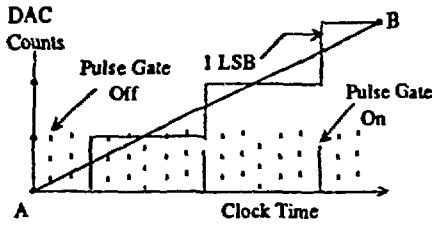

Figure 2 Staircase Line Approximation

II. REQUIREMENTS

The AFG requirements are as follows:

• Polarity	Bipolar
• Resolution (Amplitude & Time) 10 bits for magnitude 1 bit for sign	$1x10^{-3}$
• Repetition Period	0.5 s
• Function Duration (Acceleration)	0.25 s
• Number of points specified	< = 20
• Number of points supplied (Linear Interpolation used between specified points)	1000
• Dynamic update of function data	

III. THE DESIGN OF THE AFG

Figure 3 shows the correction magnet timing in an injector synchrotron cycle.

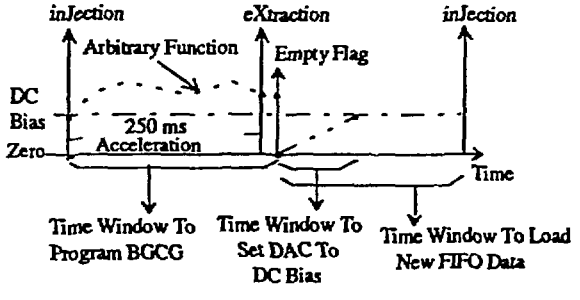

Figure 3. Arbitrary Function Timing in a Synchrotron Cycle

The injection pulse J is used as the reference pulse. The extraction pulse X is at the midpoint of the injector synchrotron cycle. The FIFO empty flag signal is generated when the last data point is output. This occurs after X when the DAC output and the FIFO read pointer are reset to zero.

Since the acceleration interval is divided into 1000 points and the function duration is 250 ms, the required clock period is 250 µs. The points that define the function to be generated are sent by the host computer to the power supply control unit (PSCU) where the pulse enable states, the DIR signal, and other initial parameters are determined prior to loading a 3-bit wide, 1000-bit deep FIFO memory.

3.1 Hardware Blocks

Figure 4 shows the Arbitrary Function Generator.

The Main FIFO block provides temporary data storage for the arbitrary function before transfer to the PS FIFO, so it eases programming and synchronization. A hardware clock is used to read this data and load the addressed PS FIFO.

Each PS FIFO stores arbitrary function data for its power supply. It can receive update data from the main FIFO and provides sync signal for the update process from its empty flag. Since all PS FIFOs are scanned in synchronism with the injection pulse, only one empty flag signal is used.

The Main Gated Count Generator (MGCG) supplies the required number of clock pulses (20kHz) to read the main FIFO and load the addressed PS FIFO. It is gated on by the presence of an update request signal at time the PS FIFO becomes empty.

Each Bias Gated Count Generator (BGCG) unit is programmed to deliver the required number of pulses (100kHz) to set the DAC to its DC bias level after its reset to zero following extraction.

The Input And Output Logic blocks generate other signals needed to synchronize the sequences of events and the selection of clock sources. PLDs (programmable logic devices) are used to implement the logic to reduce the IC count.

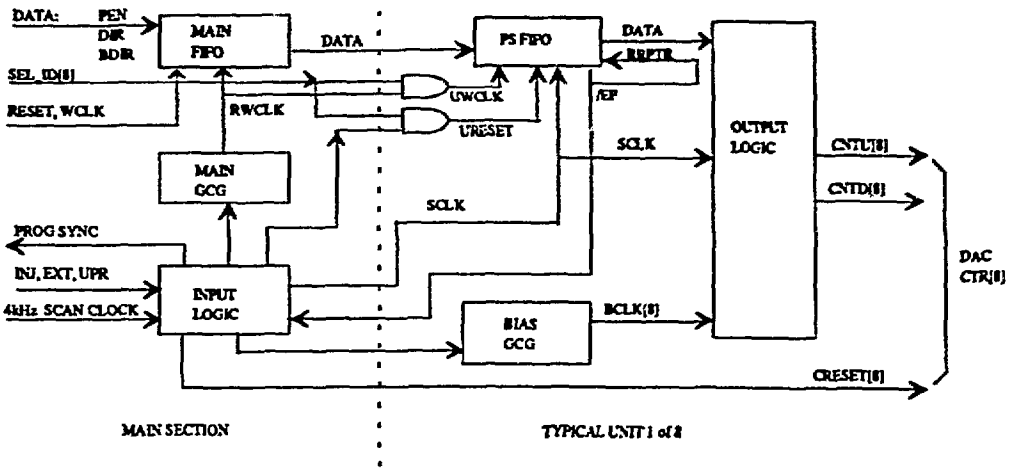

Figure 4. Arbitrary Function Generator

3.2 Operation

The PSCU receives from its host computer the data points describing the arbitrary function. The PSCU maintains the latest function data (20 points) for each power supply it services. From these data it makes calculations of the slope (DIR) and pulse enable signals (PEN) associated with the FIFO readout pulses for each line segment. The software also determines the number of pulses required to set the DAC counter to its DC bias for the new function. This number is programmed into the BGCG following injection if an update request is outstanding. The software generates update request and ID select signals to address the specific FIFO involved.

On the next empty flag signal after the update request, the addressed FIFO and DAC are reset and the addressed BGCG is activated delivering the programmed number of pulses (100kHz) to the selected DAC counter to set it to the new DC level. At the same time, the MGCG is started, reads out the main FIFO and loads the addressed FIFO. The update request latch is then reset. The new function is therefore in place when the next injection pulse occurs.

In its normal mode of operation, each function generator is repetitively scanning its FIFO in synchronism with the acceleration cycle. At every injection pulse, the 4kHz clock is selected to scan the FIFO and drive the DAC counter in accordance with the unit's direction DIR and unit's pulse enable PEN signals. At each empty flag time, the DAC counter and the read pointer of the addressed FIFO are reset to zero. The BGCG is then enabled to set the DAC to its DC bias value in preparation for the next cycle.

If at injection time an update request is present, the following additional actions are performed within the injector synchrotron cycle as indicated in Fig. 3: 1) injection timing signal is sent to the microprocessor for synchronization, 2) the BGCG is programmed with new DC bias data, and 3) addressed FIFO is loaded with new data. These actions are transparent to the normal mode of operation of the function generator as described above.

IV. CONCLUSION

The design of an arbitrary function generator for the APS injector synchrotron correction magnets is based on the staircase approximation of line segments that describe the desired function. The attributes of the segments rather than the point values themselves are stored in first-in-first-out (FIFO) memories This scheme results in a simple hardware implementation that is appropriate for applications requiring a large number of these units.

V. REFERENCES

[1] Kuninori Endo, " Minicomputer Assisted Function Generator for the Dynamic Control of Chromaticity Correction Sextupoles", IEEE Transactions on Nuclear Science, Vol. NS-26 No. 3, June 1979