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TRIGGERING THE LBL TIME PROJECTION CHAMBER

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Abstract

We have built a fast digital trigger for the LBL Time Projection Chamber (TPC) installed in the PEP-4 detector at SLAC. The TPC is an innovative High Energy Physics detector which will provide particle identification from dE/dx information within the tracking volume. The TPC trigger uses discriminator signals from 2,220 dE/dx wire channels to require a track of ionization in the TPC which originates from the colliding beam intersection region. The trigger processing is performed as the ionization drifts onto the proportional wires and is completed 17 μs after beam crossing. In this report, we describe the basic operation of the TPC detector and its trigger; a pretrigger which uses prompt TPC information from the endcap region; and the electronic implementation. The trigger can be tested with realistic simulated patterns of ionization deposits in the TPC which are stored in local memories. We show test results from electronic simulations and first results of a test with cosmic rays.

Introduction

The TPC[1,2,3] is constructed in a 2 m diameter, 2 m long cylindrical high pressure vessel, filled with Argon-Methane. A high voltage central membrane and graded field cage establish a uniform electric field which drifts ionization axially by up to one meter to the TPC endcaps in about 16 μs (Fig. 1). A uniform magnetic field parallel to the electric drift field provides momentum measurement, and will reduce transverse diffusion. Each of the TPC endcaps has six sectors subtending 60 degrees in azimuthal angle (Fig. 2). Each sector uses a grid wire plane to separate the drift and amplification regions, and a proportional wire plane with 185 sense wires at 4 mm spacing. The sense wire signals which provide tracking and dE/dx information are sampled and stored in Charge Coupled Devices, and are simultaneously compared to a computer controlled threshold for use in the trigger. The ground plane under 15 selected wires is segmented into 1200 cathode pads (7.5 mm by 8 mm) to measure the curvature of charged particles. These channels are also recorded by CCD's. There are a total of 16,000 channels each of preamplifier, shaping amplifier, CCD and digitizer for the TPC.[4]

The timing of signals from the TPC scales with the drift velocity of electrons in the gas. For the design of the trigger, we use the expected maximum drift velocity of about 6 cm/μs. At this drift velocity, the maximum drift time would be approximately 16 μs and the trigger processing would be completed within 17 μs. At the PEP storage ring, the electron and positron bunches collide every 2.44 μs. We use a pretrigger to select beam crossings of possible interest within 2 μs and leave about 500 ns for clearing the analog systems if no pretrigger is generated. A track of ionization will drift onto the TPC endplane with drift time proportional to its axial coordinate (labeled z in Fig. 1). Tracks which pass through the endcaps or pass within about 12 cm of the endcap provide prompt signals for the pretrigger decision. We use external drift chambers located inside the inner (20 cm) radius and outside of the outer (100 cm) radius of the TPC along with the prompt TPC signals to generate the pretrigger. The Inner Drift Chamber (IDC) and its use in the pretrigger is described in Reference 5.

After a pretrigger is generated, the TPC wire signals are used to search for a continuous track of ionization which extends from the outer to the inner radius of the TPC and which terminates within a time window of about 3-4 μs duration ending at 16 μs (see TS signal shown in Fig. 1). The requirement of a continuous track rejects random hits in the chamber which, for example, would be generated by synchrotron radiation. The time window requires that the track originate from the beam intersection region (z ~ 25 cm) and will suppress beam-gas scattering and stray electron backgrounds. We expect to operate with a pretrigger rate of about 1 KHz corresponding to a trigger decision dead time of about 1.5%. A trigger rate of 1-2 Hz is expected. The TPC CCD readout time of 20 ms will result in an electronics deadtime of about 5 .

Trigger Logic

The 2220 TPC sense wire signals are compared to a computer programmable threshold at the output of the shaper-amplifier. The unreshaped discriminator output signals from sense wires of adjacent sectors are ORed together to form six overlapping super-sectors to allow for curvature of the charged particles in the magnetic field (Fig 2). We divide 184 ORed signals for each supersector into 23 groups of eight. Each group of eight signals is tested for a majority logic decision. A majority logic decision requires a number of wires greater than a computer controlled threshold to be hit within a 1-2 μs time window. For example, ionization from a track making a 30 degree angle with the beam direction will drift onto the lowest wire of each group about 1 μs after the highest wire; if four or more wires are hit a majority logic unit is set. These majority signals are used to generate pretrigger and trigger decisions.

A timing signal (labeled TF in Fig. 1) limits the pretrigger decision to less than 2 μs. A programmable mask is used to select which majority units can combine with the external IDC to generate a pretrigger. The masks select a minimum track angle for triggering by enabling only radial groups above a selected radius. Two 30 degree sections of the IDC are combined with each supersector in forming the angular coincidence of the IDC and the TPC. The Outer Drift Chamber is combined with the inner chamber to generate pretriggers for large angle tracks.

Two types of trigger have been retained. One, the ripple trigger, follows and checks the continuity of the track by requiring a succession of majority units with each unit enabling lower radius signals.

The ripple is initiated by ionization drifting to the outer radius of a sector for which no enable is required, or by charged particles exiting the detector through the endcaps above the minimum radius selected by the pretrigger mask during the pretrigger time. In the rippling process each radius enables three lower radii in order to allow for missing hits due to the physical gap between sectors. The rippling is required to terminate at one of the two lowest radial groups and to arrive in coincidence with a timing signal (labeled TS in Fig. 1) which selects tracks which originate from the beam intersection region.

The rippling process will reject tracks with improper timing (e.g., incorrectly inclined tracks) and also tracks with angles greater than 84 degrees due to the enabling requirement and propagation delays. To trigger on these large angle tracks, a second trigger was designed to trigger on charged particles which make an angle of about 90 degrees with the beam direction. This trigger counts the number of majority units which are hit in a variable time window about the beam crossing region. If there is a majority of the majority units hit, then the TPC majority trigger is satisfied.

Electronic Implementation

The trigger is the only pattern-sensitive subsystem of the PEP-4 electronics. While the Inner and Outer Drift Chamber parts of the trigger are almost time independent and process simple patterns, the TPC part of the trigger is more complex. The large number of input variables, their time dependence, the processing which is performed and the testing of this processing requires special consideration.

The principal characteristics of the dE/dx wire trigger design are:

1. Synchronous operation - It is practically impossible to thoroughly check a random logic system with several thousand input variables changing state for 16 μs. One way to "eliminate" the "time dimension" is to synchronize these variables to a master sequencer that controls the processing. Dividing the drift time to the end-caps into 64 time slices and processing within each time slice, eliminates the random nature of the processing.

2. Test capability - An embedded test system provides extensive, time dependent test pattern capability. Test patterns which simulate real tracks or generate unique scope displays are stored in random access memories under computer control and are read out during a test by the master sequencer (synchronous testing). Figure 3 displays a test pattern of an ideal event with five tracks and some synchrotron radiation background which has been used to test the electronics.

3. Control memories - Each board processing the incoming data has been fitted with random access memories. These memories sample the data passed to downstream boards in synchronization with the master controller for every time slice. The data stored in these memories are read out into a computer which verifies that the processing of the current board is performed correctly and then uses these data to define the test pattern which was fed to the next downstream board. These memories made possible the use of a single test injection point per wire for the entire system and allows a playback for real events using the test pattern injection. The memories provide a storage capacity of 11K, 32 bit wide words and can be viewed as an embedded logic analyzer with a 4 MHz clock frequency (Fig. 4). This logic analyzer can be used to locate defective circuits to within a few packages.

4. Computer control - Parameters which are part of the processing, such as thresholds, masks and pulse widths are computer controlled. These parameters include test pattern data arrays and look-up tables.

5. On-line software - A real time interactive software package has been written to:

a) Set any of the trigger parameters to the appropriate value and to verify their setting.

b) Handle the trigger interrupt and to read the trigger data from the TPC Large Data Buffer List.

c) Process trigger data and perform failure checks.

d) Display data from any level of processing.

e) Generate realistic test event patterns and later to playback real events using the data recorded in the trigger memories.

Description of the Trigger Generation

The functions performed by the trigger logic have been described above and their implementation in hardware is now addressed. Signals from both endcaps are processed in parallel. Each has a separate master sequencer which is synchronized to the central timing system of the PEP-4 experiment. For each endcap, three bins process the incoming data while a fourth controls the sequencing and reads out the data recorded in the local memories. Each processing bin is controlled by a sequencer satellite. This unit, using sequencing signals from the master controller and computer set parameters, generates all clocks required for a synchronous operation of the bin.

Majority Logic Generation

The majority logic signals, Mi,j,n, are generated when the processing of a radial group, n , consisting of 8 wires in endcap i and supersector j finds a preset minimum number of triggered wires within certain time requirements adjusted to trigger on an element of a track. Inputs from the dE/dx wires (Wi,2j,l) are at first multiplexed with test inputs (T_1), ORed sector with sector, then synchronized to the master sequencer (Fig. 6). Synchronizing flip flops that are set are reset as their content is transferred to synchronized storage. Double buffered storage allows processing overlap and time multiplexed processing. Time multiplexing of a processing function between two sectors has the advantage of decreasing the package and I/O pin count and of allowing the comparison of data processing in demultiplexed and multiplexed parts of the circuit.

Each wire must maintain its information for a duration which depends on the radius of the wire signals being processed. As the system is synchronous, duration is defined as an integer number of clock periods. A clock period of 250 ns is the duration increment. Let Δ be the time duration, for a given

radius, expressed in multiples of the clock period. The number of wires triggering during each time slice is encoded and added to the sum of the number of wires triggered during each of the past Δ time slices. The number of wires triggered Δ time slices earlier is subtracted from the sum, then comparing the resultant to a threshold number yields a Mi,j,n signal.

Let k be a time slice number, $0 \leq k \leq 63$ R_{k-1} be the number of wires triggered during the Δ time slice periods prior to time slice k (ending at the beginning of k); and N_k be the number of wires triggering during time slice k, then:

$$R_k = R_{k-1} + N_k - N_{k-\Delta} \qquad (1)$$

This relation is true only for $k \geq \Delta$. For $k < \Delta$, $N_{k-\Delta} = 0$, and therefore:

$$R_k = R_{k-1} + N_k \qquad (2)$$

The time slices with $k < \Delta$ are said to be in the accumulation period. At the end of each time slice R_k is compared to a threshold number, Tn. If the resultant is greater than this threshold, then the corresponding Mi,j,n signal is set true.

The processing is handled in the hardware by the association of a PROM encoder, a FIFO memory to store the $N_{k-\Delta}$ and an eight bit arithmetic unit with output data registers (Fig. 6). (Since two supersectors are being time multiplexed on the same function operator, double storage must be provided to store the R_k numbers.) The threshold value is stored in both storage registers of the arithmetic unit prior to beam crossover. The number of wires triggering is subtracted from the stored threshold and relations (1) and (2) are replaced by:

$$R_k = R_{k-1} - N_k \quad \text{for} \quad k < \Delta \qquad (3)$$

with the initial value of $R_{k=-1} = Tn$, and

$$R_k = R_{k-1} + N_{k-\Delta} - N_k \quad \text{for} \quad k \geq \Delta \qquad (4)$$

If $R_k < 0$, the most significant bit of the arithmetic unit is set to 1. Therefore, the comparison is made by subtraction and a Mi,j,n will be issued if a negative number is detected in the arithmetic unit. An example is illustrated in Table 1. Timing for the process is shown in Fig. 5. Each arithmetic unit, AU, processes two supersectors corresponding to supersectors $2j$ and $2j+1$ on a time multiplexed basis. Propagation delays and access times determine the sequence by which the operations take place.

R_{k-1}	is available in the AU output register
$+N_{k-\Delta}$	is executed first (for $k \geq \Delta$) and loaded in the register
$-N_k$	is executed and loaded in the register

The sequencer is then repeated for the other supersector in the second half of the time slice (Fig. 5).

TPC Pretrigger Generation

The endcap pretrigger uses prompt TPC ionization information arriving within 2 μs of the beam crossing as determined by the TF timing window (Fig. 1). Majority logic decisions are ANDed with a mask which is used to define the minimum trigger angle, combined with the Inner Drift Chamber information and then the supersectors are ORed to generate the TPC endcap pretrigger, that is:

$$\text{IDC TPCF} = \text{TF} \sum_{i=0}^{1} \sum_{j=0}^{5} (A_{2j-1} + A_{2j}) \sum_{n=0}^{22} \text{Mask}(n)\, M_{i,j,n} \qquad (5)$$

where the A_j are obtained for an OR of the individual trigger logic for five cells of the inner chamber and cover 30 degrees of azimuthal angle. The indices i,j,n refer to the endcap, supersector and radius, respectively. Figure 7 includes a block diagram of the pretrigger logic.

Ripple Trigger Generation

Any majority logic decision, $M_{i,j,n}$, may initiate a ripple trigger during the pretrigger time if it is enabled by the pretrigger mask. The highest radii $M_{i,j,n}$ can initiate a trigger at any time. Each radius enables the next three lower radii for a 2-3 μs time window to continue the ripple. If this ripple signals propagates down in radius to the lowest radii within a time window TS, see Fig. 1, a ripple trigger will be generated. That is:

$$R_{i,j,n} = (\text{TF Mask}(n) + \sum_{k=n+1}^{n+3} R_{i,j,k})\, M_{i,j,n}\, F_n \qquad (6)$$

where $R_{i,j,k} = 1$ for $k > 23$, and the F_n are digital retriggerable one shots with a time duration which is radius dependent. The trigger logic is:

$$\text{TPCS} = \text{TS} \sum_{i=0}^{1} \sum_{j=0}^{5} (R_{i,j,0} + R_{i,j,1}) \qquad (7)$$

The logic is sketched in Fig. 7.

TPC Majority Trigger Generation

The majority trigger requires a minimum number of majority logic units to be set within a time window, TM, which is 3-4 μs wide ending at 16 μs. The logic divides each supersector into three sections of eight majority logic units each (that is, 64 wires). The logic can be written as:

$$\text{TPCM}_{i,j} = \prod_{k=0}^{2} \text{Majority}\,(M_{i,j,n})\Big|_{n=8k}^{8k+7} \qquad (8)$$

and

$$\text{TPCM} = \text{TM} \sum_{i=0}^{1} \sum_{j=0}^{5} \text{TPCM}_{i,j} \qquad (9)$$

The implementation of this trigger is shown in Fig. 8.

Test results

We have generated a number of patterns to test the trigger using the RAM test injections. Figure 9 displays the TPC trigger input data recording for the test pattern of Fig. 3, which had been loaded into the test RAM. The test data of Fig. 9 were recorded in the trigger memories during the drift-time, then read-out into the computer through the TPC readout system. The readout checks the test injection, data recording and readout electronics. Note that some test input signals (bits) are lost because of the one clock period deadtime of the trigger electronics (e.g. 2 bits for the steepest track where synchrotron background points were close to the track). The majority logic decisions for this simulated ideal event is shown in Fig. 10. The 1 μs width of the pulses is determined by the coincidence window programmed. The pretrigger mask and timing pulse, TF, are shown. The two smallest angle tracks in this example would generate a pretrigger since the highest radius majority decision is above the minimum radius determined by the mask. Tracks at smaller angles would not generate pretriggers nor initiate ripple triggers.

The ripple trigger is sampled at nine radial locations arranged in groups of three. The ripple trigger recording for this test event is shown in Fig. 11. The wide 3 μs window used to enable lower radii signals tends to merge the track information. The final trigger decision is an OR of the lowest two radii, ANDed with the collision point timing signal, TS. The origin of the tracks is required to be within about 30 cm of the beam collision point by the requirement that the rippling reaches the lowest radii within the TS time window.

The TPC majority trigger encodes the number of majority units which have turned on in each clock period for groups of eight and then latches them during the time window, TM, shown in Fig. 12. The memories on the TPCM trigger board record the encoded number and the n out of eight majority decision. The boxes in Fig. 12 count the number of units on and are shaded when the number exceeds the threshold of 4/8 which had been set. The final trigger decision requires that each group exceed threshold during the TM time window.

A test of the TPC concept has been performed using cosmic rays. The test included two of the TPC sectors, the high voltage and the electronics system. Figure 13 shows a recording of a cosmic ray in the trigger input data memories. In this event, the cosmic ray knocked out a delta ray as it passed through the TPC from large radius and long drift times to small radius and shorter drift times. The track is seen here after drifting almost 1 m to the TPC endplane. The majority logic decision processing for this event was recorded and found to be correct. We will continue with cosmic ray testing before moving the TPC into the colliding beams at PEP.

Conclusion

A TPC trigger has been built using 130 boards containing close to 10,000 IC's and occupying over eight bins. We have written Monte Carlo programs to study the operation of the trigger for the expected jet events in e+,e- annihilation. We have developed realtime software to load test patterns to check the electronics and to display the results. Although the trigger has not been tested under colliding beam conditions, we are confident that the built-in flexibility and programmability, as well as its large data reservoir will allow us to adapt it easily and rapidly to any additional requirements imposed by the real operating environment.

Acknowledgement

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4. R.C. Jared, D.A. Landis, and F.S. Goulding, "Analog Signal Processing for the Time Projection Chamber", to be published in the IEEE Trans. Nucl. Sci. NS-29, No. 1 (1982).

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TABLE 1

Illustration of Mijn Generation

Parameters T_n = 4 - threshold of 4 hits

Δ = 3 - time window of 3 clock counts

	Time slice	N_k	Operations	Register at end of time slice	M i,j,n
Δ	k=0	$N_0 = 0$	4 - 0	4	0
	1	$N_1 = 0$	4 - 0	4	0
	2	$N_2 = 1$	4 - 1	3	0
	3	$N_3 = 2$	3 - 2 + N_0	1	0
	4	$N_4 = 3$	1 - 3 + N_1	-2	1
	5	$N_5 = 2$	-2 - 2 + N_2	-3	1
	6	$N_6 = 1$	-3 - 1 + N_3	-2	1
	7	$N_7 = 0$	-2 - 1 + N_4	1	0
	8	$N_8 = 0$	1 - 0 + N_5	3	0
	9	$N_9 = 0$	3 - 0 + N_6	4	0
	10	$N_{10} = 0$	4 - 0 + N_7	4	0

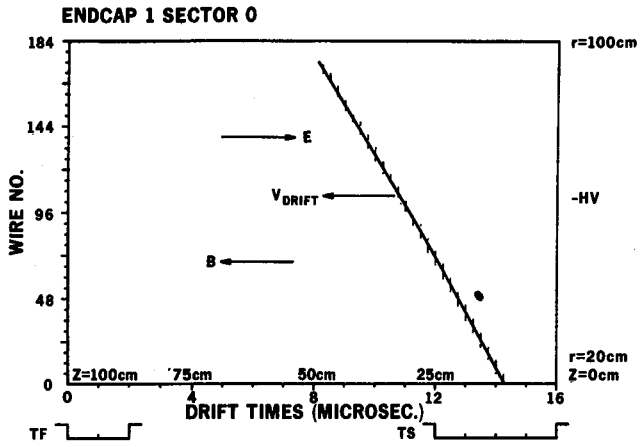

Fig. 1 Side view of one sector at one end of the TPC.

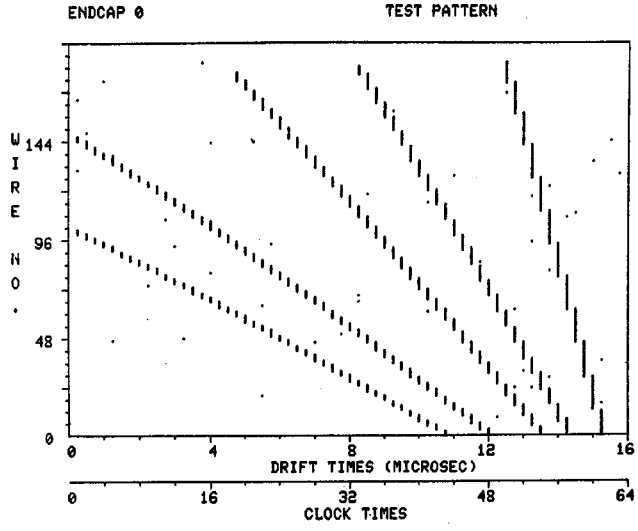

Fig. 3 Test pattern - five tracks with background.

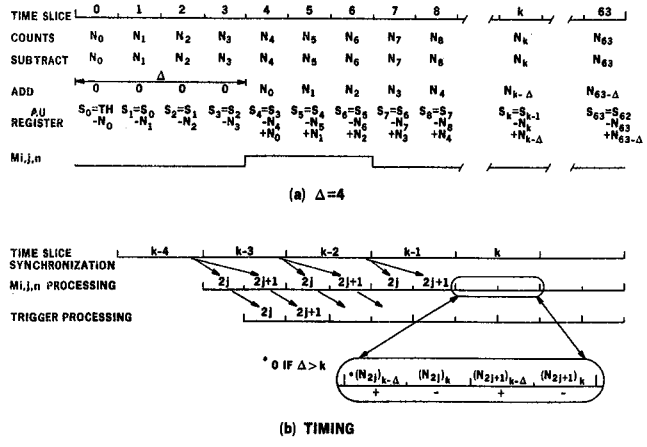

Fig. 5 Timing diagram for Mi,j,n generation.

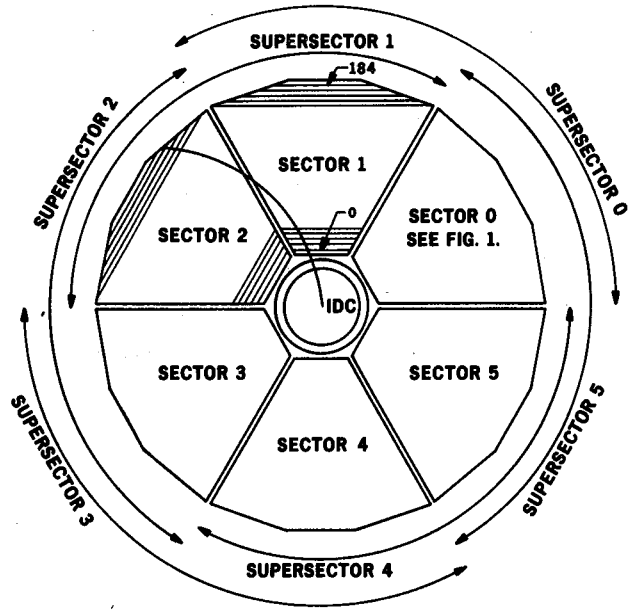

Fig. 2 End view of the TPC illustrating supersector definition.

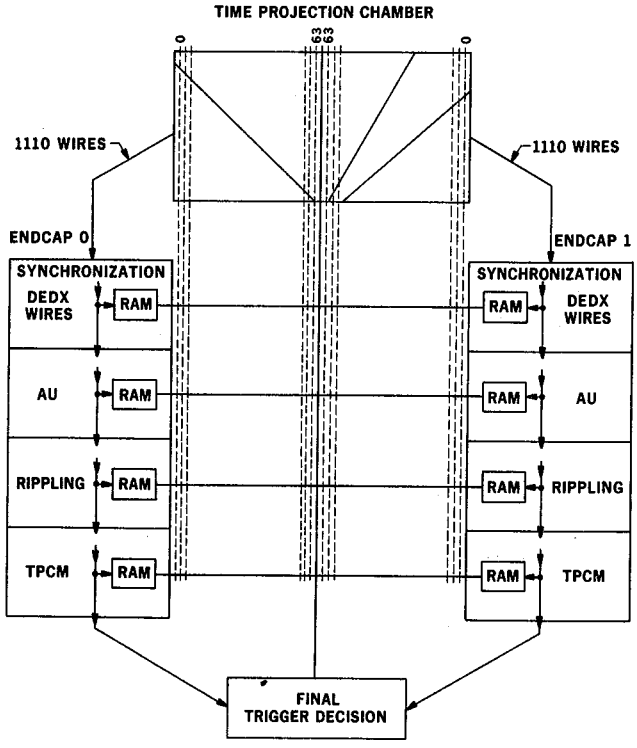

Fig. 4 Basic dE/dx structure.

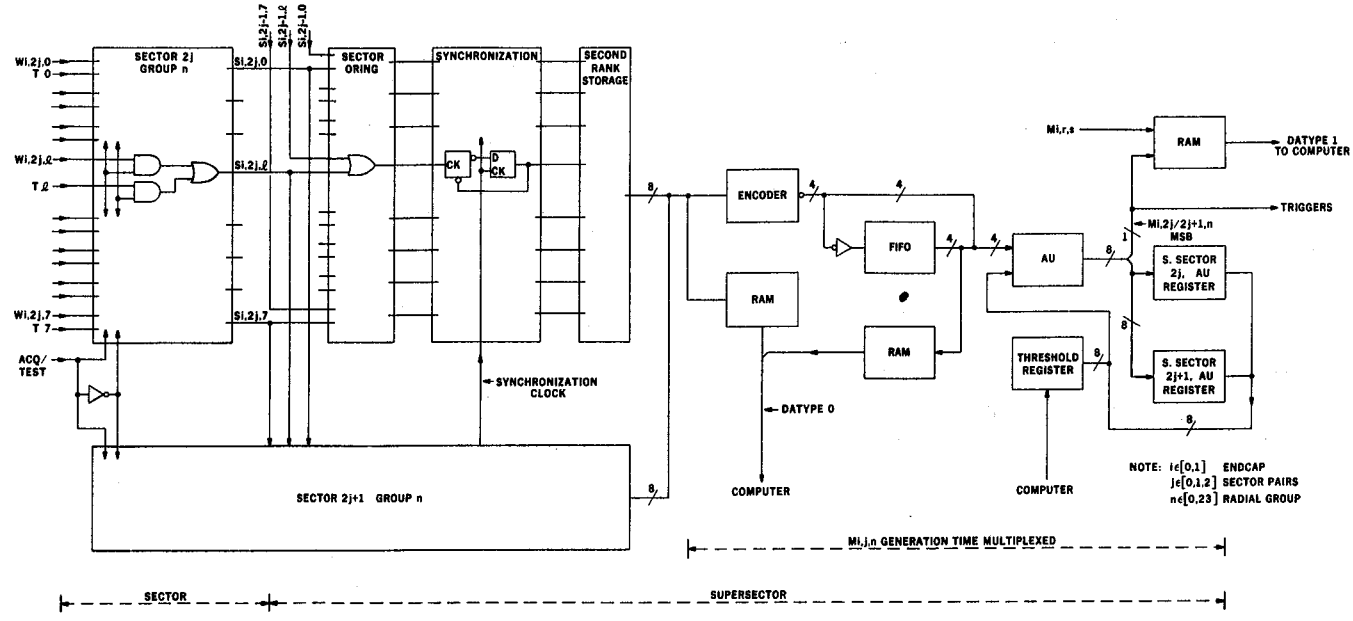

Fig. 6 Mi,j,n Generation.

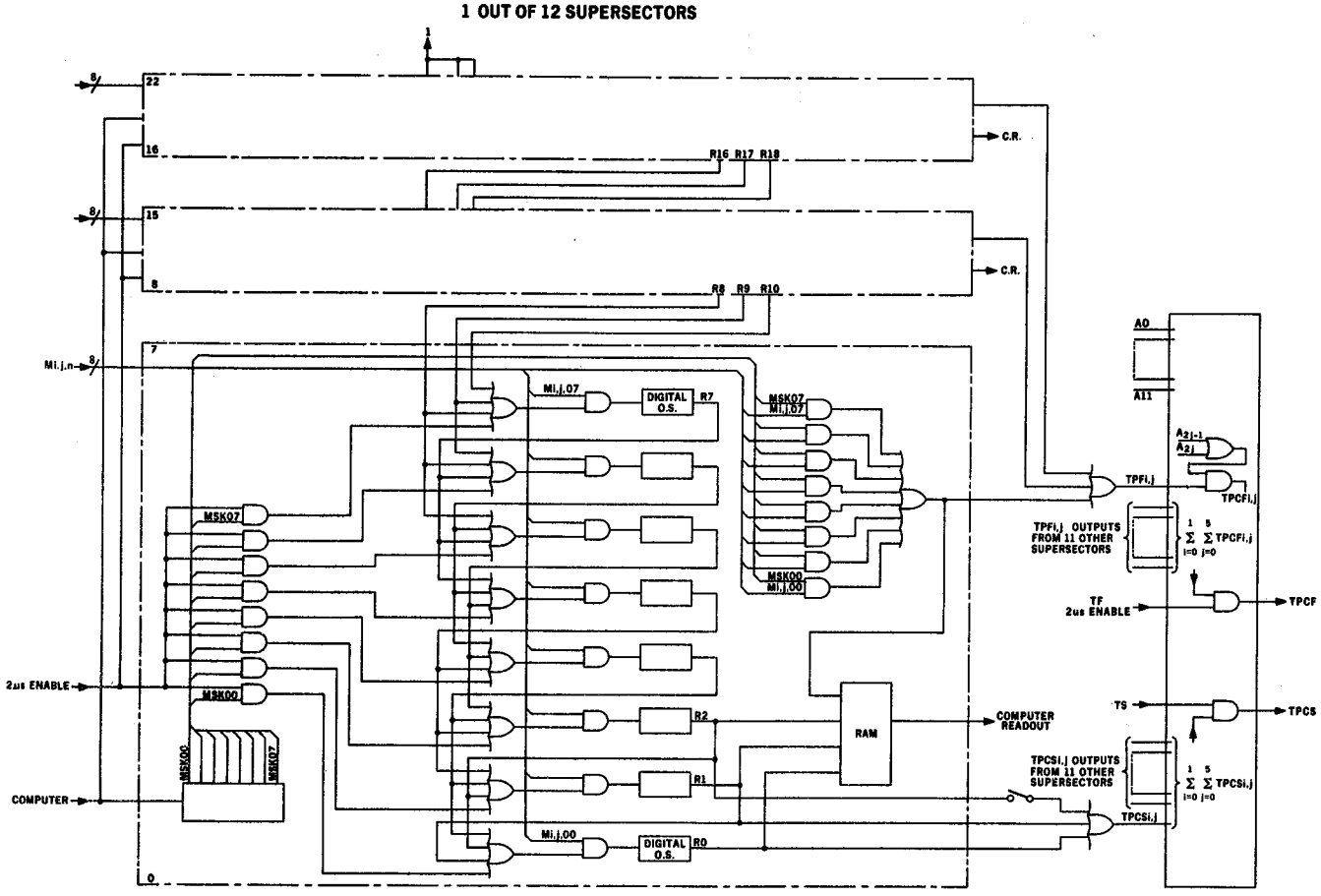

Fig. 7 TPC Pretrigger and Ripple Trigger.

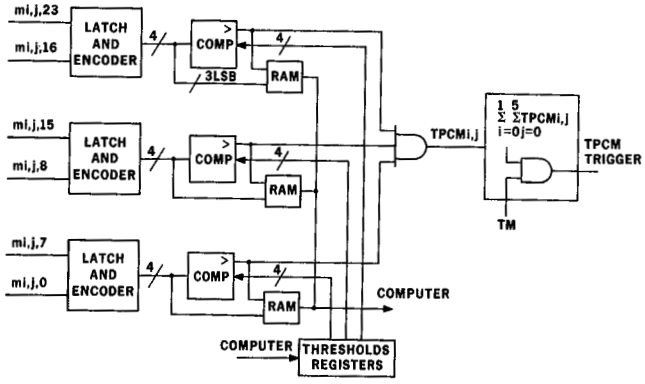

Fig. 8 TPC Majority trigger (one sector shown).

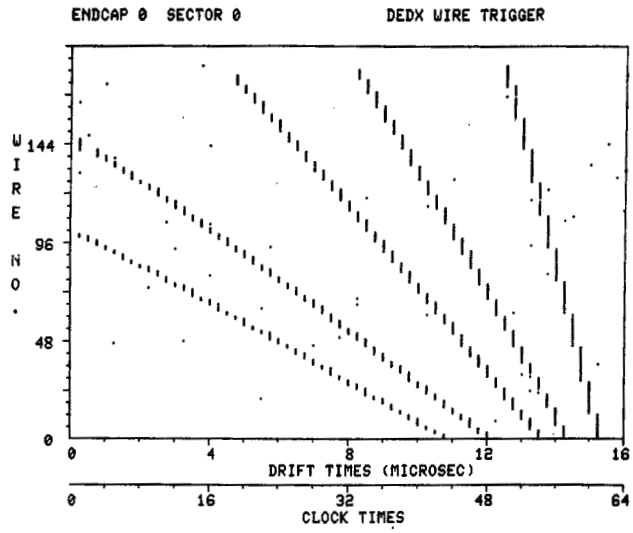

Fig. 9 dE/dx wire input recording for simulated event.

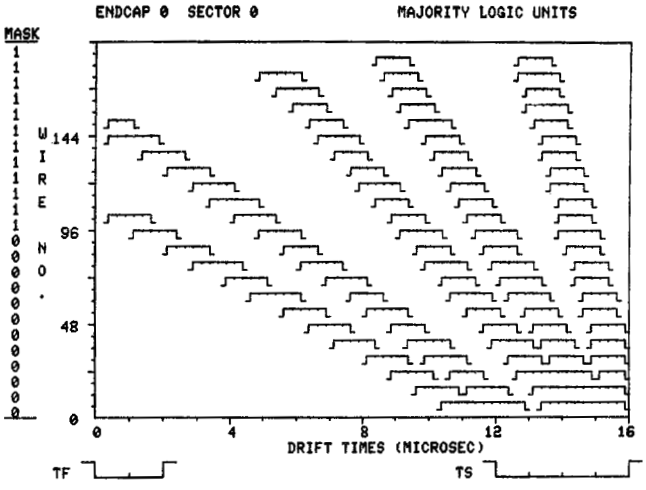

Fig. 10 Majority logic signal recording for simulated event.

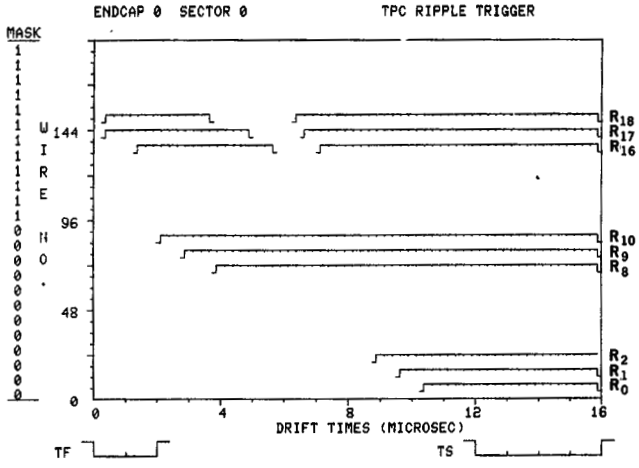

Fig. 11 Ripple trigger recording for simulated event.

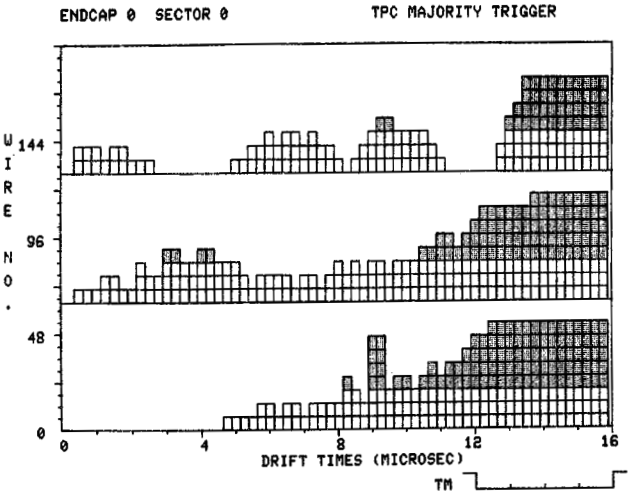

Fig. 12 TPC Majority trigger recording for simulated event.

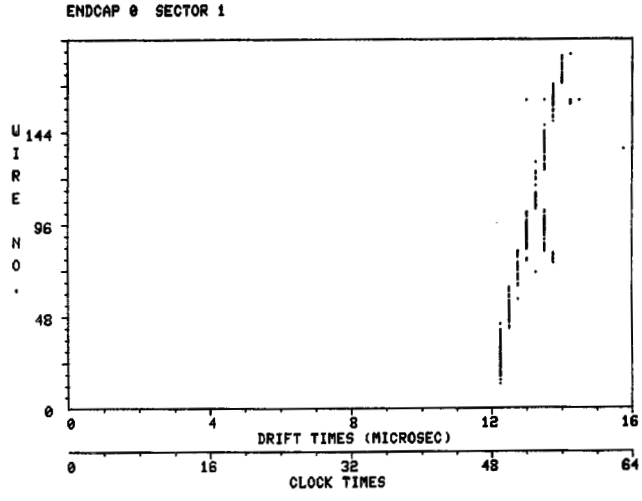

Fig. 13 dE/dx wire input recording for cosmic ray event.