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MPS II DRIFT CHAMBER SYSTEM AND RELAVENCE TO ISABELLE EXPERIMENTS*

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The MPS drift chamber[1] structure is shown in Figure 1 along with relevant performance numbers. Modules containing 5 or 7 anode readout planes are distributed throughout the 15 by 6 by 4 foot magnetic field volume of the MPS. Figure 2 is a typical high voltage curve for these drift chambers indicating a very broad region of stable operation. The drift time vs. position is shown in Figure 3 showing a very linear time vs. position relationship.

A complete module has 3 X-measuring planes and 2 Y-measuring planes (Figure 4). Three of these modules also have $\pm 30^{\circ}$ to Y cathode strip readout for 3 dimensional track reconstruction. All of the amplifier-shaper-comparator and digital delay-register electronics are on printed circuit boards mounted right on the chamber. The frames of the chamber planes are made of an extruded fiberglass-polyester pultrusion, the die for which shapes the O-ring grooves, reliefs, etc. to the precise dimension desired (Figure 5). This material is unusually stiff for a plastic (6×10^6 psi) which makes tensioning the wires relatively easy.

In the course of planning MPS II extensive computer modeling of Monte Carlo generated events was undertaken to find the optimum module configuration and module placement. Figure 6 is a scale plot of the 7 drift chamber modules and the 4 triggering PWC's placement for the physics planned in Exp. 747.[2] To better appreciate the pattern recognition problems, Figure 7 is the same event with a greatly expanded vertical scale. The X's are anode wire hits and the vertical bars are the drift times. The pattern recognition fitted straight lines through the local triplets and then circles to the straight lines. To evaluate the effectiveness of this pattern recognition technique, 100 Monte Carlo events were generated and then messed up by randomly removing 4% of the hits, then adding 4% noise hits. A track was considered found when > 70% of its hits were found and the correct point slope identified for 90% of those found hits. With this criteria, the efficiency for finding low mass $\phi\phi$ events was 93%, which increases to 96% at a mass of

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3 GeV. This efficiency is a great improvement over that obtained with the original MPS spark chambers.

Central to the development of MPS II was the successful design and production of 3 custom IC's, one of which is a truly state-of-the-art device. Figure 8 is a block diagram of the electronics mounted on the drift chamber. A more complete description of it is given in the section on wire chambers in this document. Detailed specifications of the 3 micro circuits is shown in Tables I, II and III.

Several features of this drift chamber system should be mentioned as to their relavence to Isabelle experiments. Because of the short drift distance, no time vs. distance correction need be made for angle or magnetic field effects. Also the short drift distance allows operation at high rates. Since the electronics is deadtimeless, the physics of the avalanche formation process sets the only rate limitation. The electronics converts the time information to digital at the earliest possible stage and there are no needs for offset time, time vs. distance slope or slope linearity corrections on a wire to wire basis. Thus large systems will be manageable. If finer time resolution is required, the shift register can sample as quickly as 3 ns intervals. The shift registers can be cascaded to achieve sample storage greater than 256 bits or they could be stagger-clocked to achieve time resolution as short as 1 ns.

The electronics for large drift chamber systems (100 K wires) could be built for $10 to $20 per channel using these microcircuits. Thus with the successful operation of MPS II we believe that we will have demonstrated a viable solution to the tracking detector requirements of Isabelle.

REFERENCES

1. A. Etkin, IEEE Transactions on Nuclear Science Vol. NS-26, No. 1, 54-58 (1979).
   A. Etkin and M.A. Kramer, IEEE Transactions on Nuclear Science, Vol. NS-27, No. 1, 139-144 (1980).
   S. Ozaki, MPS Note #51, 1979.
2. AGS Proposal #747, A High Statistics Study of ϕ and $\phi\phi$ Production from π^- p and K^- p Interactions at 22 GeV/c (1979).

FIGURE CAPTIONS

LIST OF TABLES

Anode wires	0.001" diam. goldplated tungsten
Field + cathode	0.003" diam. S.S. (Nitronic 50)

Drift field > 7KV/cm

Drift velocity 1 mm/20 ns - fully saturated

Maximum drift time - 60 ns

Figure 1

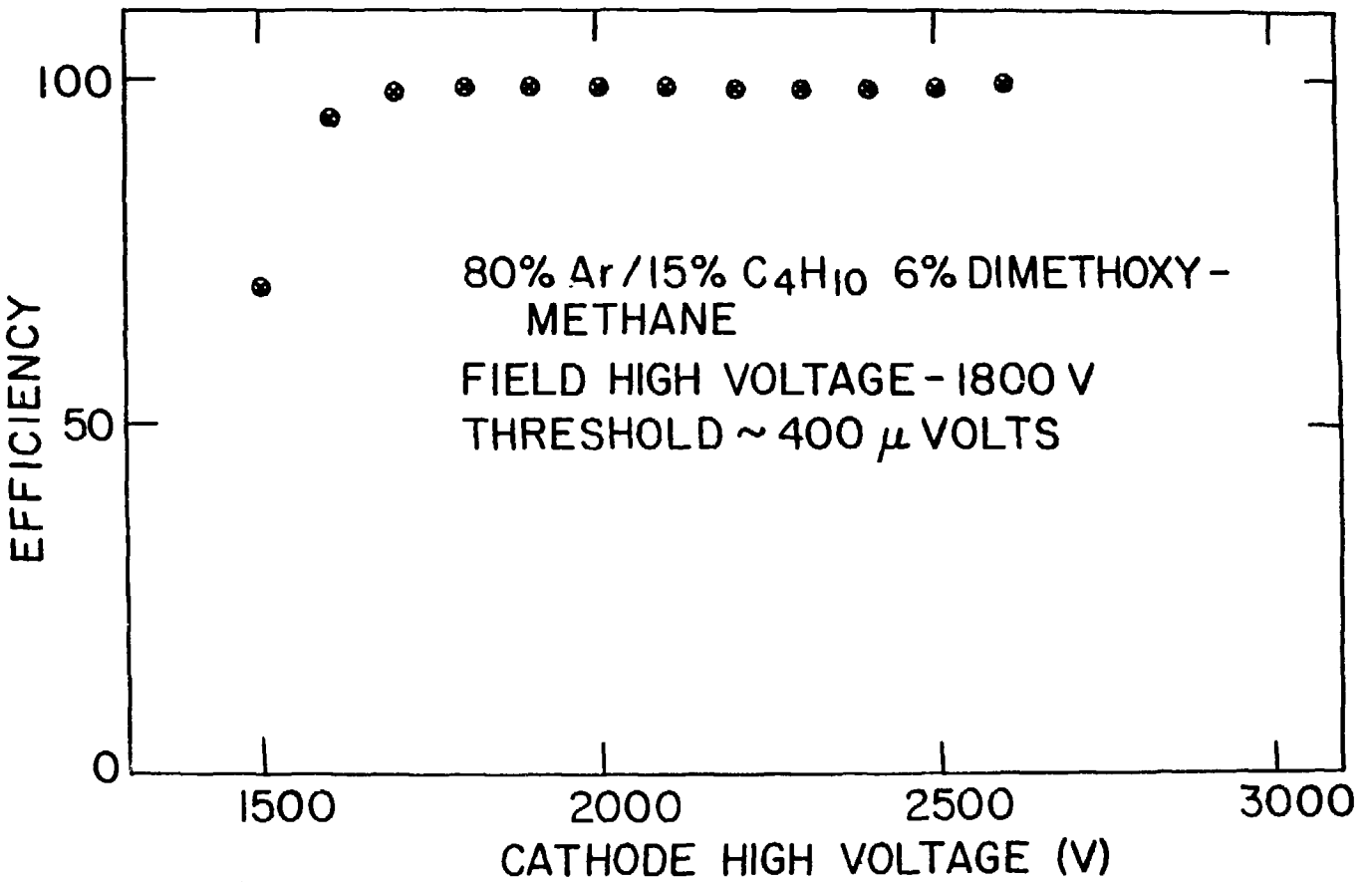

100
50
0
EFFICIENCY
80% Ar / 15% C_4H_{10} 6% DIMETHOXY-METHANE
FIELD HIGH VOLTAGE - 1800 V
THRESHOLD ~ 400 μ VOLTS
1500
2000
2500
3000
CATHODE HIGH VOLTAGE (V)

Figure 2

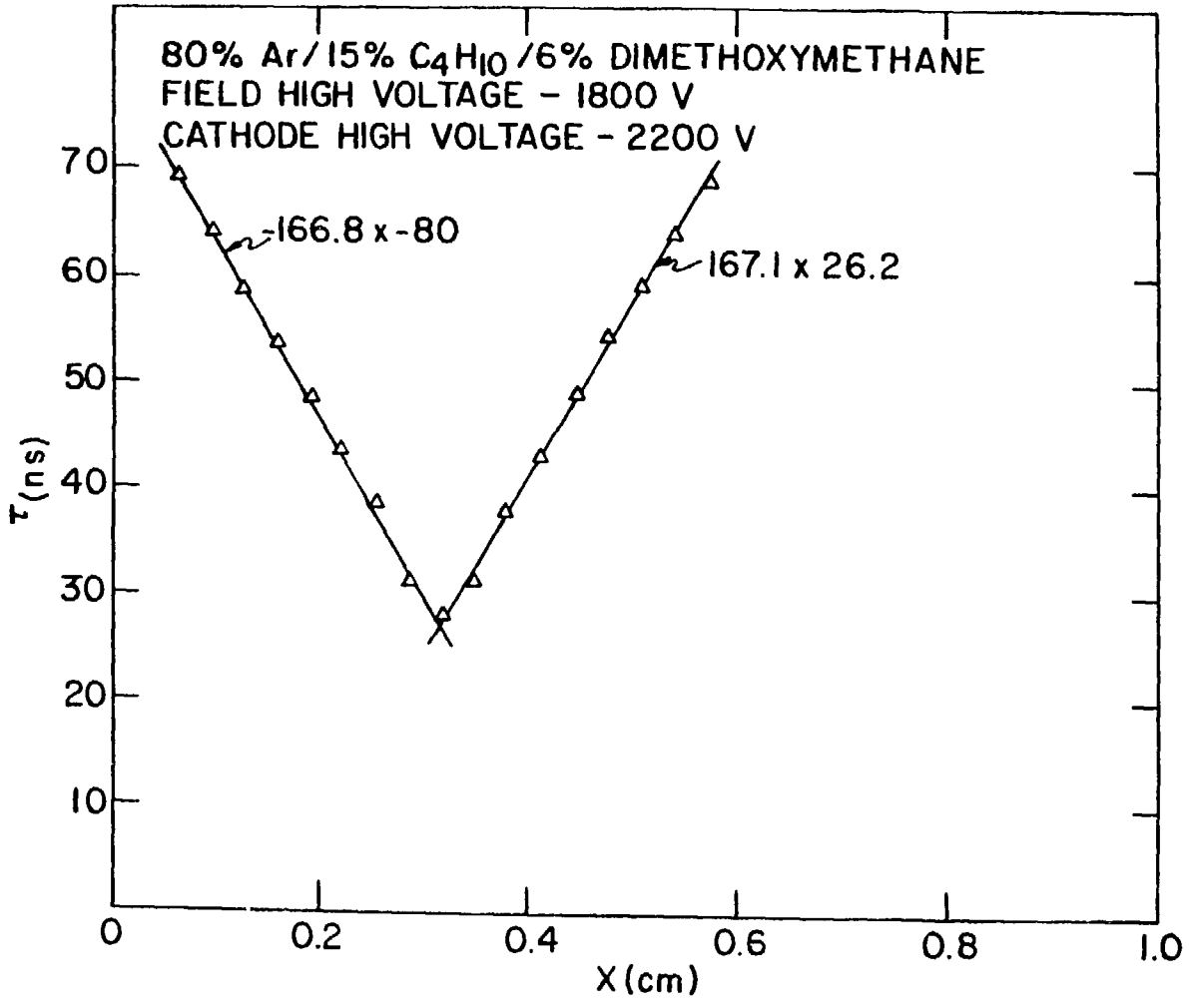

80% Ar / 15% C_4H_{10} / 6% DIMETHOXYMETHANE
FIELD HIGH VOLTAGE - 1800 V
CATHODE HIGH VOLTAGE - 2200 V
-166.8 x - 80
167.1 x 26.2
τ (ns)
70
60
50
40
30
20
10
0
0.2
0.4
0.6
0.8
1.0
X (cm)

Figure 3

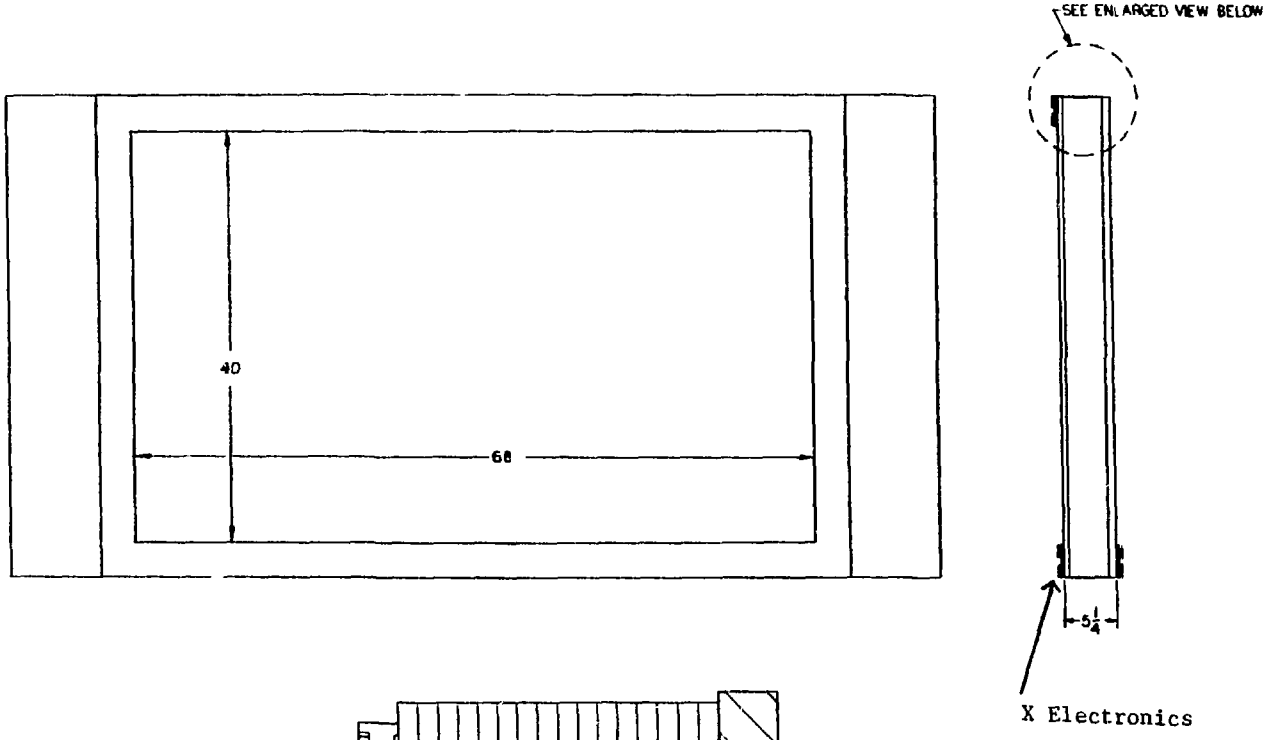
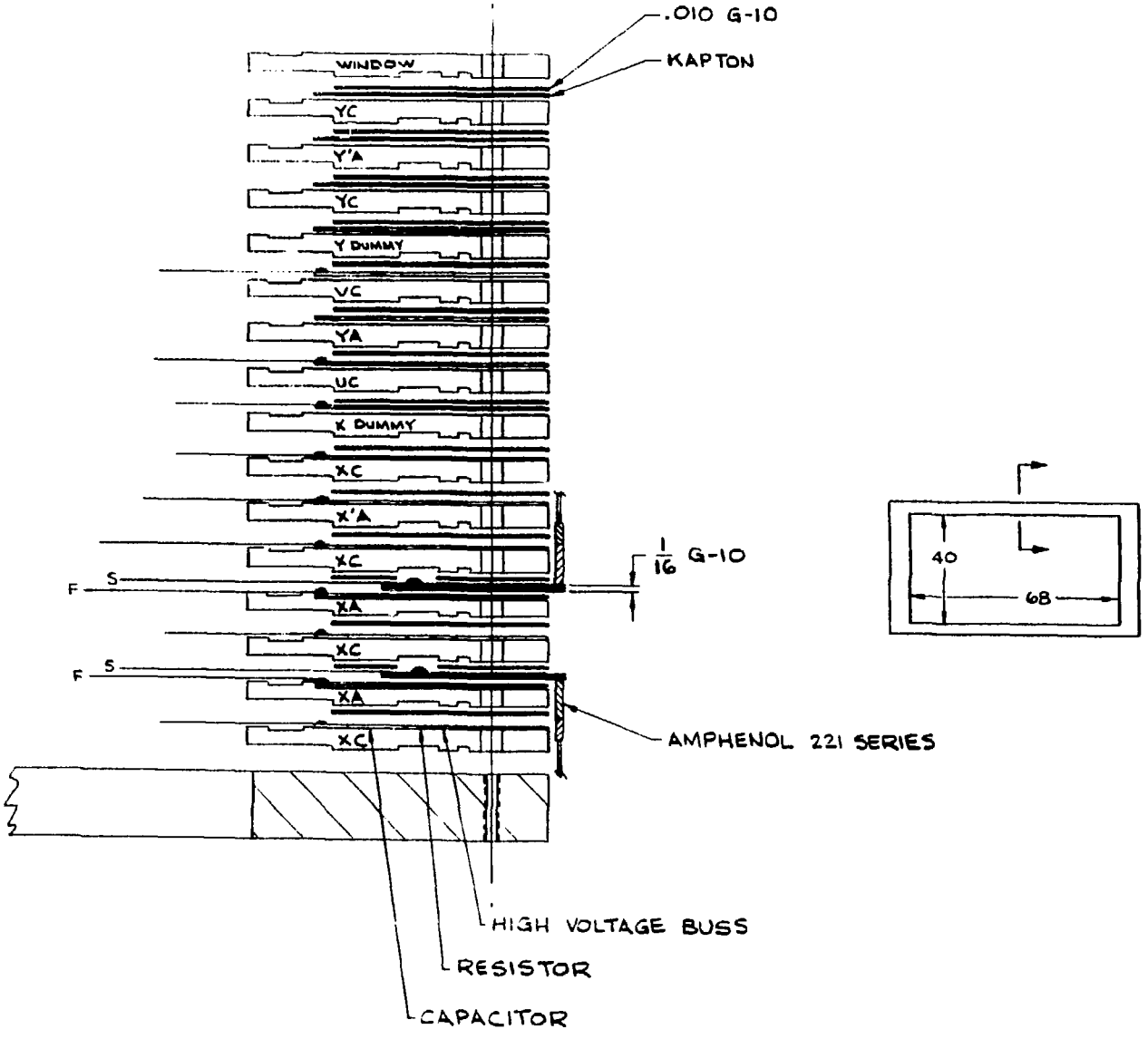


Figure 4


.010 G-10
KAPTON
WINDOW
YC
Y'A
YC
Y DUMMY
VC
YA
UC
X DUMMY
XC
X'A
XC
F
S
XA
XC
F
S
XA
XC
1/16 G-10
AMPHENOL 221 SERIES
HIGH VOLTAGE BUSS
RESISTOR
CAPACITOR
40
68

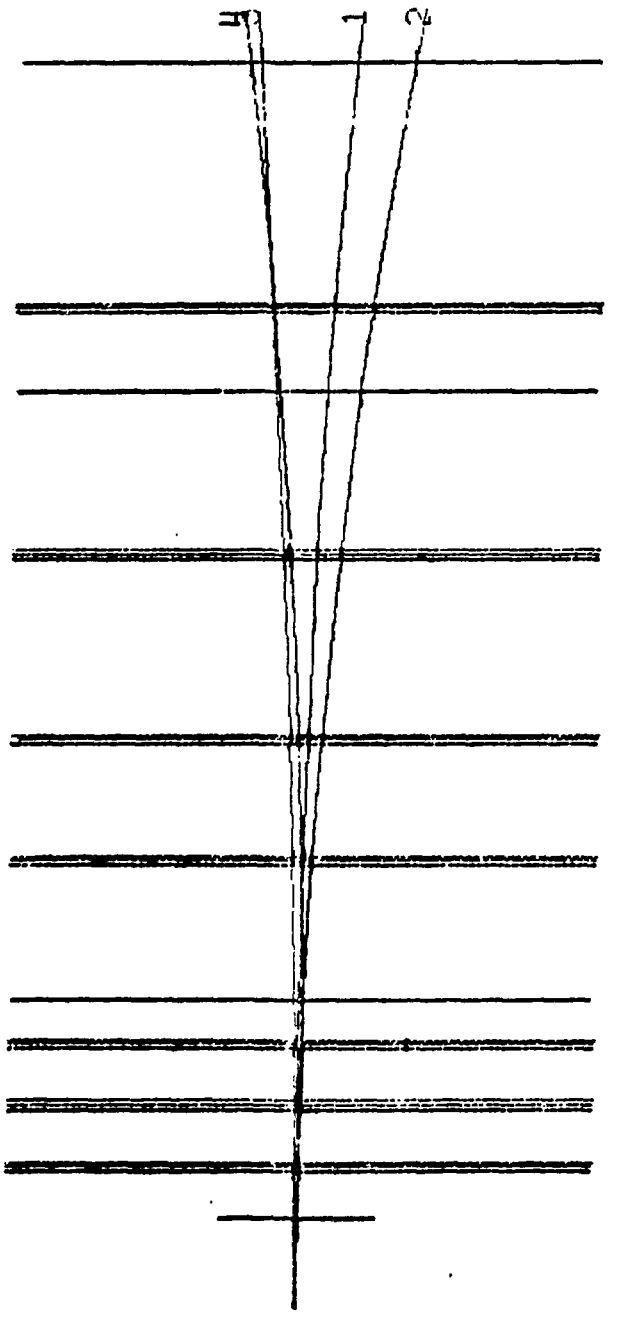


Figure 6

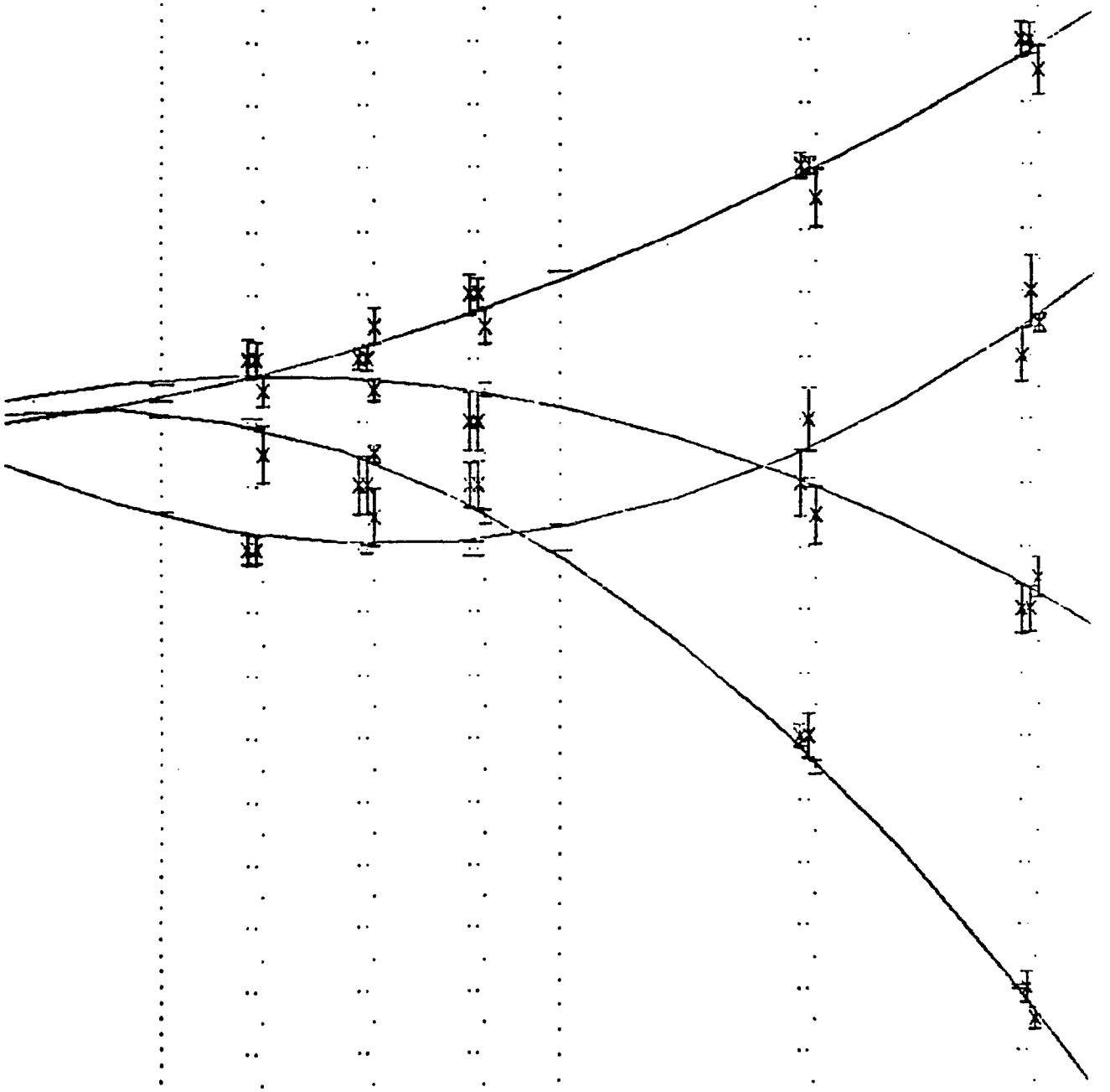


Figure 7

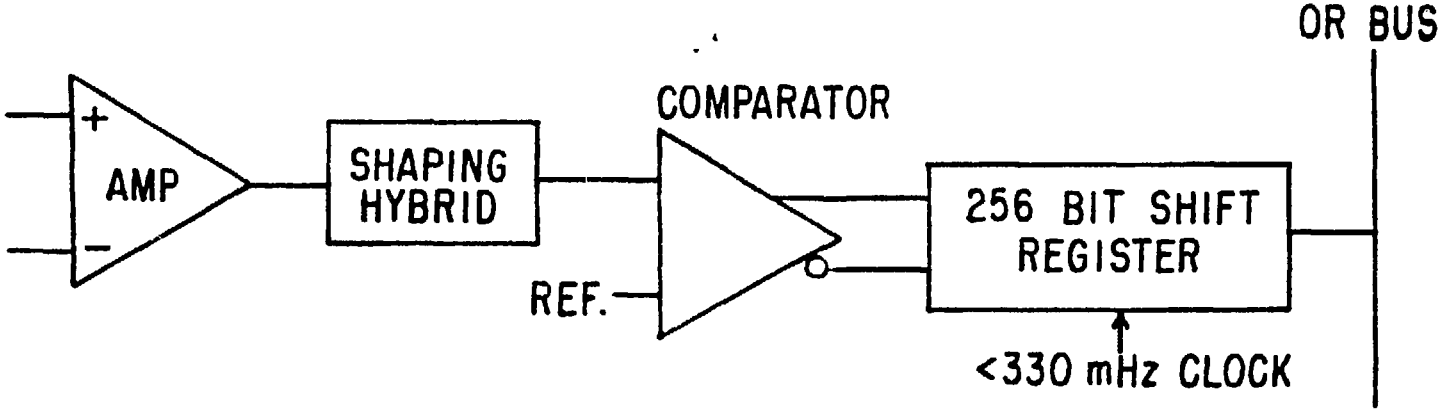

OR BUS
COMPARATOR
+
AMP
−
SHAPING
HYBRID
256 BIT SHIFT
REGISTER
REF.
<330 mHz CLOCK

Figure 8

Table 1

BNL TRA401

AMPLIFIER CHARACTERISTICS

Characteristics	Minimum	Maximum	Units	Remarks
Input Type	True Differential			
Input Noise (RMS)		0.25	uA	8 nsec integration time constant.
Input Resistance		80	ohms	
Input Protection		1.13×10^{-4}	J	47 pF charged to 2.2 kV.
Transfer Impedance	20		Kohms	
Delta Transfer Impedance	-10%	+10%		Lot to lot mean within lot.
Gain Stability		0.25	%/°C	
Output Impedance		50	Ohms	
Rise Time		4.4	nsec	
Max. Linear Output	1.2		Volts	
Propagation Delay		10	nsec	
Delta Propagation Delay		1.5	nsec	Applies to amplifiers on common chip
Temperature Range	0	50	°C	
Supply Currents				
+5.5 V		65	mA	
-2.5 V		45	mA	

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Table 2

BNL MVL400
DISCRIMINATOR CHARACTERISTICS

Characteristics	Minimum	Maximum	Units	Remarks
Input Resistance	3		Kohms	
Input Z Threshold Control	1.5		Kohms	
Threshold Control Range (1:1)	0	1.5	Volts	
Threshold Hysteresis	6	10	mV	
Threshold Match		±5	mV	Applies to disc. on common chip.
Crosstalk between Inputs of Channels		-40	dB	
"0" Logic Level		1.8	Volts	Driving 100 ohm pull-down resistor to +1.5V.
"1" Logic Level	+3.5		Volts	Driving 100 ohm pull-down resistor to +1.5V.
Output Response Time		4.4	nsec	Driving 100 ohm pull-down resistor to +1.5V.
Slewing		3	nsec	For 2 to 20X threshold.
Double Pulse Resolution		20	nsec	
Input Capacitance		6	pF	Each comparator input.
Propagation Delay	14.5	17.5	nsec	
Operating Temperature	0	50	^{o}C	
Supply Currents				
+5 V		200	mA	Including current in 100 ohm pull-down resistors.
-5 V		22	mA	Including current in 100 ohm pull-down resistors.

Table 3

Clock speed	0 to > 330 HHz
Ch to Ch phase to phase delay NS clock	< 1 ns
Readout delay NS clock	40 - 60 ns
Max readout speed	40 MHz
Vcc	5 ± 5 V
Power at 250 MHz	160 mw