Fermi National Accelerator Laboratory

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Performance of the CAMEX 64 Silicon Strip Readout Chip

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Introduction

The CAMEX64 is a 64 channel full custom CMOS chip designed specifically for the readout of silicon strip detectors. CAMEX which stands for CMOS Multichannel Analog MultiplEXer for Silicon Strip Detectors was designed by members of the Franhofer Institute for Microelectronic Circuits and Systems and the Max Planck Institute for Physics and Astrophysics.

Each CAMEX channel has a switched capacitor charge sensitive amplifier with 4 sampling capacitors and a multiplexing scheme for reading out each of the channels on an analog bus. The device uses multiple sampling capacitors to filter and reduce input noise. Filtering is controlled through sampling techniques using external clocks. There are no on board discriminators and there is no data sparsification. The device operates in a double correlated sampling mode and therefore cannot separate detector leakage current from a charge input.

Normal operation of this device is similar to all other silicon readout chips designed and built thus far in that there is a data acquisition cycle during which charge is simultaneously accepted on all channels for a short period of time from a detector array, followed by a readout cycle where that charge or hit information is read out. During the readout cycle, data acquisition ceases until the readout is complete.

This device works especially well for colliding beam experiments where the time of charge arrival is accurately known. However it can be used in fixed target or asynchronous mode where the time of charge arrival is not well known. In the asynchronous mode it appears that gain is somewhat dependent on the time interval required to decide whether or not to accept charge input information and thus the maximum signal to noise performance found with the synchronous mode may not be achieved in the asynchronous mode. All data presented in this paper is for operation in the synchronous mode.

General Operation

A single channel representation of the CAMEX chip is shown in Figure 1. Input charge is integrated by an inverting charge sensitive amplifier (CSA1). The signal at the output of CSA1 is sampled by switches S1 to S4 and capacitors C1 to C4. Charge sensitive amplifier CSA2 is used to sum the information from the different sampling paths.

Operation in the synchronous mode is best described by examining the timing diagram shown in Figure 2 which shows a group of BEFORE samples and a group of AFTER samples. A data acquisition cycle begins with the charge sensitive amplifier reset switches R1 and R2 closed to remove integrated charge from the feedback capacitors Cf1 and Cf2. CSA1 is made active by opening R1. After R1 is opened and while R2 is still closed, switches S1 through S4 are closed in sequence for a short period of time and then opened to store the difference voltage between the output of CSA1 and the input to CSA2 along with the instantaneous noise voltage at the output of CSA1 on capacitors C1 through C4. When the BEFORE samples are completed, R2 is opened and input charge, Qin, arrives causing the output of CSA1 to shift. (After the BEFORE samples, Qin could arrive before R2 is opened without any difference in performance.) AFTER samples are then taken. The AFTER samples are accomplished by toggling S1 through S4 as was done for the BEFORE samples. When a switch such as S1 is closed, the signal at the output of CSA1 is amplified by the ratio of the capacitors C1/Cf2 and stored as voltage on Cf2. Also stored on Cf2 is the noise at the output of CSA1 (times the capacitor ratio) at the instant S1 is opened. Since the input to CSA2 is a virtual ground, the output voltage of CSA1 is stored on C1. When each of the remaining switches S1 through S4 is toggled, more charge is transferred to Cf2. Each time one of the sampling switches is opened, a different noise voltage is stored on Cf2. The noise voltages add according to an RMS relationship and give a lower overall signal to noise than if a single sample is used. (Each AFTER sample directly increases the output signal. Each AFTER sample causes the magnitude of the output noise to increase, but not as much as the signal increases. Thus the overall signal to noise is improved.)

The noise performance of this circuit is dependent on the time between each of the BEFORE samples and each of the AFTER samples. This time is known as the sampling time. (The sampling time as far as noise is concerned is the time difference between <u>opening</u> the sample switches, not the closing of the switches.)

Noise performance is also dependent on the time between groups of BEFORE and groups of AFTER samples. As the groups of samples get further apart, low frequency components of noise can appear as a signal at the output of CSA1 which are then sampled and add directly to the output noise.

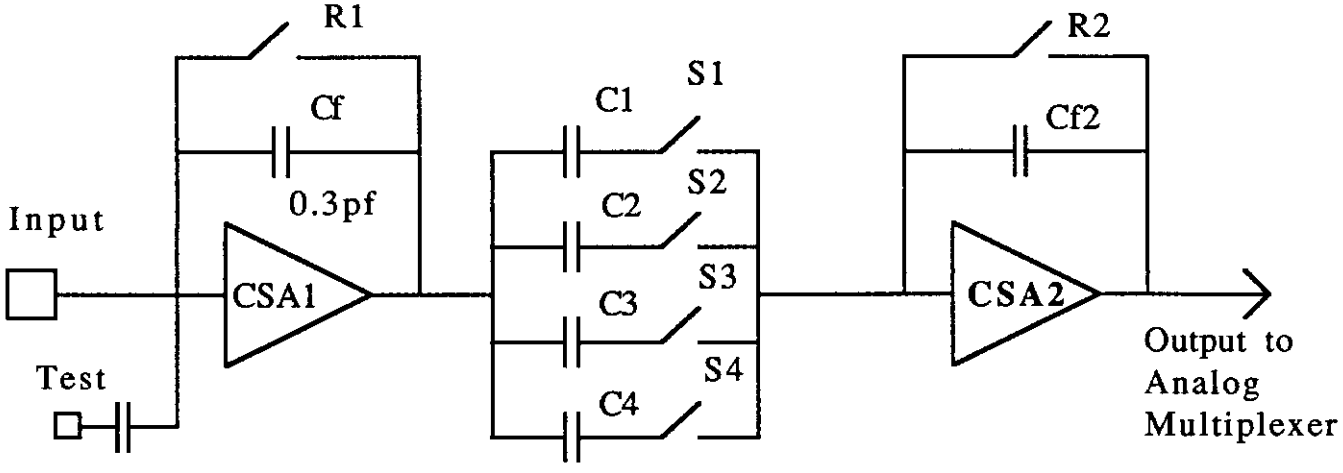


Figure 1 - Single Channel Circuit Diagram

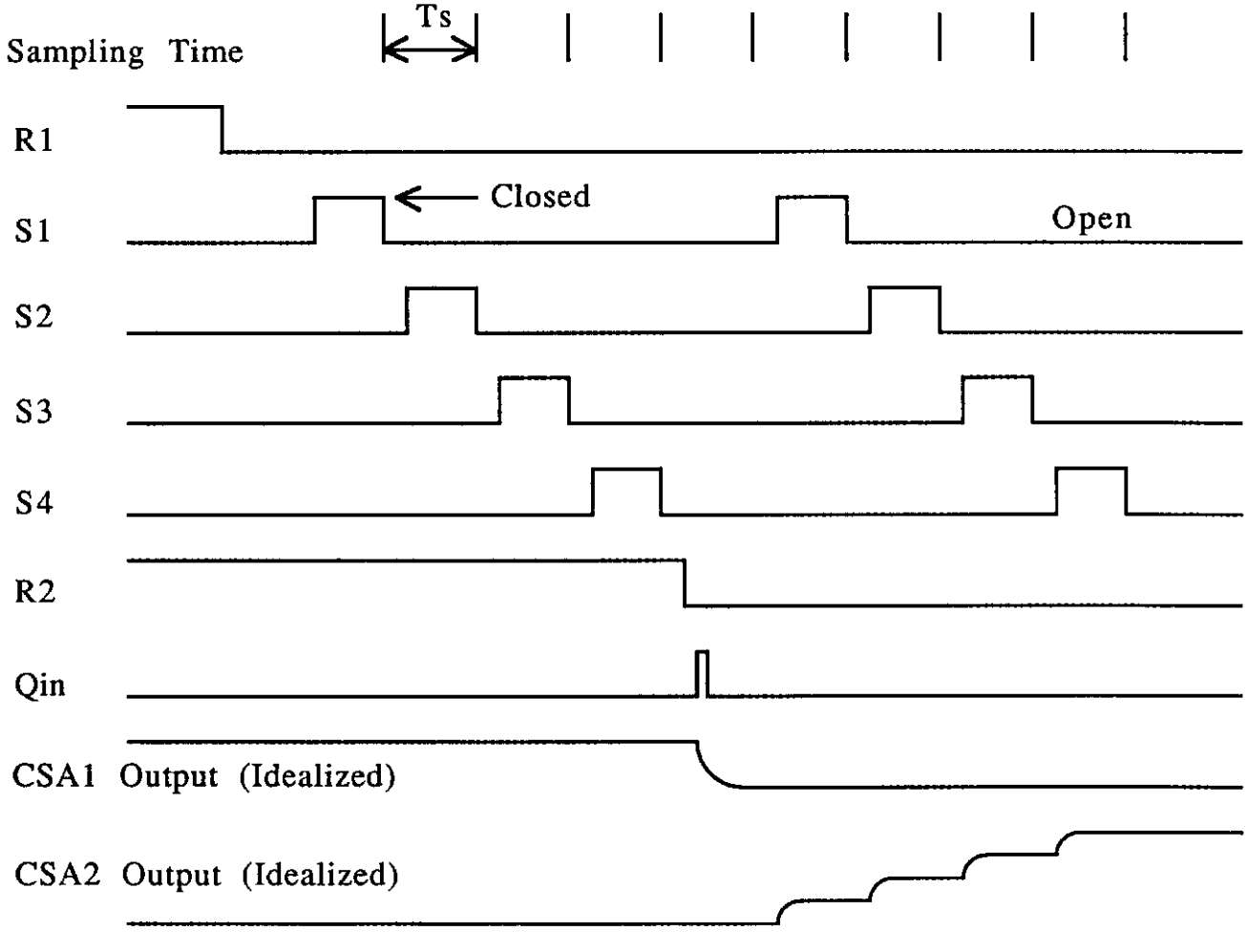


Figure 2 - Synchronous Application Timing Diagram

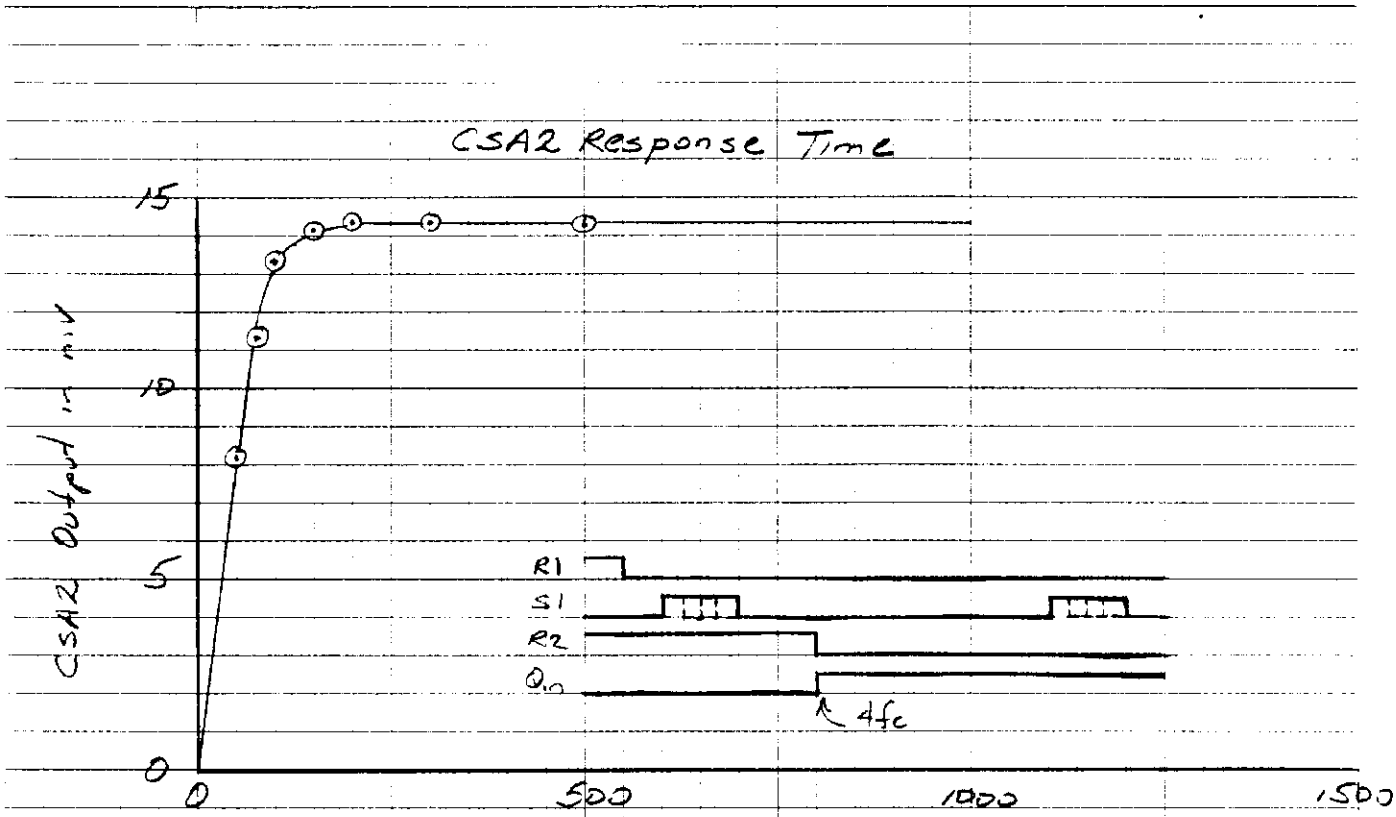
Practical Operating Considerations

In the proceeding section, the ideal response of the CAMEX chip was discussed. Due to bandwidth limitations within the device certain restrictions should be observed.

First, the switch closure times for S1 through S4 must be long enough to allow CSA2 to respond to the inputs from the different sampling switches. A test was done using a single sampling switch, S1, wherein the closure time was varied over a wide range. Figure 3, which is basically the response characteristic of CSA2, shows that for for long closure times, the output for a 4 fc input is 14.3 mv. The gain begins to decrease for closure times below about 150 ns and has fallen to 11.8 mv/4 fc for a closure time of 75 ns. The other sampling switches (S2-4) showed similar performance. At longer closure times, the gains of all the sampling paths is essentially the same. At very short closure times (50 ns), the gains of the the different sampling paths vary somewhat. To obtain maximum gain from the circuit, the closure times should not be less than 125-150 ns. If shorter times are used, a slightly reduced gain will be obtained for each sampling path resulting in a lower overall channel gain.

A second test was done where the sampling time was held fixed at 250 ns and the switch closure time was reduced from 200 ns to 50 ns. Under these conditions, the equivalent input noise remained about constant down to about 100 ns. At 50 ns closure times, the equivalent noise at the input had risen by about 40%, possibly due to jitter on the timing pulses and the associated fast rise time signals. It should be noted that for a given application if larger signal to noise exists than what is needed, and higher speeds are required, shorter switch closures are a possible trade-off.

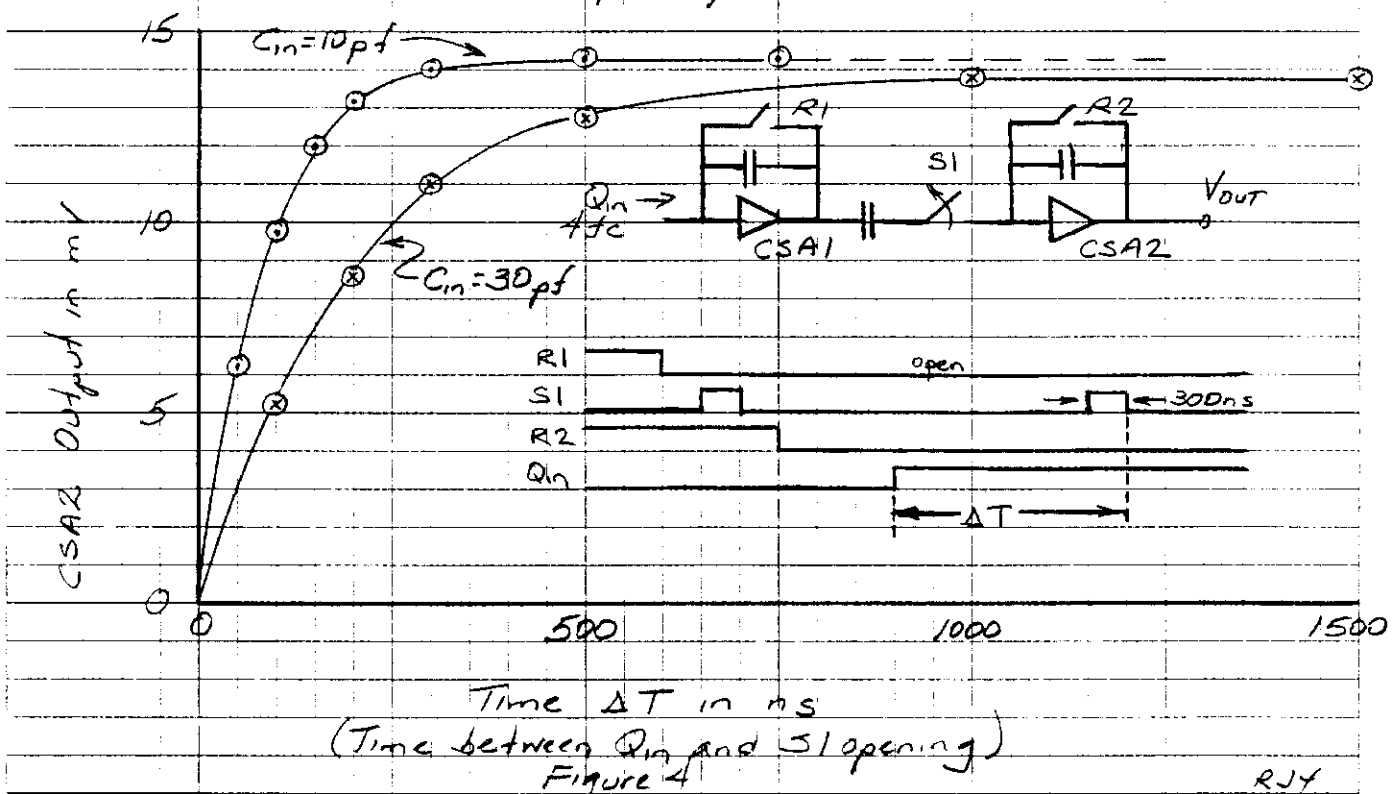
Another limitation is the time required for the integrator to respond to an input charge pulse. In Figure 2 this means that after the arrival of the Qin pulse, sufficient time must be allowed for the output of CSA1 to rise before the sampling switches S1-S4 are opened. Normally the sampling switches are toggled sequentially. Therefore if sufficient time is not allowed, the charge or signal to be transferred to CSA2 will be limited for the first switch closure (normally S1) with smaller effects on each succeeding switch closure. Later samples have the benefit of the delay between sampling pulses and therefore are less sensitive to the integrator rise time. The overall effect is that the RMS noise voltage at the output stays constant, the overall gain decreases and therefore the equivalent input noise increases. It is important to note that the rise time at the output of the integrator is dependent on the input capacitance. Therefore, the amount of time required after the arrival of Qin before opening S1 is dependent on the input capacitance if maximum gain and signal to noise is



Time S1 is Closed in ns

Figure 3

Integrator Response
vs.
Input Capacitance



Time ΔT in ns
(Time between Qin and S1 opening)

Figure 4

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desired. In some applications the reduced gain associated with short delay times and the resultant increase in S/N may be quite acceptable.

Another test using a single sampling switch (S1) was done where the time between Qin and opening S1 was changed for different input capacitances. Figure 4 shows the results of this test for two different input capacitances. Since the rise times which are observed are significantly slower than shown in Figure 3 for CSA2, the plots are basically the rise time of the integrator (CSA1) for different input capacitances. The plot also shows that there is a small gain difference for different input capacitances. This will be discussed more later.

There is a choice in the width of the sampling pulses compared to the sampling time. Based on the tests previously described, the switch closure times should be a large fraction of the sampling time. Additional tests have been done which show that closure times equal to the the sampling time have little or no effect on gain or noise. Sampling pulses which overlap, however, have been found to reduce gain and increase input noise and are not recommended.

Charge Injection Effects

Each of the switches, R1, R2, and S1-S4, injects charge into the charge amplifiers CSA1 and CSA2 under some conditions. It is interesting to look at these effects and their magnitude. Figure 5 shows a typical channel with a single sampling switch where the switches are drawn with their associated parasitic capacitances. A +/- 5V digital level controls each of the switches. Each time the digital control level for a switch changes, charge is injected through the parasitic gate-drain and gate-source capacitors into the circuit. In a normal timing pattern, the data acquisition cycle starts with R1 and R2 closed and S1-S4 open. In the first half of the data acquisition cycle R1 opens, injecting charge into CSA1 which results in an offset voltage at the output of CSA1. When each of the sampling switches closes and opens, this offset voltage is stored on the series coupling capacitor, removing this offset from further consideration during the rest of the cycle.

The second half of the data acquisition cycle begins when R2 opens. Charge is injected through the parasitic capacitors into the input and output of CSA2. Since the output of CSA2 is a low impedance, the injected charge only has an effect at the input to CSA2. Figure 6 shows the output of CSA2 changing by 51 mv in response to R2 opening. The charge injected by R2 in other channels and the resultant output offset appears uniform across the chip. After R2 is open, each of the sampling switches is again toggled. When a signal is applied to the gate of S1 and S1 is closed, charge is injected through the parasitic capacitance of S1 into CSA2 causing the output to shift negatively. When the switch is opened, the same voltage

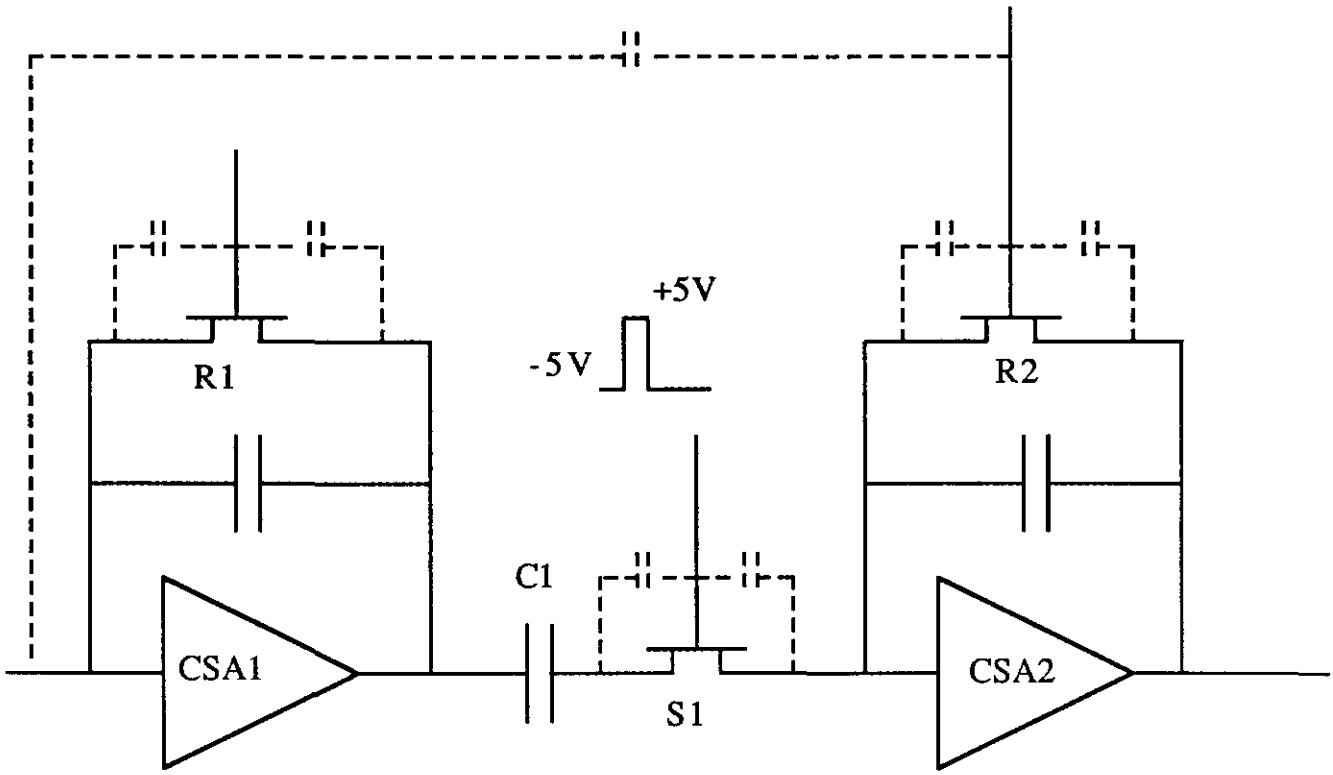
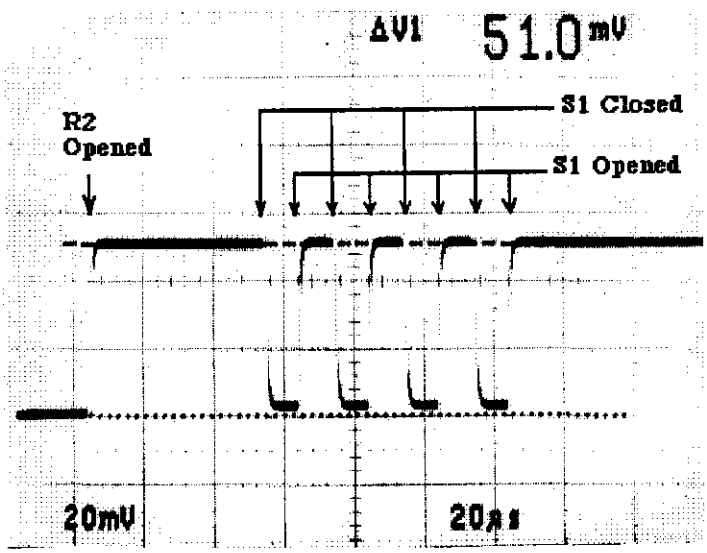


Figure 5 - Single Channel Parasitics



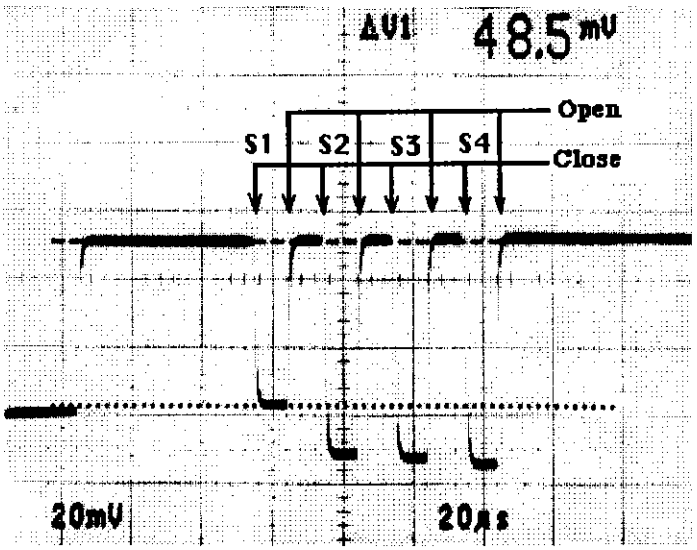
Note: R1 is closed. Charge injection from switch closing equals that from switch opening.

Figure 6 - Charge Injection Effects From R2 and S1

swing with opposite polarity appears on the gate of S1 and is coupled through the same parasitic capacitance to cause the output to return to exactly the same level as was present before S1 closed. Thus the charge injections from a sampling switch closing and opening exactly cancel. The second half of Figure 6 shows a 48.5 mv shift in the output of CSA2 due to S1 closing and opening repeatedly. While the sampling pulses in Figure 6 are very slow in order to clearly show the effect, the same cancellation takes place when the sampling pulses are fast. It is interesting to note that the magnitude of the shift seen at the output of CSA2 is different for different sampling switches on a given channel. Figure 7 shows each of the switches S1-S4 toggled sequentially and four different levels of injected charge corresponding to the four different switches. (S1 shift = 48.5 mv, S2 shift = 62 mv, S3 shift = 64 mv, S4 shift = 66 mv.) The shift for the same sampling switch on different channels however is essentially the same. (i.e. The injected charge for S1 on different channels is the same.) This is probably due to a layout difference between sampling switches which is repeated on every channel.

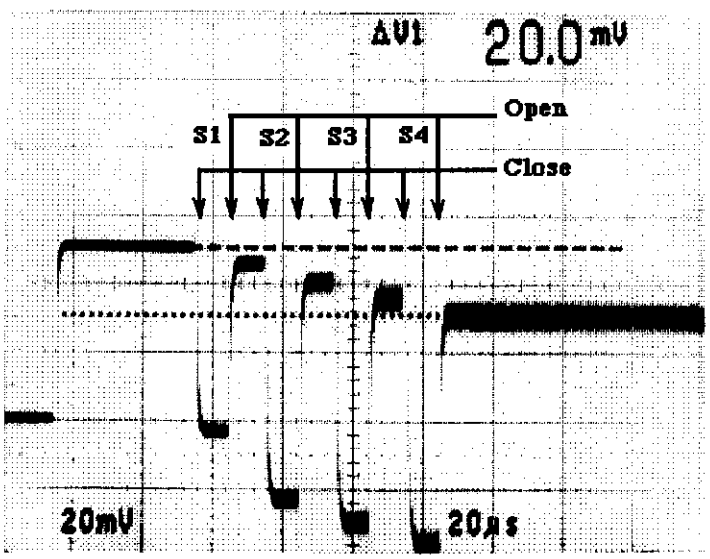
In the previous figures, the switch R1 was closed to better show the effects being described. In normal operation, R1 is open during the second half of the data acquisition cycle when R2 is opened. Under these conditions another parasitic effect appears. A parasitic capacitance apparently exists between the control line for R2 and the input to CSA1 as shown at the top of Figure 5. Figure 7 had shown that with R1 closed and R2 open, the output level of CSA2 remained unchanged when sampling switches S1-4 were closed and then opened. With R1 open this is no longer true. A parasitic capacitance appears to couple a small charge from R2 back to the input to CSA1. The coupled charge acts just like an input signal. Whenever one of the sampling switches is then closed, that signal is passed to the output in the form of a negative 5 mv step for each sampling switch as shown in Figure 8. Thus, the offset caused by opening R2 and injecting charge into CSA2 is actually canceled in part by the same switch opening feeding back through the input and subsequent closures of the sampling switches. (An obvious violation of Murphy's Law.) Assuming that the logic voltage swing is 10 volts, the required feedback capacitor is only 0.13 fF.

Most of the parasitic charge injection effects which exist have been shown to cancel or nearly cancel and cause no problems under normal operating conditions. However, if the device is operated in a nonstandard way, the charge injection effects could become more significant and cause problems. One example is as follows. If between the groups of BEFORE and AFTER sampling pulses, R2 is opened at the same time as S4 is opened, a large offset corresponding to about a 4 fc input appears at the output of CSA2 due to S4 opening. An understanding of the mechanisms present can help to avoid such problems.



Note: R1 is closed

Figure 7 - Charge Injection Effects From S1, S2, S3, and S4 With R1 Closed



Note: First open R1 and toggle S1-S4, then open R2 and then toggle S1-4.

The output shifts by -5 mv/sampling switch.

Figure 8 - Charge Injection Effects From S1 - S4 With R1 open

Power Dissipation

The CAMEX64 chip is powered by fixed +5 volt and -5 volt power supplies and two separate adjustable bias supplies as shown in Figure 9. Power dissipation, which occurs primarily in the charge sensitive amplifiers, is controlled by the separate bias lines to the CSA1 amplifiers and the CSA2 amplifiers and/or by pulsing the voltage on the bias lines to the amplifiers. Only the effect of varying the bias line voltages to control dissipation was examined in this study.

A plot of the currents drawn by each of the groups of amplifiers was made as a function of bias voltage. From these plots, shown in Figure 9, the power dissipation in all the first stage amplifiers can be separated from power in all the second stage amplifiers. When all of the CSA1 and CSA2 amplifiers are biased off (V(CSA1)=V(CSA2)=-2V), the chip still dissipates a total of 18 mw from the Vss and Vdd supplies. Figure 10 shows a plot of total power dissipation versus bias voltage assuming that V(CSA1)=V(CSA2). Also shown are the three individual power dissipation components which make up the total dissipation: 1) the 18 mw which is always present, 2) the variable power dissipated in the CSA1 amplifiers, and 3) the variable power dissipated in the CSA2 amplifiers.

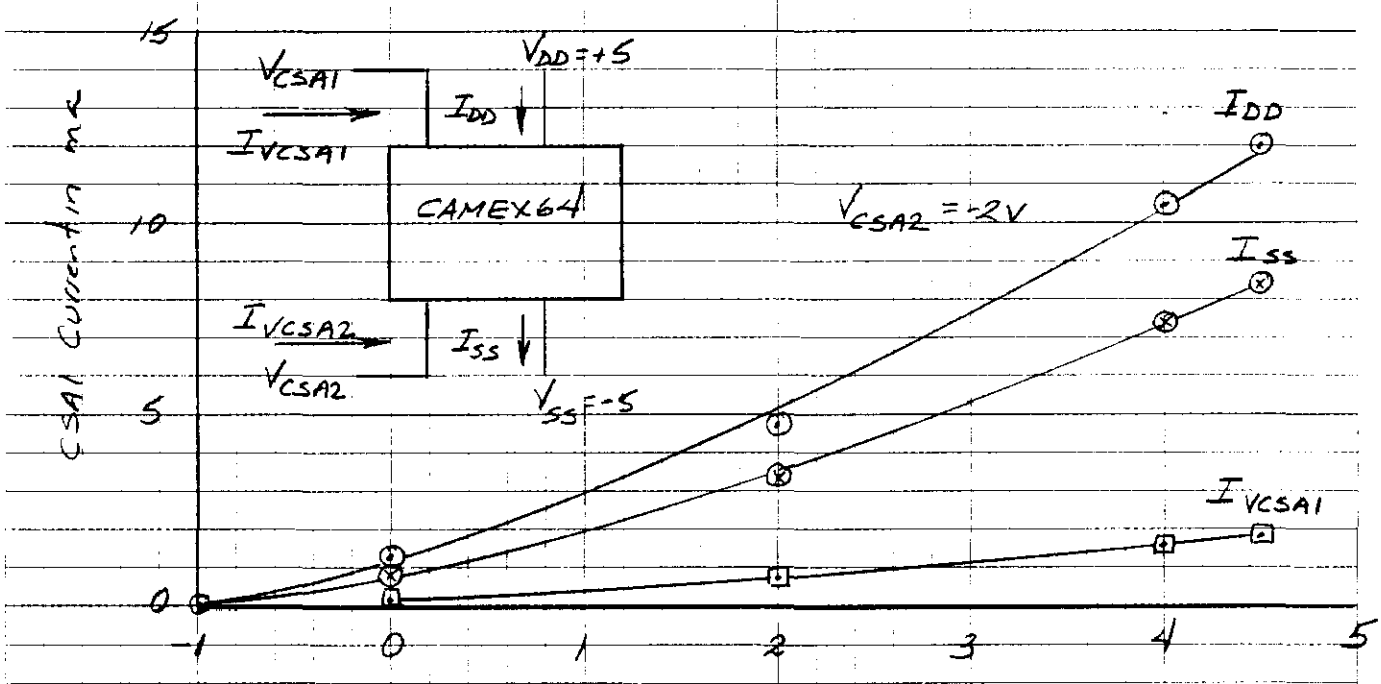
The bias voltage settings and resultant power dissipation have a significant effect on some of the CAMEX characteristics. CAMEX gain, linearity, noise, and output speed have been examined as a function of bias voltage.

The output response time of the CAMEX chip is dependent on the bias voltage for CSA2 between 0 and +4.5 volts. The same voltage range for the CSA1 bias voltage has no effect on the output response time. The positive and negative output response of the chip are different. The positive response has a standard rise time response with a small dependence on the V(CSA2) bias voltage, whereas the negative response is slew rate dependent with a significant dependence on the bias voltage. Figure 11 shows the output slew rate limitation with the bias and input amplitude set to dramatize the effect. The following table summarizes the effect of changing the CSA2 bias (Test conditions: V(CSA1)=1.7 V, Cin=10 pf).

V(CSA2) bias voltage	Output rise time (0-90%)	Output negative slew rate
0 V	1.6 us	40 mv/us
1.7	1.0	143
4.5	0.7	400

Table 1- Output Response Time

CAMEX 64 POWER SUPPLY CURRENT



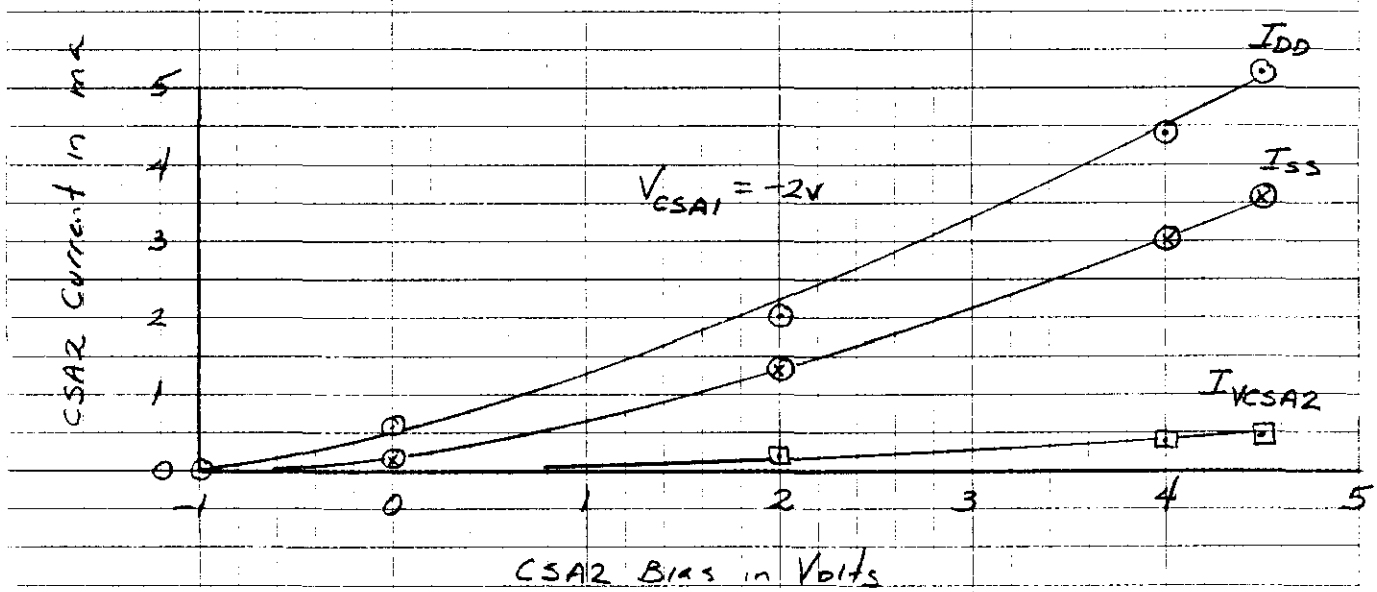


Figure 9

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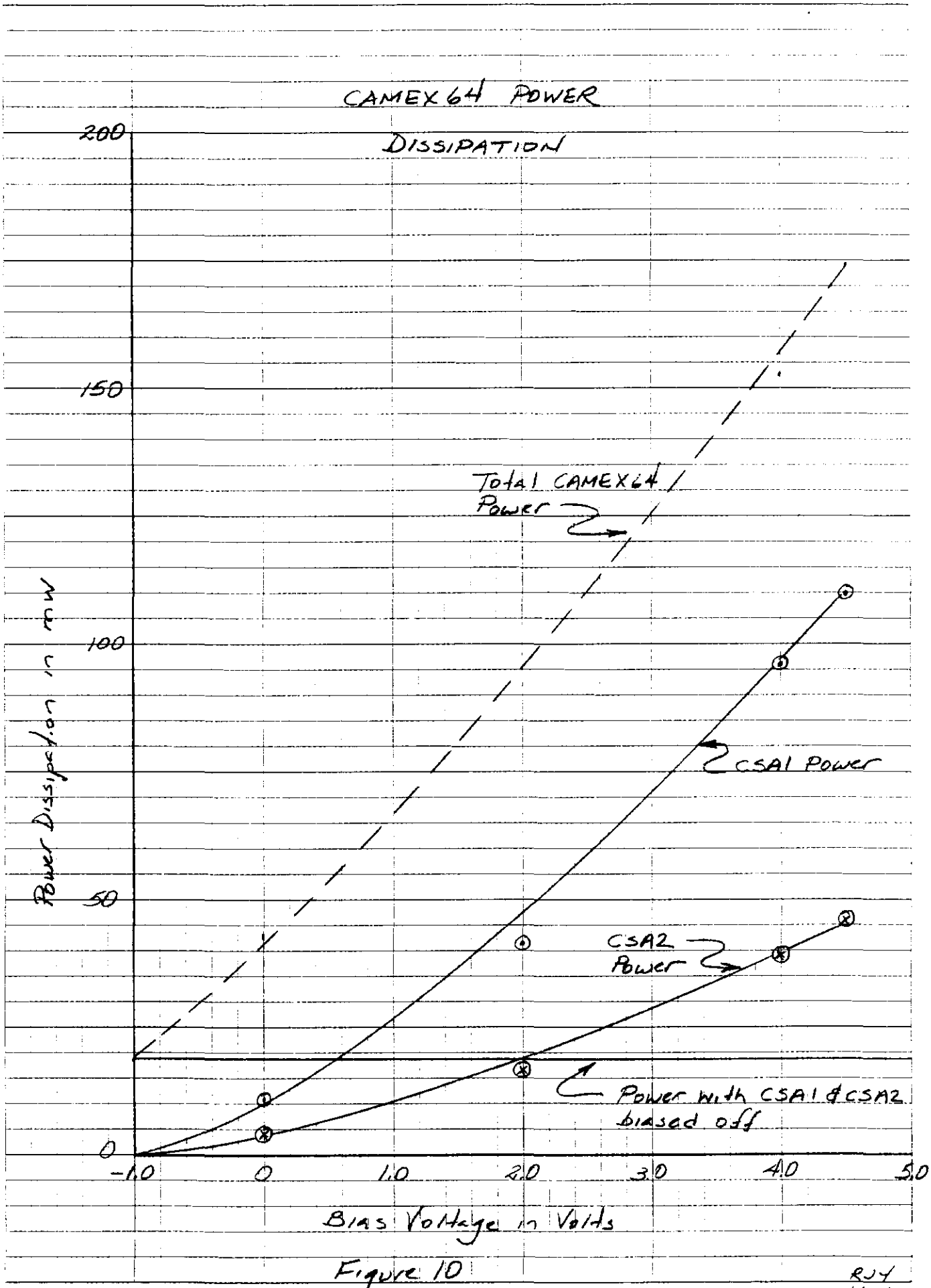

Figure 10

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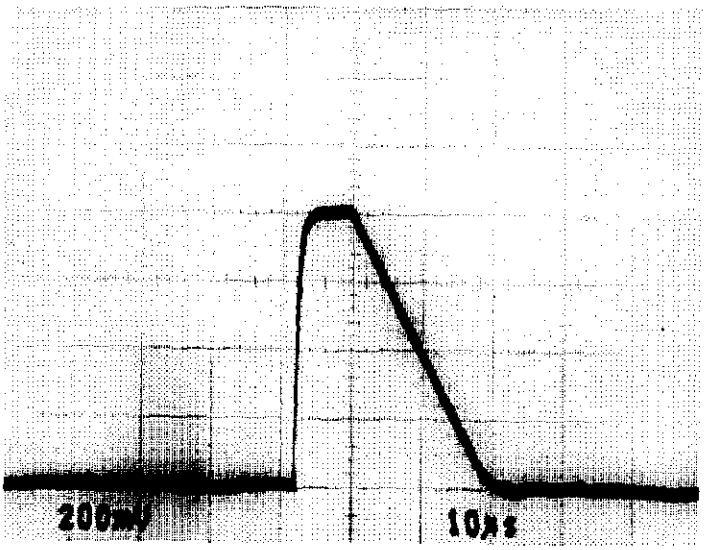
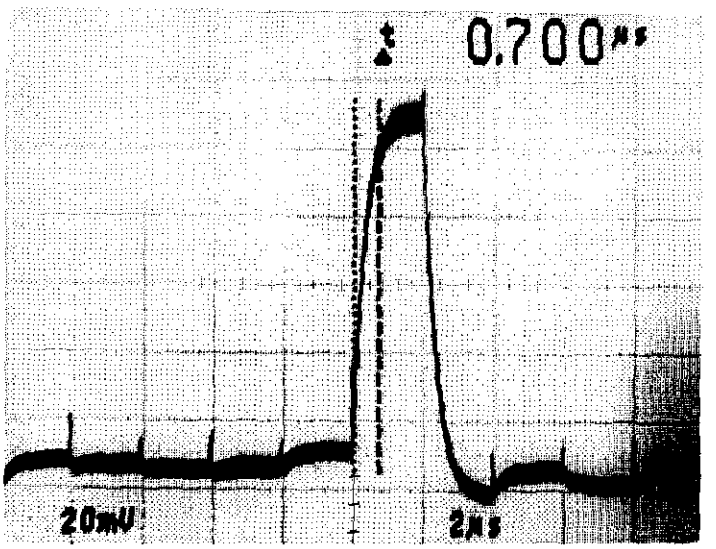


V(CSA1) = 1.7 V

V(CSA2) = 0 V

Figure 11 - Output Response Time With Slew Rate Limiting



V(CSA1) = 1.7 V

V(CSA2) = 4.5 V

Figure 12 - Output Response Showing Fast Rise Time

If the bias voltage is not large enough and a large input signal is received, the output may not have enough time to slew from one analog level to another, resulting in incorrect analog information for the following channel. Figure 12 shows the fast output response obtained on the analog output bus for a typical input signal when the CSA2 bias level is set at +4.5 V.

The dependence found on output rise time does not appear in the CAMEX gain or linearity. Varying V(CSA1) and/or V(CSA2) from 0 V to +4.5 V with Cin=10 pf has no effect on the gain or linearity of the CAMEX chip provided sufficient time is allowed for the output to respond. Specific gain and linearity information will be presented later.

Only a small dependence of input noise on power dissipation was observed. Tests were run wherein power dissipation and input capacitance were varied to determine the dependence of noise on power over a range of input capacitances. A 10 pf, 1% capacitor was used to inject charge into channel 0 of the CAMEX chip. Additional 1% capacitors were added from the input to ground to vary Cin for noise and gain measurements. For no input capacitance, channel 2 (unbonded) was used. By comparing the noise measurements for bonded and unbonded channels, it was found that a bond wire and pad added about 0.7 pf to each input. Results of the tests are shown in Table 2. (For the tests, a sampling time of 1 us and a sampling switch closure time of 250 ns was used, and a delay of 500 ns after Qin was allowed before S1 was opened.)

V(CSA1&2) Voltage	Power/ Channel	Input Capacitance 0pf	0.7pf	10.7pf	20.7pf	30.7pf
4.5 V	2.7mw	349e	405e	825e	1140e	1443e
2.75	1.8	331	382	792	1117	1390
1.75	1.4	331	368	792	1103	1395
1.10	1.1	331	368	811	1122	1433
0.25	.73	340	387	844	1202	1544

Table 2 - CAMEX Input Noise in RMS electrons Versus Channel Power

The above table shows that input noise has only a very small dependence on input power for the range of interest.

From all of the proceeding tests varying input power, a bias level of 1.75 V for CSA1 and CSA2 which corresponds to 1.4 mw/channel, seems to give reasonable overall performance (i.e. low noise, moderate power, and reasonably fast output response). For this reason most of the following test were done with V(CSA1)=V(CSA2)=1.75 V. Figure 13 is a plot of noise versus capacitance at this operating point. As can be readily seen, the relationship is not a straight line. Thus, specifying noise at the 0 pf intercept and a slope can be misleading. The noise slope from 0 to 5 pf is

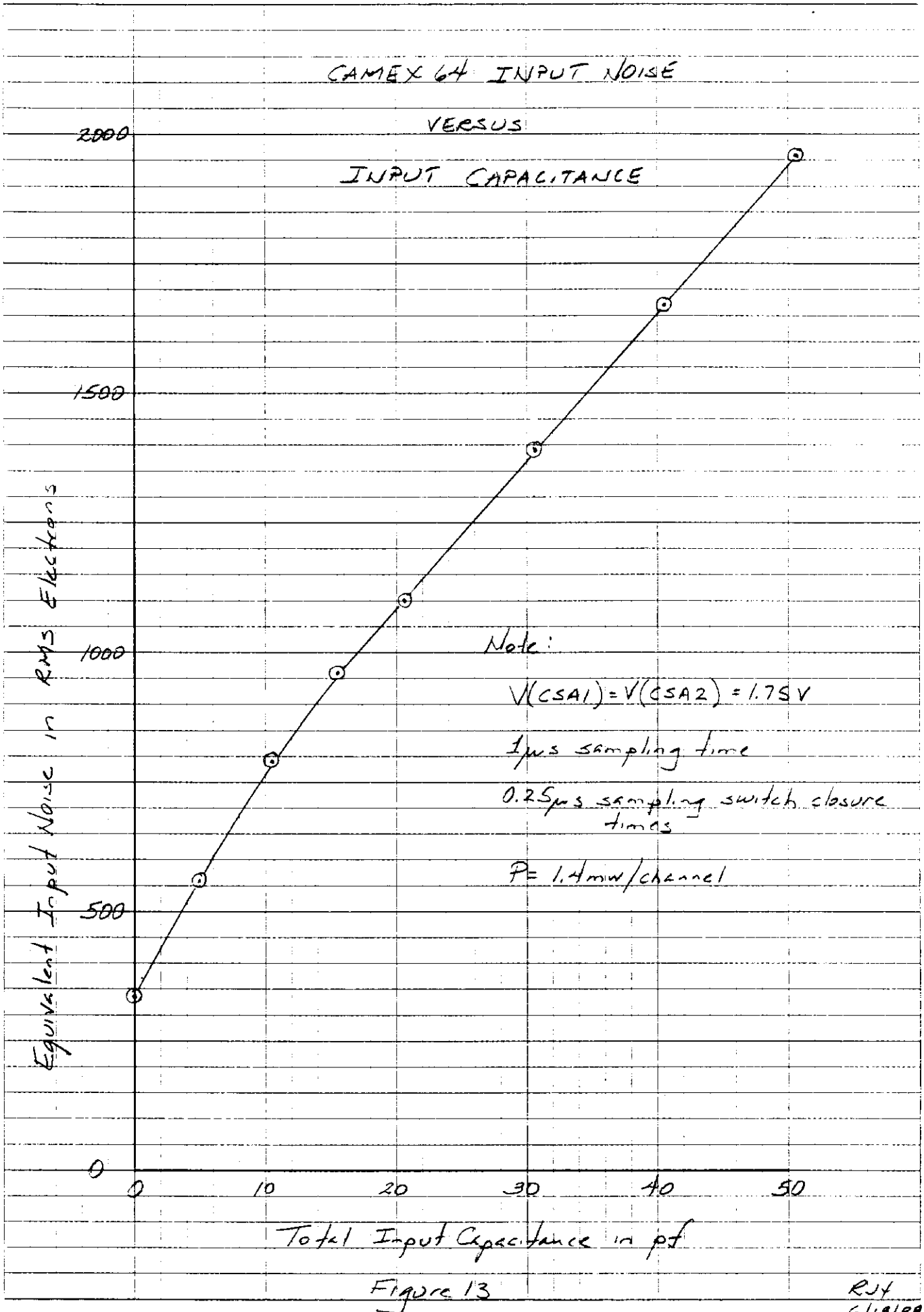


Figure 13

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47 e/pf, while the slope from 20 to 40 pf is 28 e/pf. For critical noise applications, check the noise in Table 2.

The largest detrimental effect on performance from varying the bias voltages is seen in lowering CSA2. There is only a minimal increase in noise for lowering CSA1. Thus in critical power applications, CSA1 could probably be run at lower levels than CSA2 with little change in performance and with a significant savings in power. During a normal cycle, most time is spent in the readout cycle where only CSA2 requires power. Thus if the bias lines are pulsed, CSA1 could be powered off most of the time for additional power savings.

Gain and Linearity

The range and linearity of the CAMEX device was found to be quite good. Table 3 presents the results of a linearity test on a single channel with a 10 pf input capacitor.

Qin	V(out)	Gain
+4 fc	57 mv	14.25 mv/fc
+15	214	14.25
+50	705	14.1
+150	2030	13.5
-4	-57	-14.25
-15	-214	-14.25
-50	-710	-14.2
-150	-2100	-14.0
-186	-2460	-13.2

Table 3 - Linearity and Range of CAMEX

The table shows that the CAMEX device has a range of +/-150 fc with very good linearity for most of that range. These results are unaffected by changing V(CSA1) and V(CSA2) between 0 and 4.5 V.

The gain of the CAMEX chip has a slight dependence on input capacitance. Table 4 shows the change in gain for small values of input capacitance. For these tests, sufficient time was allowed for CSA1 to reach equilibrium to insure accurate results after injecting charge.

Cin	10 pf	30 pf	50 pf
Gain	14.25 mv/fc	14.0 mv/fc	13.75 mv/fc

Table 4 - Change of CAMEX Gain with Input Capacitance

Gain across the chip from channel to channel is uniform to better than 1%.

Pedestal Variations and Crosstalk

Pedestal variations between channels on the analog output can be significant. Two chips were studied. The analog output for one chip, shown in Figure 14, had peak to peak pedestal variations between channels of 21 mv. A second chip had pedestal variations of 30.5 mv. These variations are independent of whether R2 is open or closed during the data acquisition and readout cycle. Thus these pedestals are not due to variations in charge injection from R2 opening. The pedestal variations, which are equivalent to an input charge of at least 2 fc, are large enough to be of concern. For small input signals, these variations will need to be subtracted off chip to give useful analog information.

The CAMEX device has separate capacitively coupled test inputs for the odd and even channels. Crosstalk on the CAMEX chip was studied by pulsing these odd and even test input lines and by pulsing a single channel. Figure 15 shows the CAMEX analog output when when odd channels receive a test pulse. The adjacent unbonded even channels do not change. When a large pulse is injected into a single bonded channel, no change in the adjacent unbonded channels is observed. On chip crosstalk is less than 1 part in 10000.

Using the previously determined gain for the CAMEX chip (which was measured using 1% charge injection capacitors), the value of the test input capacitors is easily found. The value of the test input capacitors is 0.92 pf.

Noise Versus Number of Samples

The CAMEX chip has four sampling switches and capacitors for each channel. The four sampling paths appears to be a reasonable compromise between noise performance improvement and added circuit complexity. Under normal conditions, all four sampling paths are used. If fewer paths are used, the equivalent input noise can be expected to increase. Because noise adds in an RMS relationship and the signal is summed directly, the equivalent input noise should vary as the square root of the number of samples. Figure 16 shows the results of a noise test wherein the number of sampling pulses was changed. Data was taken with a power dissipation of 1.4 mw/channel and a sampling time of 1 us. As before, the results show that noise does not increase linearly with capacitance. A zero capacitance noise intercept and a slope is not an accurate representation of the noise performance of the CAMEX device.

Figure 17 shows how the equivalent input noise decreases as the number of samples increases for Cin=10 pf. When the number of samples is doubled from 1 to 2 or from 2 to 4, the equivalent input noise is

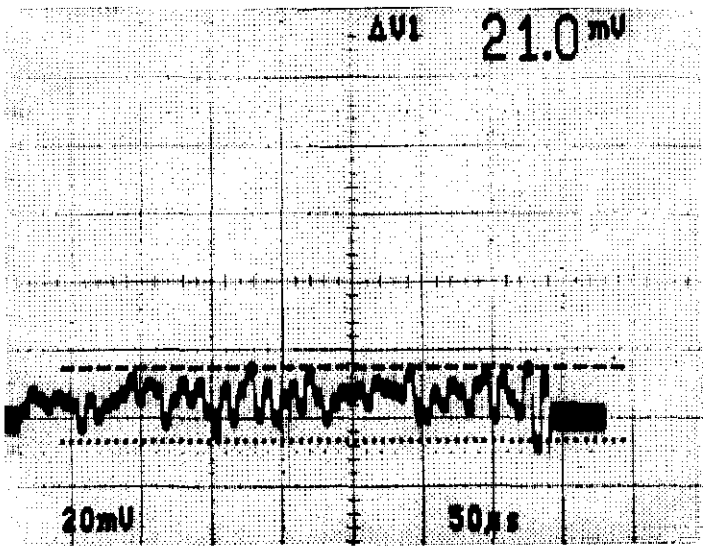

Figure 14 - CAMEX Analog Output Pedestal Variations

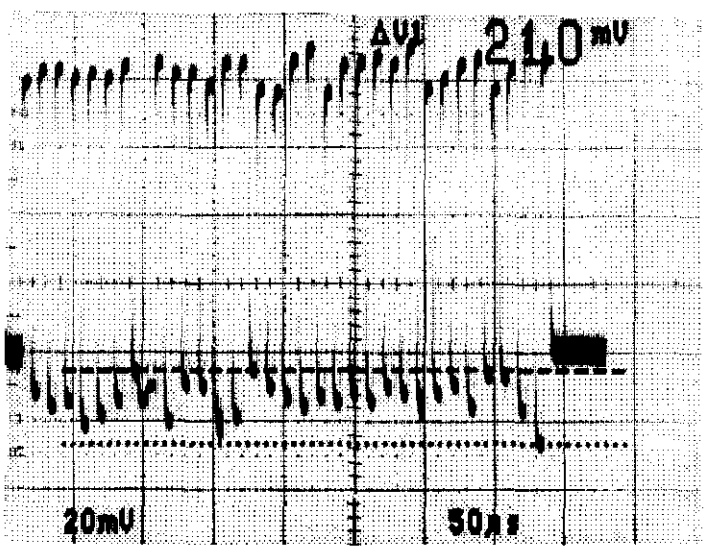

Figure 15 - CAMEX Response to Odd Channel Test Input Signal

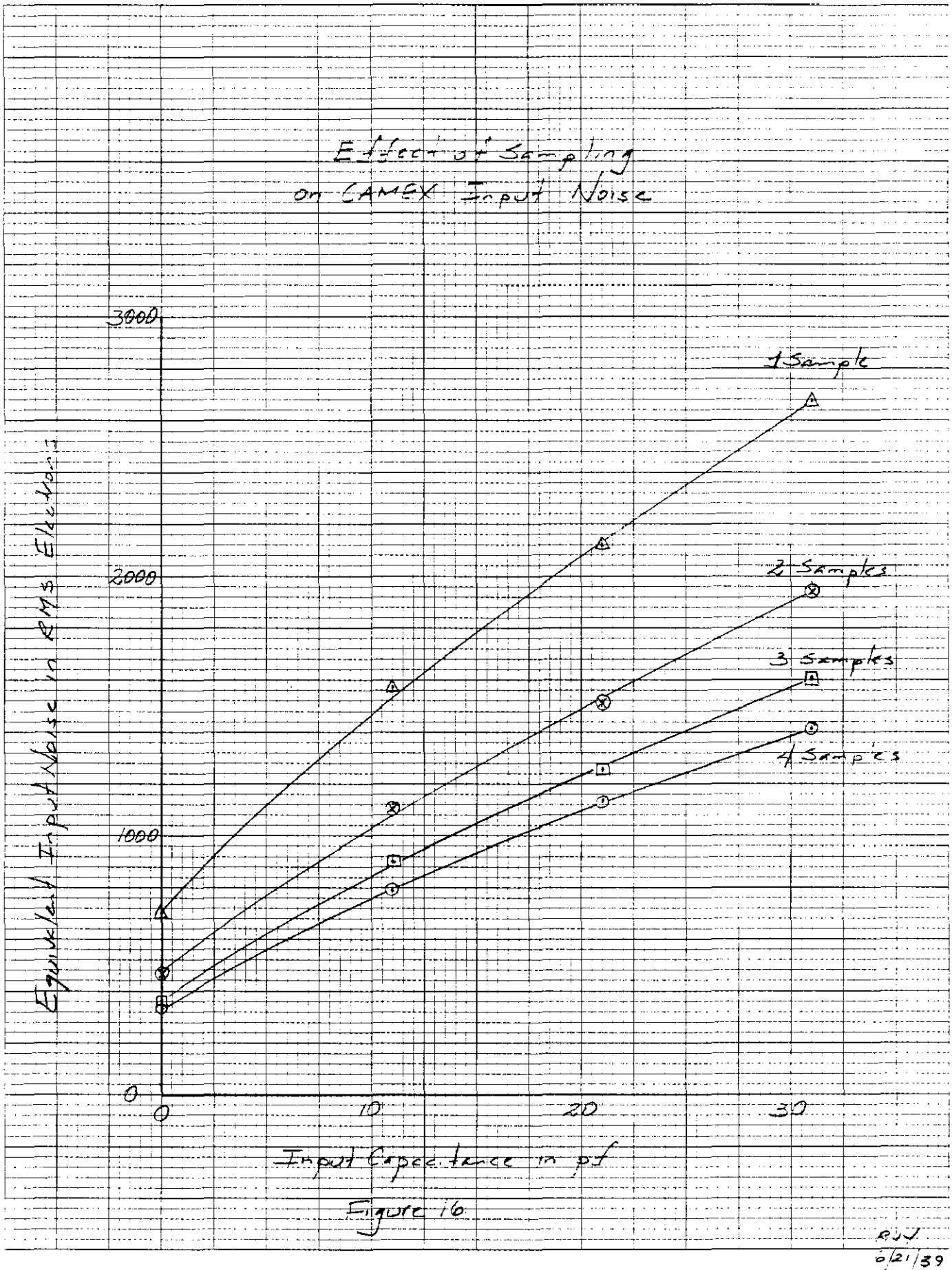

Figure 16

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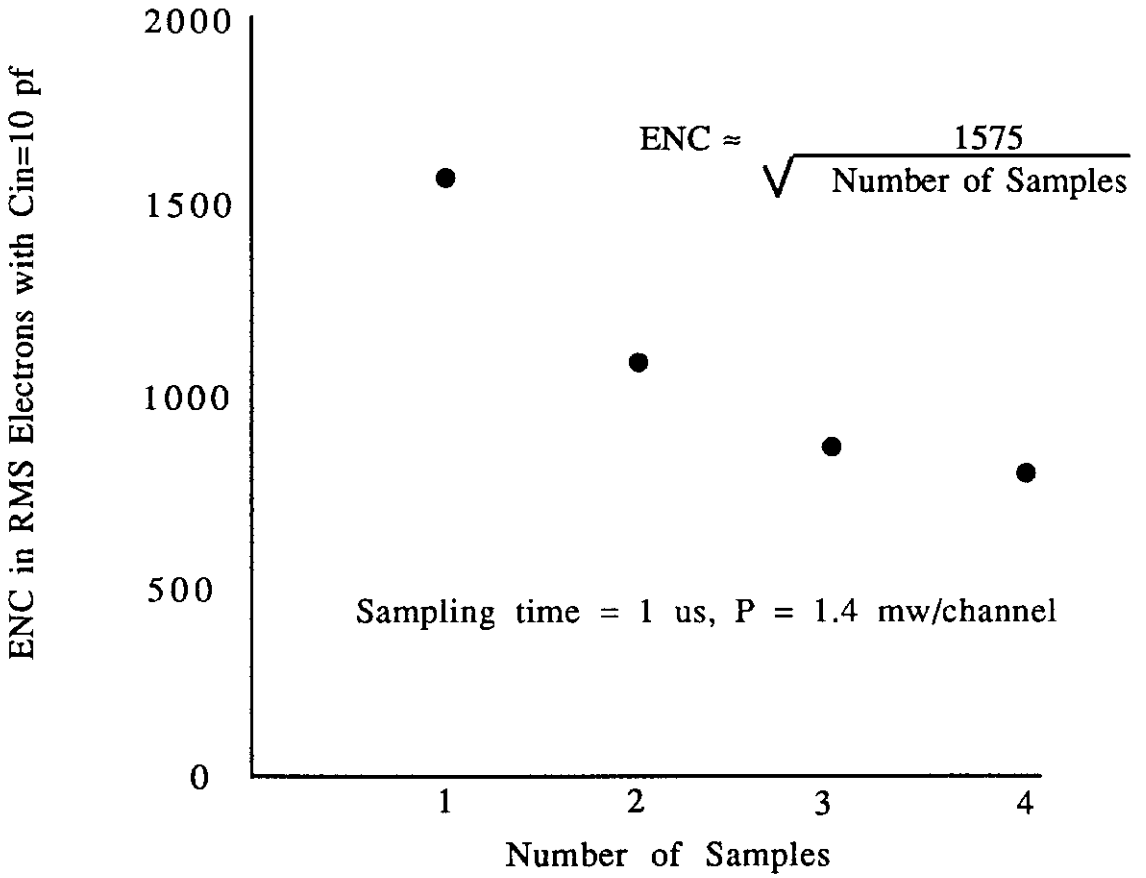

Figure 17 - Equivalent Noise Charge Versus Number of Samples

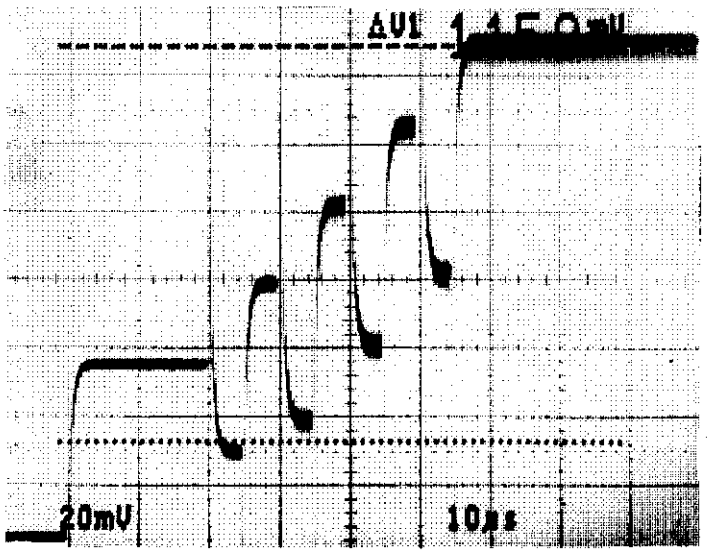

Figure 18 - Signal and Noise Buildup For 4 Samples

decreased by a factor of 1.4 which is very close to the theoretical value of 1.414. Figure 18 shows the second half of a data acquisition cycle with channel 0 connected to the output bus, beginning with the opening of R2. In this figure slow timing pulses were used to clearly show the buildup of the output signal and noise during data acquisition. A charge of 8 fc is injected after opening R2 causing the output to shift by a total of 115 mv after all sampling pulses. With each sampling switch (S1-S4) closing and opening, the output signal increases from the pedestal level by 115 mv/4 or 37.5 mv. The noise which appears as a slightly wider trace after each sampling pulse increases at a lesser rate. As previously discussed, charge injection from S1-S4 cancels.

Noise Versus Sample Time

Theoretically, noise is dependent on the time between sampling pulses. Practical considerations must take into account the bandwidth of the amplifiers as well. To determine the effect on the CAMEX chip, a test was run where the sampling time was varied over a practical range of interest. For the test, the sampling switch closure times were always 150 ns and the time from charge injection to opening the first sample switch, S1, was always held fixed at 300 ns. This was done to insure that gain change effects from other factors did not influence the results. Test results are shown in Table 5.

Sample Time	Input Capacitance 0 pf	10.7 pf	20.7 pf
200 ns	322 e	832 e	1299 e
400 ns	331	802	1129
800 ns	340	802	1107

Table 5 - CAMEX Noise Versus Sampling Time

As can be seen, the equivalent input noise does not change much for reasonable sampling times. Sampling times above a few hundred nanoseconds are unnecessary, while sampling times of 100 ns or less result in low circuit gain.

Summary

The CAMEX64 performance has been independently characterized for those quantities of general interest to those planning to use the chip. More information and greater details of the operating conditions has been presented than has previously been reported. For background information see the papers listed in the following reference section.

References

1) G. Lutz, W. Buttler, H.Bergmann, P. Holl, B. J. Hosticka, P. F. Manfredi, and G. Zimmer, "Low Noise Monolithic CMOS Front End Electronics", NIM A263 (1988) 163.

2) W. Buttler, G. Lutz, H. Bergmann, H. Dietl, D. Hauff, P. Holl and P. F. Manfredi, "Low noise - Low Power Monolithic Multiplexing Readout Electronics for Silicon Strip Detectors", MPI-PAE /Exp. El. 178, July 1987.

3) W. Buttler, G. Lutz, P. Cattaneo, and D. Hauff, "A Low Noise - Low Power CMOS Chip For Readout of Silicon Strip Detectors", ICFA Instrumentation Bulletin, May 1988.

4) W. Buttler, B. J. Hosticka, and G. Lutz, "Noise Filtering for Readout Electronics", presented in Munich at the 5th European Symposium on Silicon Strip Detectors, February 1989.

5) Private communication with W. Buttler, February 1989.