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TITLE: CONFIGURATION FOR THE WNR DATA ACQUISITION SYSTEM FOR NEUTRON MEASUREMENTS

AUTHOR(S): R. O. Nelson
D. M. Barrus
G. Cort
J. A. Goldstone
D. E. McMillan
R. V. Poore
D. R. Machen, Scientific Systems International

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Los Alamos Los Alamos National Laboratory
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CONFIGURATION FOR THE WNR DATA ACQUISITION SYSTEM
FOR NEUTRON MEASUREMENTS

R. O. Nelson, D. M. Barrus, G. Cort, J. A. Goldstone,
D. E. McMillan, L. B. Miller and R. V. Poore

Los Alamos National Laboratory 151 2470

and D. R. Machen

Scientific Systems International 151 7026

Abstract

The configuration for a new data acquisition system for the Weapons Neutron Research Facility at the Los Alamos National Laboratory is introduced. The system utilizes a FASTBUS front-end for real-time data collection and DEC computers for the experiment control and analysis. A local area network is used extensively within the overall system.

Introduction

In recent years the Weapons Neutron Research (WNR) facility has developed into one of the nation's principal neutron scattering centers for nuclear physics and condensed matter measurements. Neutron flux intensities and pulse characteristics will be substantially enhanced when the Proton Storage Ring (PSR), which circulated first beam this spring, becomes fully operational in the fall. Flux intensities are generally expected to increase by a factor of approximately 250, thus rendering the present data acquisition system inadequate. The PSR repetition rate may be adjusted as low as 12 pulses per second without sacrificing average intensity. With this capability new measurements using slow neutrons are practical and may increase memory requirements for data storage up to an order of magnitude over that now employed. Using the current facility repetition rate, these slow neutrons arrive at the detector after the start of the next burst of neutrons (frame overlap) thus creating ambiguity. Because of growth in the measurements program, it is further desired to increase the number of instruments served by the new system to a dozen.

From these neutron source characteristics, from the strengths and weaknesses of our present system as well as those at other laboratories, and from the availability of high performance computer and communication equipment at reasonable cost, five basic guidelines for our new system evolved. 1) Service each instrument with its own dedicated system. 2) Support real-time data acquisition in dedicated hardware outside the general purpose computer environment. 3) Link the instrument system together loosely with a local area network. 4) Include within the network a more powerful computer to serve data reduction and analysis needs and oversee data archiving. 5) Modularize both software and hardware to enable the broadest use of modules in support of diverse instruments and experiments.

Upon examining options available in the computer market, the preferences of users, and software and hardware from other installations that might be incorporated within our system, a solution based on DEC equipment was dictated. To handle the estimated count rates which, time averaged, may reach 1 MHz and in-

stantaneously reach 45 MHz, our design required the speed and flexibility afforded by FASTBUS[1]. This paper introduces the factors which motivated our design, the resulting data acquisition configuration, and the current status of the work. Discussion begins with the system wide perspective and proceeds toward the FASTBUS hardware at the detector interface.

Network

At the highest level of generalization, our system may be viewed as a network which links a relatively powerful central host system to a set of less complex front-end systems, each dedicated to data acquisition for a single neutron scattering instrument. The network, shown schematically in Figure 1, provides the hardware communication path and software control for the data transport from the front-end systems to the central data archive, as well as for the flow of software modules in the opposite direction. As the staffing support for the project is established at a minimum level, we prefer to buy commercial products whenever possible. Thus, the network is necessarily considered to be an off-the-shelf item.

At this time the network is largely in place. The local area network linking our systems together is an Ethernet system consisting of both fiber optic and coax sections. The coax sections are used within a

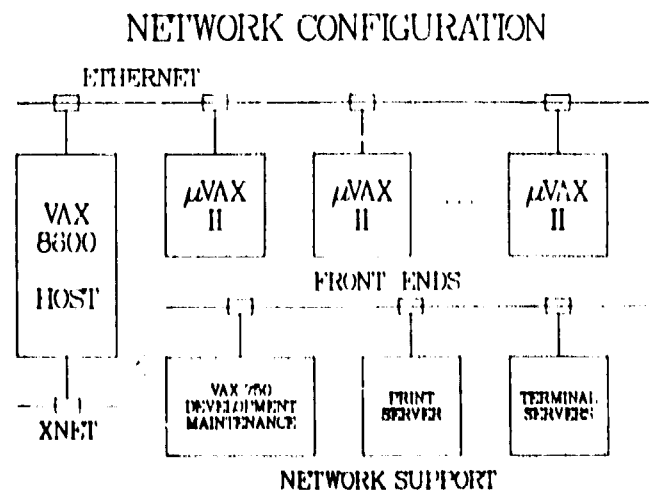


Figure 1. Block diagram for the major system components of the WNR local area network. No attempt is made to distinguish between the cable and fiber optic portions. The host acts as a gateway to the laboratory wide network, XNET.

single building and the fiber optic sections are used for geographically isolated buildings and sites where differing grounds may pose problems. Presently, the fiber optic portion is installed between six buildings. It links together two VAX 11/750 computers and one microVAX I computer. A connection to the laboratory wide broadband network is provided through one VAX 11/750 system. We still are in the development phase of the project so the new systems and the coax joining them do not yet exist. Software control is provided with DECNET. Should performance issues arise in the shipment of large data files, some work to adapt a locally defined protocol to the existing drivers would be acceptable at some point in the future.

Print servers and terminal servers will be connected to the network and will provide network resources not associated with any particular computer system. Two terminal servers are currently on order.

Host System

The central host system is designed to provide added capability for the experimental program in three major areas: data archive management, data reduction and analysis where extensive numeric calculations may be involved, and software development and maintenance support. This system will have no real-time data acquisition role and is intended primarily to support experiments which have been completed, in contrast with those in progress. The central host system will be a VAX 8600 class machine.

After data collection, data obtained with the front-end system will automatically be forwarded to the host system where it is archived and retained on-line for the duration of the run cycle. Not less than 10 Gigabytes of disk storage is envisioned for this system. Powerful color graphics terminals supported with DMA access will be provided to assist with data interpretation and analysis. Through the laboratory network (XNET), it will be possible to access powerful computing resources with Crays, 7600s, etc., as well as exotic peripherals such as high speed laser printers and photo-plotters. More routine peripherals like magnetic tape drives will be available locally for archive, backup, and data export functions.

Presently, the host is an overloaded VAX 11/750. However, much of the host functionality is present in this system including connection to the laboratory network and a single color graphics terminal. Disk storage capacity is limited to 1 Gigabyte at this time. To extend this system to the desired configuration requires a significant amount of funding.

At this writing a second VAX 11/750 dedicated to software and hardware development and maintenance has been added to the local area network. While originally perceived as an integral component of a single host computer system, the separation of many of the maintenance aspects of system support to this computer will likely prove highly beneficial over the lifetime of the data acquisition system.

Front-end Systems

Each front-end system exists to service the needs of a single neutron scattering instrument. Although each computer will likely have sufficient resources to service several experiments, this approach seems unwise at present system costs in view of the risk of disruptive user interaction. These extra CPU cycles should be regarded as a resource available to the experimenter which, for example, may allow him to

determine the health of the experiment via some detailed on-line analysis. Other experiments may be able to finish data collection and at the same time be finished with data reduction and analysis.

Powerful as it may be, the front-end computer is incapable of handling the expected worst case data rates from the detector arrays. Scaling current WNR counting rates to the expected PSR levels indicates that burst rates of 45 MHz for a period of 10 us early in the neutron pulse are possible. Of course these count rates drop at later times in the pulse finally reaching an average count rate of 1 MHz for the worst case. Additional requirements that dead-time corrections not exceed 0.5% and constant dead-time be enforced (drop all data from a neutron burst if any event cannot be processed within a user defined fixed time interval) force an implementation with custom hardware for buffering events as they arrive from the detector. In our judgement it is reasonable to complete the data capture process, including data compaction and histogramming, in hardware and dedicate the computer to control and analysis tasks. This hardware is described at length in the following section.

Development of these front-end computer tasks is extremely software intensive and has been the focus of considerable effort over the past year. As the subject of other papers[2,3], the main data acquisition tasks are listed below as background for the hardware requirements. They include configuration initialization, instrument control, data collection, data cataloging, automatic run sequencing, and graphics for monitoring the health of the experiment and data analysis.

The basic hardware configuration for each front-end is shown in Figure 2. As delivered, each microVAX II will be contained within a 5.75" rack mount chassis which includes 2 Megabytes of memory, a 71 Megabyte hard disk, a 95 Megabyte cartridge tape, 4 serial ports, and an Ethernet interface. We anticipate that in the future it will be necessary to upgrade this disk to increase the local storage capacity to at least 120 Megabytes. At the completion of each run, control information and data selected by the experimenter will be written to the local disk in a generalized and flexible format. These files may be as large as 4 Megabytes, so even large local disks could be filled quickly. Local storage is mandatory since reliable operation of the network and host system should not be taken for granted. At a minimum, local storage capacity for files created during a day of running is required. Should the network/host remain unavailable, the local cartridge tape could be used to make copies of all data from the preceding day. Normally, the cartridge tape is reserved for disk backup operations.

Since the data obtained with the front-end systems can be subtle and complex, high resolution color graphics will be included here as well as on the more powerful host system. This graphics capability enables rapid inspection of the quality of the data and allows in near-time an experimenter to select measurements that make best use of his beam time. Initially, a combined command/graphics terminal will provide experiment control and data monitoring capability. Later a second high resolution dedicated graphics terminal with color and a parallel DMA interface will be added.

A simple register driven I/O interface for a CAMAC system crate will be included on the front-end system. Since no preset scalars for FASTBUS systems

FRONT-END CONFIGURATION

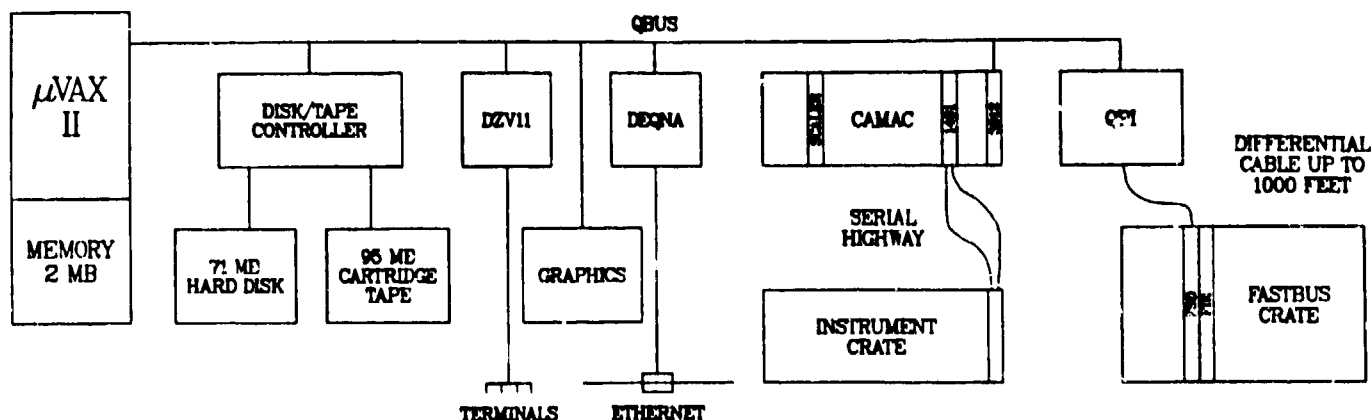


Figure 2. Block diagram for the front-end system. Contents of the FASTBUS and CAMAC crates depends on the instrument and/or the experiment.

are commercially available at this time, existing scaler and pre-set scalers will be used in the CAMAC environment. Likewise, motor control interfaces and monitoring equipment distributed throughout the facility on various CAMAC serial highway systems will continue in use with a serial driver located in the system crate.

As delivered, our current prototype front-end system consists of a microVAX I CPU with 1 Megabyte of memory, a 31 Megabyte hard disk, two 400 Kbyte floppy drives, a four-port serial interface, and an Ethernet interface. We have added a register I/O interface, Model 1912 from Kinetic Systems, and a CAMAC crate for the support of existing CAMAC modules which will continue in use. Also installed in the CAMAC crate is a register driven FASTBUS interface, the FIORI, from CERN[4]. To date this system has been used exclusively as a FASTBUS hardware development workstation.

FASTBUS Systems

Each front-end will also connect with a FASTBUS subsystem, the truly real-time component of the system. The interface for FASTBUS will be a QPI (Q-bus Processor Interface), currently under development at Kinetic Systems. The unit is essentially the QPI designed at Fermilab[5] for use with the DEC buses, but adapted for the 22-bit wide address/data multiplexed Q-bus. Within the FASTBUS crate, the interface connects to a set of five custom module types. Details of these modules have been presented elsewhere[6], and only the basic functionality is summarized here. Note, however, that the histogramming memory module has benefited from the introduction of 256K RAM technology and now each module contains 2 Megawords of 20-bit memory.

As in most neutron measurements, the flight time over a fixed length path characterizes the neutron momentum and is the primary parameter of any measurement. Three of the FASTBUS modules are directly involved with the time interval determination, one acting as a master clock and two as time-of-flight input buffer modules. The fourth module type provides a limited event processing capability and the last type is an auto-incrementing histogram memory.

Figure 3 illustrates the basic data flow of the FASTBUS system. Stepping through the operation of the system briefly, the master clock is initialized through the host interface, and begins counting time bins when triggered at the leading edge of the neutron burst (TO). The time information and optional parallel information is strobed into the time-of-flight (TOF) input buffer by a pulse from the detector system. Data is accumulated in the buffer for the duration of the neutron burst. At the start of the next neutron burst the data is read for a complete frame of events into the mapper processor which compacts the data. Compaction is accomplished primarily through substitutions from a map loaded into the mapper processor through the QPI interface. Individual events are reduced to addresses which are presented to the bulk store module for histogramming. The histogram may be read by the front-end microVAX for data monitoring or recording.

The modularity of FASTBUS and the flexibility of the design allow the experimenter to configure the module set to accommodate a wide spectrum of counting rate environments. Additional modules may be added to provide independent parallel paths from TOF buffers to bulk store memories. Should dead-time reach an unacceptable level during the count, additional TOF buffers may be introduced to reduce multiplexing at the TOF module. If average count rates saturate the capability of the mapper processor, then additional mappers may share the TOF service load. If the histogramming bandwidth becomes the limitation, then as with the others, more modules can be installed. Maximum system performance is finally limited by the speed of the FASTBUS backplane for inter-module communication.

With ECL implementation of modules, random FASTBUS data transfers can achieve rates of 10 MB. In our design, the block transfer mode is used extensively and transactions between the mapper and bulk store utilize only the address cycle. Effectively, only one half as much data passes on the bus as with random cycles, but it always passes twice: once from buffer to mapper and again from mapper to bulk store. Neglecting the overhead of bus arbitration and some setup delay incurred once for each block transfer, the data might be expected to flow at the 10 MB rate for ECL implementations. As a mixture of both ECL and TTL,

SYSTEM DATA FLOW

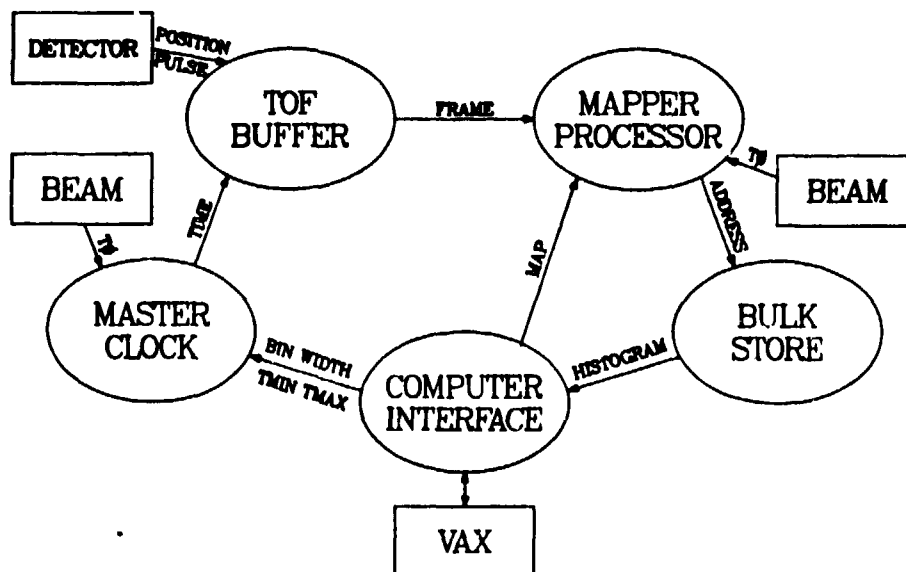


Figure 3. Schematic flow of data through the FASTBUS module set. Before data acquisition begins, modules are initialized through the computer interface. Once begun, the data flow proceeds from the master clock in the clockwise direction.

our design goal is set at 5 MHz for time averaged histogramming rates.

Design and fabrication of prototypes of the module set has been completed and only the mapper module remains to be debugged. Since the mapper timing remains uncharacterized, actual system performance figures are not yet available. Unless more than one bulk store is used, however, the read/increment/write cycle time, 300 ns, is the limiting factor. A future design which enabled memory interleaving will eliminate this performance problem.

Buffer performance in the TOF greatly exceeds the design specification. Pulse pairs with time spacing as low as 20 ns may be accepted without loss of data in a pair of registers preceding a 64 word deep FIFO. Data then flows into this FIFO at its maximum rate, 20 MHz. Data is removed from the bottom of the FIFO at 10 MHz and deposited in one of two static RAM frame buffers that toggle between neutron bursts. The logic which monitors the event strobes can resolve strobe separation times down to 10 ns and thus any dead-time in excess of this amount can be flagged. Assuming Poisson statistics, the dead-time correction for the highest count rate of 1.7 MHz for a single detector element and for a duration of 10 μ s is less than 0.02%.

Summary

To date our experience with the coalescing system is very positive. The partitioning of the system architecture is perhaps its greatest feature: 1) data capture and histogramming within the excellent real-time FASTBUS environment relieves the front-end computer from time critical functions and therefore 2) enables the use in the front-end systems of a familiar and robust operating system (VMS) not known for its impressive real-time characteristics. Finally, 3) the network, in addition to providing a loosely coupled system, also allows gradual growth which matches well our funding outlook.

Acknowledgements

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