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MULTICHANNEL INTERVAL TIMER

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Abstract

A CAMAC based modular multichannel interval timer is described. The timer comprises twelve high resolution time digitizers with a common start enabling twelve independent stop inputs. Ten time ranges from 2.5 μs to 1.3 μs can be preset. Time can be read out in twelve 24-bit words either via CAMAC Crate Controller or an external FIFO register. LSB time calibration is 78.125 ps. An additional word reads out the operational status of twelve stop channels. The system consists of two modules. The analog module contains a reference clock and 13 analog time stretchers. The digital module contains counters, logic and interface circuits. The timer has an excellent differential linearity, thermal stability and crosstalk free performance.

Introduction

The multichannel interval timer is a modular system for the measurement of time intervals between a common start and twelve separate stop inputs. The timer is equivalent to a system of twelve single channel time digitizers. Each one covers a range of up to 1.3 ms in 78.125 ps increments. The counting of time is initiated simultaneously in all twelve digitizer channels by the start pulse. An additional, thirteenth, digitizer counts the selected time range. An internal 50 MHz reference clock is used for coarse counting of time in 20 ns intervals. Analog time interpolators[1,3], one of them for the start and twelve for the stop channels, have been designed for the stretching of time fractions smaller than a clock period occurring at the beginning and the end of each time measurement. The time stretching by a factor of 256 is equivalent to increasing the effective counting clock frequency from its actual 50 MHz to 12,800 MHz[2]. Each interpolator controls an additional, vernier counter for the digitizing and storage of stretched time fractions.

The whole timer system consists of two CAMAC modules. One is an analog module containing the thirteen interpolators, and the internal 50 MHz clock oscillator together with the control circuits. The other is completely a digital module, containing counters (two each for the start and twelve stop channels), and the arithmetic, control and interface circuits. The system is fully CAMAC compatible. An alternative interface for automatic serial data transfer to external derandomizing data storage FIFO (first in first out) register, is also provided.

In measurements where more than twelve stop channels are required, several additional multichannel interval timers, working in parallel, may be needed. An independent clock module was added to the system providing the simultaneous clock reference for up to six timers. The clock module also includes a precision calibrating pulse generator. The calibrator output is a series of accurately spaced time markers, which can be used for driving the start and stop inputs of the timer. This makes for an easier alignment, calibration and trouble-shooting of the system.

General Description

The analog module block diagram is shown in Fig. 1. Figs. 2 and 3 are the block diagram of the digital module, and Fig. 4 shows the basic timing. The analog circuits include the 50 MHz clock generator which is controlled by either the internal oscillator or by an external 50 MHz source. The separation of the analog from the digital circuits minimizes the interference between the two modules and number of interconnections between them.

Time counting is initiated by a start pulse setting the start interpolator latch FF1 (Fig. 1). A timing capacitor C in the interpolator is then charged by a constant current I1. The charging of C stops when the latch FF3 is set by the second clock pulse following the start. The capacitor C at that point starts discharging back to its original level by a small current, I2. The ratio of the two currents is the time stretching constant. In this case a ratio of 256 was selected. The lines A to F in Fig. 4 illustrate this sequence. A comparator circuit in the interpolator senses the level across the timing capacitor. When the initial level is reached, the comparator resets the start latch FF4 (line H). The leading edge of this square pulse is timed with the clock, since the marker pulse that had started the capacitor discharge had set FF4 at the same time. The width of this square gate pulse controls the counting of clock pulses in the start interpolation counter (Fig. 2). Each count thus represents 1/256th of the clock period, i.e., 78.125 ps (for the 50 MHz clock). The interpolator gate pulse sets also the start latch in the digital module, which in turn initiates the counting in the range counter and all stop counters, digitizing the time in "coarse" 20 ns increments.

All twelve inputs to the stop channels are enabled simultaneously by the start interpolator about 15 ns after the acceptance of the start signal. The inputs remain enabled for the duration of the range time counting. Any stop pulse appearing during this enable time is accepted by setting the FF1 latch in the corresponding stop interpolator (Fig. 1). The stop interpolators are identical to the start interpolator. The time interval between the leading edge of any stop pulse and the second clock marker that follows it is stretched 256 times in the same way as the start pulse was processed in the start interpolator. A square pulse, equal in length to the duration of the stretched stop interval, is generated (Fig. 4, line R). This pulse sets the corresponding stop latch in the digital module (Fig. 2). Each stop channel has two counters. All twelve "coarse" stop counters are started simultaneously with the range counter by the start latch. They count real time in 20 ns increments. The setting of the stop latch by the stop interpolator terminates the counting in the corresponding "coarse" stop counter but in turn starts the counting in the stop interpolation counter, digitizing the length of the stop interpolation pulse (lines S and T in Fig. 4).

The measured start-stop time equals thus the sum of the start interpolator counter and stop "coarse" counter reading minus the reading of the stop interpolator counter. During the data readout, each stop channel is switched to the arithmetic unit by addressing the data selector. After the calculation, the stop can be presented in a 24-bit binary word to either CAMAC Dataway or an external FIFO register for fast temporary storage.

Status of each stop latch indicating that the stop channel had operated is displayed on the front panel of the digital module. Also, the status of all stop

latches can be read out first, as a separate status word, making shorter the transfer time by reading out only the stop channels containing data. The FIFO register readout logic automatically skips the unused channels in order to save on memory space. Such a readout sequence, initiated by the accepted start, begins with a blank word for spacing the events in the FIFO register, followed by the status word first and then only the stop channels containing data. The timer system is cleared automatically at the end of the readout sequence and enabled for a new start.

Access to the start interpolator can be controlled by fast NIM signal applied to the gate input. Also, the analog module is locked up for the duration of the CAMAC inhibit signal.

Once started, the timer is not affected by additional start input signals. The system remains busy until cleared at the end of the data transfer cycle. Also, the system can be cleared either manually or electrically by an external "fast" clear signal. A NIM output monitoring busy status of the timer is available for external timing purposes.

Interpolation Technique

In order to achieve an incremental resolution of 78.125 ps by direct counting, the time digitizer would require an unfeasible clock frequency of 12,800 MHz. The need for a very high frequency clock for timing is eliminated by using the interpolation technique, based on rapid charge and slow discharge of a capacitor[2,3]. This method offers an excellent differential linearity of time-to-digital conversion. Two interpolators are required for stretching the time fractions, at both ends of each measured time interval. Cost, space and power dissipation per interpolator are especially important parameters in a crowded multiple channel system. Crosstalk, particularly between adjacent channels, is minimized by careful lay-out and filtering. Due to the interpolation, all the counting in the process of time digitization can be done by a frequency of 50 MHz. Thus low power Shottky devices can be used because of this relatively low counting speed.

The principle of a start-stop interpolator pair operation was outlined above. In explaining Fig. 1 more in detail, the flip-flop FF1 is triggered on the leading edge of the start pulse providing that the D input has been enabled by the start gate. FF1 switches a constant current I_1 from the transistor Q_1 to Q_3, starting to charge the capacitor C. Also, F1 enables the D input of the flip-flop FF2, which is then set on the following leading edge of the free running clock pulse train. FF2 in turn enables FF3, which is set by the next clock pulse (Fig. 4, lines D and E). FF3 stops the charging of C by switching the current I_1 from Q_3 into Q_2. The charging time of the capacitor cannot be shorter than one clock period nor longer than two periods. The linearity of time stretching is thus greatly improved.

The capacitor is continually discharged by a smaller constant current I_2. Ratio of the currents that charge and discharge the capacitor is the interpolation constant: $(I_1-I_2)/I_2=K$. The triangular voltage waveform across the capacitor has the leading slope proportional to $(I_2-I_1)/C$ and the trailing slope proportional to I_2/C. This voltage is sensed by a comparator, producing square pulse, equal in length to the base of the triangular waveform on the capacitor (lines F and G).

The flip-flop FF4 was set at the beginning of the capacitor discharge cycle by the output of the FF3 (through a differentiating circuit), and reset at the end of discharge by the trailing edge of the comparator output (line H). The reset of FF4 is synchronized with the clock by superposition of the clock pulses upon the comparator output. Since the leading edge of this waveform is also synchronized with the clock, it can be easily digitized by counting the clock pulses it spans (line L).

By setting the start flip-flop FF1, a row of 12 stop interpolators is enabled by removing the clear from the stop flip-flops FF1 and FF4. The stop interpolators are now ready for accepting the stop pulses. The start interpolation timing diagram of Fig. 4 (lines B to H), also applies to the processing of the stops. The start and stop interpolator FF4 outputs control the digital module. The separation and width of these waveforms are digitized by counting the clock pulses. Each measured time interval is thus defined by three numbers, representing the "coarse" time separation between the start and the stop pulses, and the expanded fraction of a clock period left at the beginning and the end of the measurement.

Description of Logic Module

The separation of analog from digital circuits minimizes electrical interference and reduces to only a single twisted line the interconnections between each interpolator and its counting and logic circuits. Each interpolator is sensed by a line receiver (Fig. 2), setting the start latch and the stop latch at appropriate time (lines H and R in the timing diagram, Fig. 4). The start latch enables the clock gate to all the counters. The "coarse" start (range) counter and all the 12 stop counters start counting simultaneously (lines M and T). Only one stop channel is shown in Fig. 4. The start interpolation counter is also enabled by the line receiver and counts for the duration of the start interpolation time (lines H and L).

The "coarse" counting in the stop counter closes upon the setting the stop latch (lines R and T) and the stop interpolation counter then counts for the duration of the stop interpolation time (lines R and S). There is no error in counting since all waveforms were synchronized with the clock by the interpolator.

The total time elapsed since the start is counted by the range counter in increments of 50 MHz clock periods. The active time range is defined by the range selector (Fig. 2). When the range time is up, the clock is stopped after a fixed delay of about 8 μs, allowing the stop interpolators to complete the conversion of the stops arriving toward the end of the time range. At the same time, the ready latch is set indicating that data is ready for readout (Fig. 4, lines N, O, and P). Any of the twelve stop channels can be read out, by addressing a 24-bit data selector, into the arithmetic unit (Fig. 2), performing the following arithmetic operation:

$$T_n = T_0 (N_{st} + 256N_n - N_{spn}) \qquad (1)$$

T_n is time between the start and the n^{th} stop, T_0 an incremental resolution constant (T_0=78.125 ps), N_{st} the reading of the start interpolation counter and N_{spn} and N_n are the reading of the interpolation and "coarse" stop counters of the n^{th} stop channel. From the arithmetic unit the data is either routed to the CAMAC dataway or to the front panel connector to external register depending on the readout mode selected. The status of the stop latch can be also read out. One bit of the 24-bit status word is assigned to each of 12 latches.

Basic readout and control logic is shown in the block diagram (Fig. 3). CAMAC control logic contains a function and subaddress decoder, circuits for interrupt and status response (L, Q and X) and clear. All the CAMAC functions recognized by the timer are also shown.

The logic for data transfer to the external FIFO register is shown in the lower left part of Fig. 3.

Each start event accepted by the timer generates a data ready regardless of how many stops (if any) have been also accepted within the time range. The first step in data transfer is to shift the FIFO register by one (blank) word in order to space the new data from the preceding event. The next word is the content of the status register. After that, the logic scans automatically the stop channels. Only the stop channels containing data are sequentially transferred to the FIFO register. Thus the longest event requires 14 words of register space (a blank, status and 12 stops) and the shortest one only two words (a blank and status word). This program of selective serial readout is run by a pulse generator advancing a binary counter, which in turn controls an address selector.

Discussion of Test Results

Repeated measurement of a constant time interval is shown in Fig. 5 as an example of typical distribution of events in an external storage memory. All 12 stop sections of the timer are quite uniform and, providing that the start and stop interpolators are properly aligned, the distributions are quite similar. The theoretical channel profile (i.e., distribution probability function) is a triangle, p(t), illustrated in Fig. 6. Such a distribution is characteristic for measurements where the reference and the measured quantity are uncorrelated. The base of the distribution triangle should stretch to the centers of the two adjacent memory channels, separated in this case by t_0=78.125 ps in real time. If A is the address of the center channel and t_0 channel calibration, the measured time is $t=At_0$. Since the end of t is shown falling right under the top of the channel profile, where the probability is 1, each time an interval t is measured, the event should be added only to the address A of the processor memory, increasing its content by one. In an ideal case [distribution p(t)], all events should be accumulated in only one memory location (A). Real channel profiles have the base stretched more than t_0 on each side [$p_a(t)$, $p_b(t)$ and $p_c(t)$]. The distributions $p_b(t)$ and $p_c(t)$ intersect at the point m under the peak of the distribution $p_a(t)$. Therefore, although the majority of identical events t are stored at the location A of the processor memory, a fraction m of total events will be stored in the memory location A+1 and another fraction m of total events in the memory location A-1. Such a case is shown in Fig. 5, where A=400 and m=0.18.

The stretching of the channel profile base is caused by imperfect alignment of the start and/or stop interpolator (i.e., the interpolation constant is different from K), and due to the nonlinearity of the time-to-digital conversion and noise in the interpolators. For the distribution shown in Fig. 5, the spread of the measured time is mt_0 = 14 ps.

If the measured time interval t (Fig. 6) is increased by Δt, the three distribution functions are crossed at points a, b, and c. Consequently, N measurements of the same time interval t + Δt result in distributing the events into three locations of the data processing memory (A, A+1 and A-1), each storing N_a, N_b and N_c events, respectively. The total is a sum of all events $N=N_a+N_b+N_c$. Assuming that the three distributions are identical, it follows:

$$N_a/(t_p-\Delta t)=N_b/(t_p-t_0+\Delta t)=N_c/(t_p-t_0-\Delta t) \qquad (2)$$

from which a fraction Δt of the measured time t, smaller than the LSB calibration of t_0=78.125 ps of the timer, can be calculated:

$$\Delta t/t_0=(N_b-N_c)/2(N_a-N_c) \qquad (3)$$

Eq. (3) was used in the calculation of thermal drifts shown in Fig. 7, from the measured data taken when the timer stability was tested at various temperatures. Gradual cooling from 36°C to room temperature indicates an average drift of 2.7 ps/°C and a very good uniformity among the 12 stop channels.

Long term thermal drift has been also recorded for a period of a week. Three measurements a day were made and the ambient temperature recorded. A very small time drift was observed, barely showing only daily temperature cycle effects. Virtually no aging effects or permanent time drift was observed in any of the 12 channels.

The stop channels were also tested for a possible timing error or broadening of the distribution function due to mutual interference. In measuring crosstalk, one stop channel was tested at a time. First, a constant time interval was measured when all other stop channels were not operating. Next, high rate random stop pulses were applied to the two stop channels adjacent to the tested one. Very small shift in the measured time was observed. The third measurement was made after the disturbing signals were removed from the adjacent channels in order to verify that the original reading was repeated. The results are shown in Fig. 8.

Linearity of time measurement was also tested by running the timer with start pulses 60 μs apart and random stops. An external 4096-channel memory was available for the accumulation and display of the data, covering only a small, 320 ns wide, initial section of the 10 μs time range. The result is shown in Fig. 9a. The beginning of the spectrum shows a small transient due to the interference of the start circuit in enabling of the stop input. Expanded vertical scale of the same spectrum in Fig. 9b shows no visible structure (except for the initial portion explained above). Until more thorough numerical analysis is made, it appears that the scattering of data is within the statistical limits.

Acknowledgements

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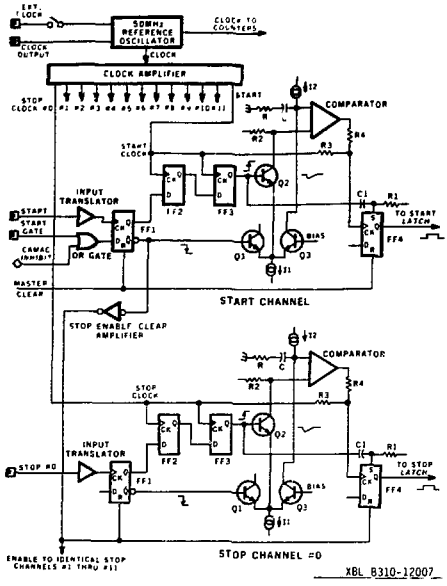

Fig. 1. Block diagram of multichannel interval timer interpolators. The start and one of the twelve stop interpolators are shown.

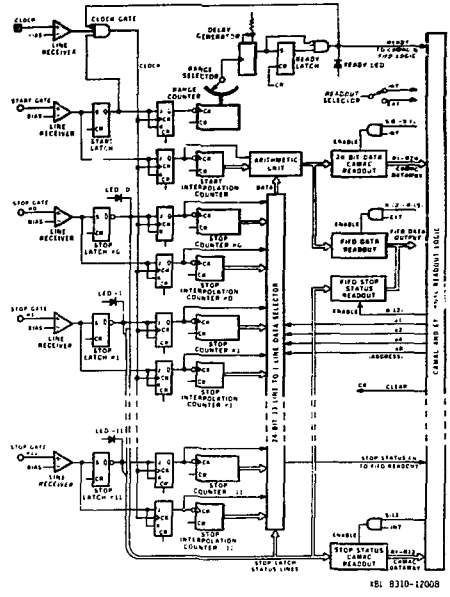

Fig. 2. Timer's digital module block diagram containing counting and logic circuits.

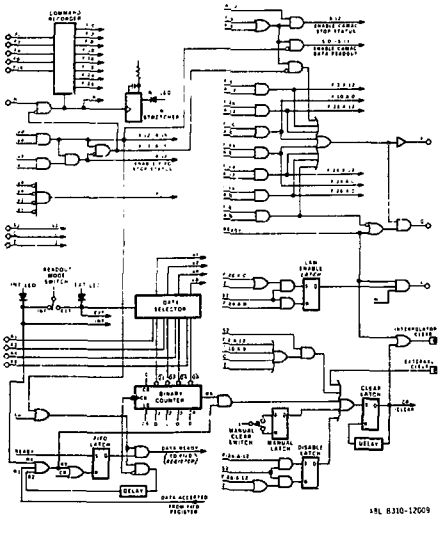

Fig. 3. Timer's CAMAC and FIFO readout block diagram.

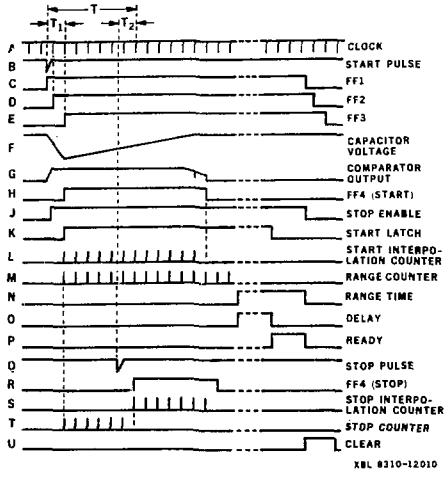

Fig. 4. Basic timing diagram.

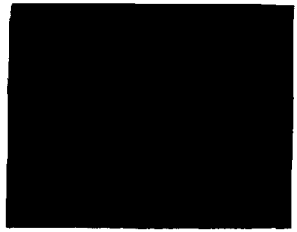

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Fig. 5. Multiple measurements of 31.25 ns time intervals generated by a delay line. Horizontal calibration: 78.125 ps/channel; spread in the adjacent channels indicates total jitter of ±14 ps.

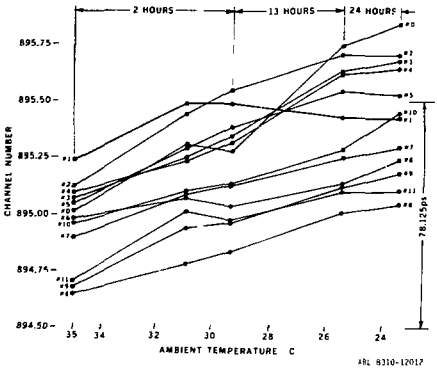

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Fig. 7. Timing error due to the ambient temperature variation.

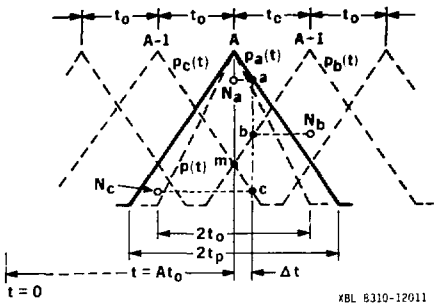

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Fig. 6. Illustration of ideal and actual triangular channel profiles (i.e., distribution probability functions) of the timer. Time can be resolved to a fraction of the channel width t_o = 78.125 ps.

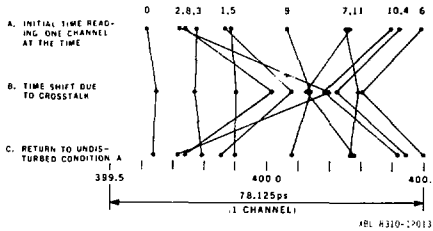

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Fig. 8. Timing error due to crosstalk. High repetition random stops were applied to adjacent channels during the measurements B. Rows A and C show timing before and after disturbance.

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Fig. 9a. Distribution of random stops in 320 ns time range following the start. Incremental resolution: 78.125 ps/channel.

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Fig. 9b. Expanded vertical scale of Fig. 9a showing small differential nonlinearity of the timer.

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