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Conf-910340--46

ANL-HEP-CP--91-48

DE91 015545

DEVELOPMENT OF A CUSTOM MONOLITHIC DEVICE FOR DATA ACQUISITION FROM A SCINTILLATING CALORIMETER AT THE SUPERCONDUCTING SUPER COLLIDER

T. Ekenberg, J. W. Dawson, R. L. Talaga,
A. E. Stevens, W. N. Haberichter

Argonne National Laboratory
High Energy Physics Division
Argonne, IL 60439

ABSTRACT

A clock-driven continuous sequential write/random read data acquisition architecture for a scintillating calorimeter at the SSC is presented. Simplicity of design and operation as well as potentially dead time-less operation are the motivations of this effort. The architecture minimizes the number of fast control signals, thereby reducing pickup from digital control lines by sensitive analog circuits in the front-end device. This architecture also reduces the logic necessary on the front-end device improving relability and easing design and operation. Operation and design of the front-end device are discussed.

INTRODUCTION

A major challenge in the SSC detector development is the design of efficient data acquisition and trigger electronics under the severe constraints imposed by the high event-rate, stringent power consumption budget, and the radiation damage. The SSC will be operating with a luminosity between 10^{33} $cm^{-2}s^{-1}$ and 10^{34} $cm^{-2}s^{-1}$ and with a beam crossing frequency of 60 MHz, generating 10^8 events per second. Total number of read-out channels will be on the order of 5×10^5. Considerations of response time and hermeticity of the detector forces much of the calorimeter electronics to be located deep inside the detector where they are suspect to high radiation doses as well as forced to be minimized with respect to physical space and power.

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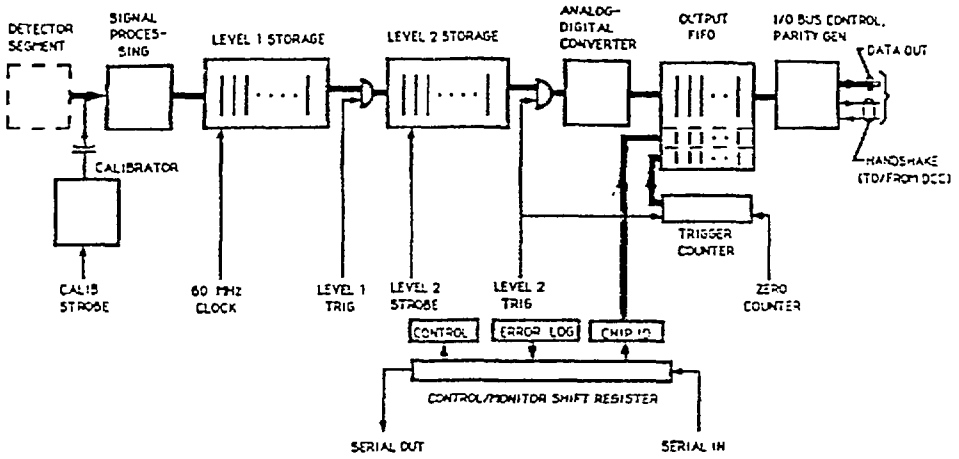

Figure 1: Generic DAQ design for SSC detector. Figure from [1].

In order to design the electronics to be placed in the immediate vicinity of the detector elements one has to optimize with respect to several constraints: power consumption, speed, noise performance, packing density, radiation damage, and a high degree of multiplexing to reduce cable volume. Many of these constraints are inversely related to each other, and there are always trade-offs to be made. Another important design consideration is the effect of a large number of high speed digital control signals switching in the vicinity of sensitive analog devices.

A generic DAQ architecture for SSC detectors has been developed in the High Energy Physics community and is outlined in Fig. 1. In this architecture the detector signal is routed into a signal processing unit and through the level 1 pipeline/storage device and is transferred to level 2 storage on a level 1 trigger. The signal is held until a level 2 trigger accept arrives. At this time it is digitized and stored in the output FIFO, after which the signal is shipped to the level 3 processing. The high event-rate of the detectors (10^8 events/second) dictates that the event reduction done by the trigger must be on the order of $10^3 - 10^4$ for the level 1 trigger, $10^1 - 10^2$ for the level 2 trigger, and another factor of $10^1 - 10^2$ in the level 3 processing. This results in approximately 100 events/second written to permanent storage.

In this paper we propose an architecture for a scintillating calorimeter DAQ. It consists of a front-end device, which may be implemented as a VLSI circuit, that stores the data and digitizes valid level 2 events with an on-board ADC, and a central control unit that interfaces the front-end device to rest of the DAQ and to the trigger system. This architecture limits the number of fast control signals to the front-end device to two, and minimizes the logic on the front-end device.

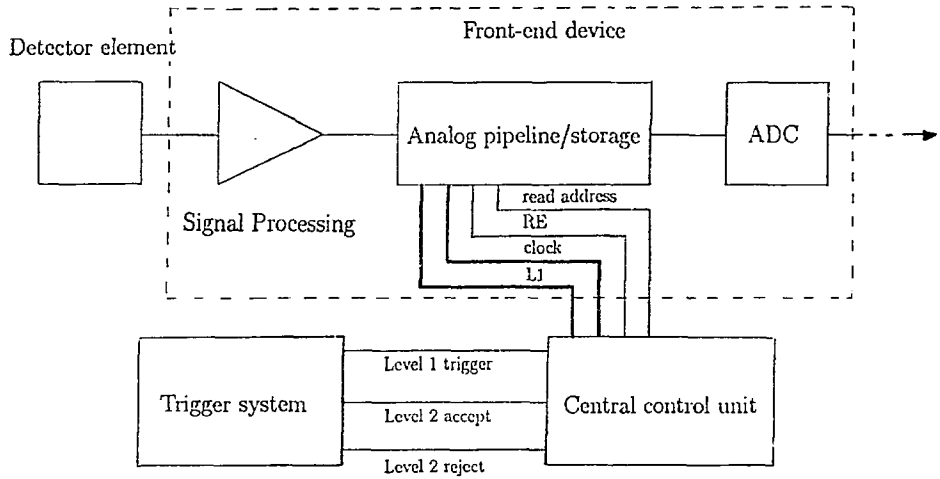

Figure 2: Schematic of proposed architecture. Border of front-end device outlined as well as the flow of control signals from the central control unit (CCU) and trigger system. Fast control signals are marked with heavy lines.

ARCHITECTURE

The motivation for the proposed architecture is simplicity. In order to ease design, trouble-shooting, and operation of the entire calorimeter system, an architecture has been developed that minimizes the number of fast and slow control signals, and reduces the amount of logic on the front-end device. The only fast signals necessary are the global clock and the level 1 trigger. Logic at the front-end device is limited to an array write-selector, decoding logic for the loading of the read addresses, and some logic necessary for diagnostics.

The reduction in total number of control signals is important in order to minimize the cable count, but the implementation of a front-end device with only 2 signals that must be driven at 60 MHz also improves noise performance of the system. This is the case since mixed analog/digital signal systems are highly sensitive to cross-talk between the high-frequency digital signals and sensitive small-signal analog circuits. The motivation of reducing the controlling logic on the front-end device is two-fold. Since all front-end devices for the calorimeter would be the same, significant savings in silicon area can be accomplished by collecting all controlling logic in one place. Reliability is also improved by implementing only very simple functions on the front-end device which will be largely inaccessible except during special circumstances. This system will be easier to operate, trouble-shoot, and repair with all control logic in a central location.

The architecture is implemented with a front-end device and a central control unit (CCU), as shown in Fig. 2. The front-end device is a mixed analog/digital signal IC, or set of ICs. The controlling signals from the CCU to the front-end device

are the Level 1 (L1) trigger, global clock, Read Enable (RE), and the read address word. Included in the front-end device is the signal processing, the analog pipeline/storage, and the ADC.

The front-end device of the proposed architecture consists of eight arrays of analog storage sites. The storage sites are capacitors that record and store charge or voltage signals. Each array is a 128 elements deep pipeline, *i.e.* a 2 μs deep memory that holds the data until the level 1 trigger makes its decision. Each array is controlled locally for writing and reading by a 128 bit long loadable shift register. This shift register selects elements for sequential write or random read operations as instructed by the central control unit.

OPERATION

All interfaces between the trigger system and the DAQ system, as well as between level 3 processing and the front-end device of the DAQ, are handled by the CCU. When the calorimeter system is enabled for data acquisition, the CCU enables the front-end devices by write enabling the first array. The shift register associated with the write selected capacitor array is clocked by the 62.5 MHz global clock, writing each array element in sequence. When the write pointer reaches the end of the array, it wraps around and starts at the beginning of the array again. This continues until a level 1 trigger arrives at the CCU. The CCU logs the trigger and issues a L1 trigger to the front-end devices. At this time the array selector is incremented, write enabling the second array, and writing commences with the first element of the second array. The analog data is continuously written to the second array until the next L1 trigger arrives. At this time the array-selector is incremented again and writing continues at the beginning of the third array. In this manner each array is written in order, and when the last array contains a L1 trigger, the write pointer wraps around to the first array again. See Fig. 3 for functional lay-out of front-end device.

The L1 trigger is a fast signal and its arrival must be precisely defined and timed since it indicates valid data a fixed-time interval preceding its arrival. The CCU maintains the correct timing relationship of the L1 trigger with respect to the level 1 trigger signals. When the level 2 trigger arrives at the CCU it is processed and the storage site address word corresponding to the triggering event is generated. This address word is presented to the front-end device and is latched at the front-end device when the CCU issues a read enable (RE) to the front-end device. RE and the read address lines are slow signals. When the address is latched the selected site is connected to the ADC and the value digitized and outputted through to the level 3 processing. This system is flexible with respect to the number of storage sites to be digitized since this can be changed in the CCU and the front-end devices remain uneffected. This is important since the actual number of samples needed for baseline subtraction is not yet fixed.

This operation is dead time-less in our application. An event rejection ratio in the level 1 trigger system of 10^3 to 10^4 produces level 1 triggers on the average

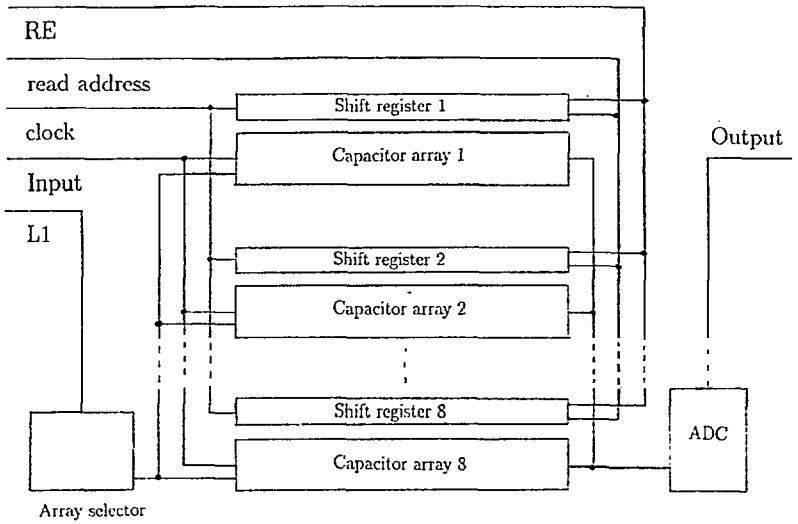

Figure 3: Functional lay-out of front-end device. Each capacitor array contains a write select decoder and a read address decoder. Input is a analog signal from the detector and output is the digitized signal going to level 3 processing.

between every 16 to 160 μs [3]. Level 2 trigger decisions are made approximately every 10 μs with a maximum latency of 50 μs. This will allow continuous operation with eight storage arrays since level 2 decisions will be made before the array comes up in the write queue again. No special level 2 reject is necessary since the storage arrays are just over-written every time they come up in the write queue.

Since the local shift registers are cleared on every L1 trigger the device is automatically re-synchronized at that time. A local counter on the front-end device tracking the global clock outputs its value for each valid event, allowing for a global check on the timing integrity of the data at the level 3 processing. If corrupt timing data is found the event is discarded without any need for re-synchronizing of the front-end devices. This means that corrupt data is always isolated to one event and does not effect subsequent events.

DESIGN

Several different schemes are currently being investigated for implementing the front-end device. One way is to fold the signal processing and storage unit into one by integrating directly on the storage capacitors. This approach has been investigated previously by Anghinolfi, et.al. [2]. Integrating directly on a storage capacitor is a very attractive option in a scintillating calorimeter where the current pulses from the photo multiplier tubes are expected to be confined to less than 16 ns, the time between beam-crossings. This can be implemented with a high speed operational amplifier with the

storage capacitors switched in and out of its feedback path every 16 ns. The inverting input of the op amp is connected directly to the base of the photo multiplier tube.

One can also use a time continuous signal processing unit followed by a sample and hold circuit. In this approach a pre-amplifier converts the current signal from the detector to a voltage signal which is processed through a shaping amplifier. The output of the shaping amplifier is then sampled at discrete time-intervals and stored on a analog storage device pending digitization. This is especially well suited for systems with slow signals that will be extended over many beam-crossings at the SSC, like liquid Argon calorimeters.

To keep the data on the same physical storage location during the entire time between initial write and digitization is important since every transfer introduces a degradation of analog data. This is accomplished in our design by using the capacitor arrays as the initial memory element as well as both level 1 and level 2 storage. The transfer of signals between level 1 and level 2 is virtual, and since no physical signal is transferred no dead time is introduced at this step.

SUMMARY

A clock-driven continuous write/random read DAQ architecture that limits the number of fast control signals to two and minimizes the logic at the front-end is presented. This improves reliability and makes design and operation simpler.

The interface between the front-end devices and the trigger system and the level 3 processing units is the central control unit (CCU). The CCU controls all front-end device of the calorimeter system. Each front-end device consists of eight capacitor arrays and a few simple logic functions. During data acquisition the data is being written to the write selected array every 16 ns. The array is 2 μs deep and is continuously being over written until a first level trigger arrives. The next array is then write enabled and writing continuous at the beginning of that array. This is repeated for every level 1 trigger until all eight arrays are full. At this time the writing continues on the first array again.

The operation of this architecture is dead time-less in our application and the front-end devices are automatically re-synchronized on every level 1 trigger by virtue of always start writing at the beginning of each array. This isolates events with corrupted timing information from subsequent events, and no special re-synchronization must be carried out.

ACKNOWLEDGMENTS

Work supported by the U.S. Department of Energy, Division of High Energy Physics, under contract W-31-109-ENG-38.

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