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THE MPS II DRIFT CHAMBER SYSTEM*

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Summary

The MPS II detectors are narrow drift space chambers designed for high position resolution in a magnetic field and in a very high particle flux environment. Central to this implementation was the development of 3 multi-channel custom IC's and one multi-channel hybrid. The system is deadtimeless and requires no corrections on an anode-to-anode basis. Operational experience and relevance to ISABELLE detectors is discussed.

The MPS II Project

The MPS

The BNL MPS (Multiparticle Spectrometer)[1] is a large 10 Kg "C" magnet shown in Fig. 1 with a plane view in Fig. 2. It has been in operation since 1975

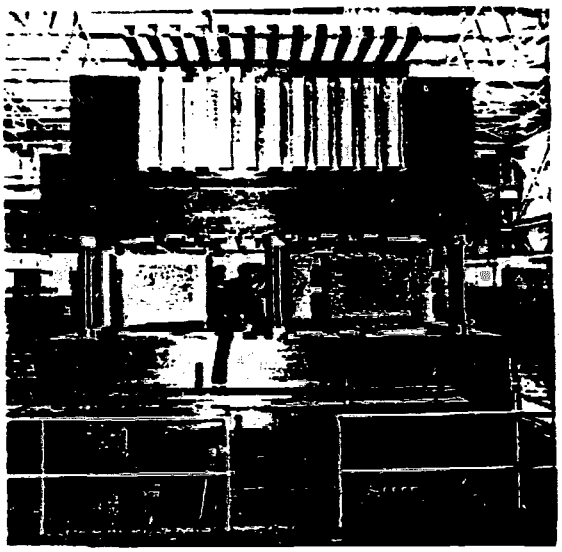

Fig. 1. Brookhaven Multiparticle Spectrometer Magnet

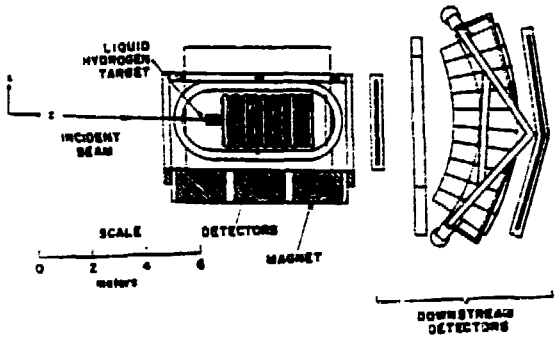

Fig. 2 Plane view of MPS with detectors

as a facility instrumented with magnetostrictive spark chambers, PWC's, scintillator and Cerenkov hodoscopes and a variety of user-provided detectors including shower counters and transition radiation devices. However, since its initial operation, the greatest physics interest has fallen into the sub-nanobarn cross section region. Therefore, replacement of the spark chambers with detectors capable of efficient operation in rates ≈ 100 times higher became essential. It was also desirable to improve the position resolution and absolute accuracy of the tracking detectors.

Charged Particle Detector Goals

At the outset of this work a substantial amount of computer simulation was used to help optimize detector configurations best suited to the event reconstruction software. In addition, hardware "deficiencies" that impact on computing time were to be minimized. With this background the following set of goals was generated.

- Tracking detector must be capable of very high event rates - electronics to be deadtimeless.
- Good position resolution in a magnetic field with no or very limited position-dependent corrections.
- Minimum need to calibrate - good system stability as a function of channel-to-channel t_o, time vs. position slope and linearity.
- Compact and reliable - suitable for large detectors with poor accessibility such as inside of a 4π calorimeter.

Drift Chamber Design

The drift chamber design was determined by the need to operate at very high rates in a magnetic field while minimizing any need for track position or angle-dependent corrections. It was also important from event reconstruction considerations to attempt to resolve the right-left ambiguity and to generate 2-dimensional vectors locally where curvature in the B field is negligible. A geometry that satisfies all these criteria is shown in Fig. 3. These "X" anode, field and cathode wires lie along the B field lines. By arranging 3 such anode planes only 1.2 cm apart, no curvature is seen within the chamber resolution. Also by staggering the anode position in the X_3 plane resolution of the right-left ambiguity will occur in 70-80% of the tracks locally when fits allowing up to 2σ deviations are done.

The full module consists of the triple X anodes, a pair of Y anodes, one of which is displaced by a drift distance, and a U and a V anode plane which are 30° to the Y (Fig. 4). Therefore locally within a module it is possible to reconstruct 3 dimensional vectors of the particle track. It should be noted that in X the reconstruction finds one or more vectors per hit. If more than one vector is found, in general only one is correct. The correct vector is selected by matching with the vectors in adjacent modules. In Y there are always 4 vectors generated. However there is no curvature in Y so that many of the calculated vectors can immediately be discarded because the track must come from the vicinity of the target.

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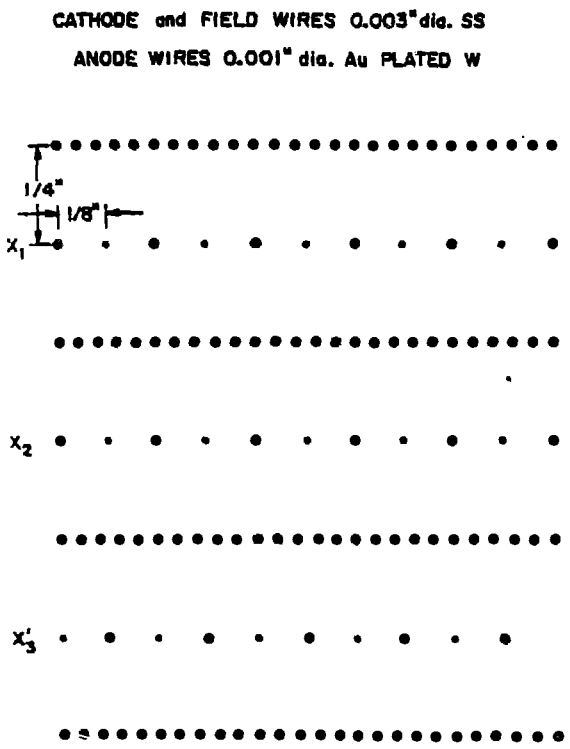

Fig. 3 Three X planes of an MPS II drift chamber module.

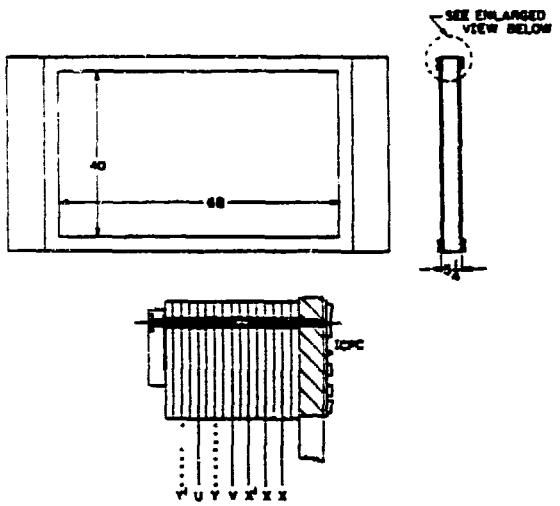

Fig. 4 Full drift chamber module with 7 anode planes.

One of the important features of this drift chamber system is the electronics developments that allow all channel-by-channel circuit elements to be mounted directly on the chamber frame. This circuitry is shown in Fig. 4 and is called the ICPC. Each anode lead is attached to a short flat pigtail cable to the ICPC. On the ICPC are the transresistance amplifiers, pulse shapers, comparators, digital delay and registers required for each anode. Figure 5 is a picture of the complete module with ICPC's, cable harnesses and interface electronics. Figure 6 is a plot of drift time vs. track position in a 10 Kg field. In this gas mixture

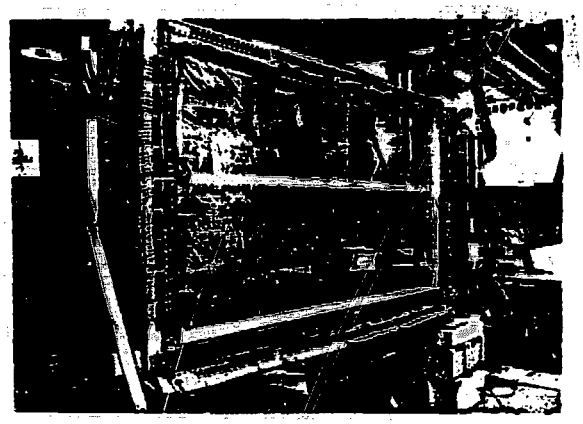

Fig. 5 Picture of completed drift chamber module with ICPC's, cable harnesses and interface circuitry.

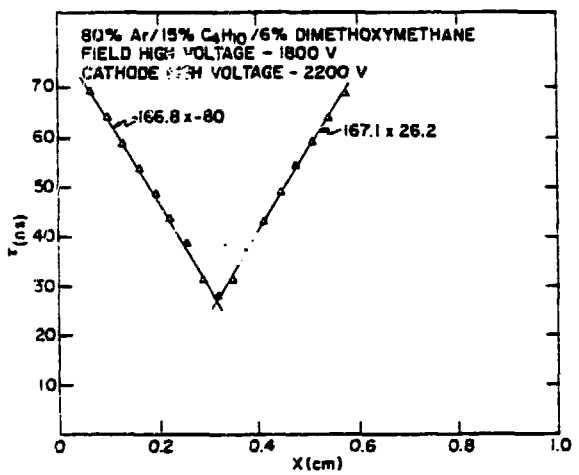

Fig. 6 Drift time vs. track position in a 10 Kg B field.

the drift velocity is fully saturated and the drift time vs. position in linear at the 100u level from the anode to near the field wire. Figure 7 is a plot of the HV plateau where the electronics threshold is 4 ua.

Electronics

The desire to build a system easily expandable to ISABELLE-sized detectors capable to handling ISABELLE event rates, i.e. deadtimeless electronics and requiring an absolute minimum of variable parameters such as time-to-digital conversions that are different for each readout channel led us to develop a number of custom integrated circuits and hybrids. Figure 8 is a block diagram showing 3 custom IC's and a hybrid. Each of these circuits contains 4 channels of electronics. The amplifier specifications are given in Table 1.[2] It should be noted that the rms noise level is low enough that comparator thresholds as low as 1 ua are possible. Figure 9 shows 1 channel of the hybrid. This shaping

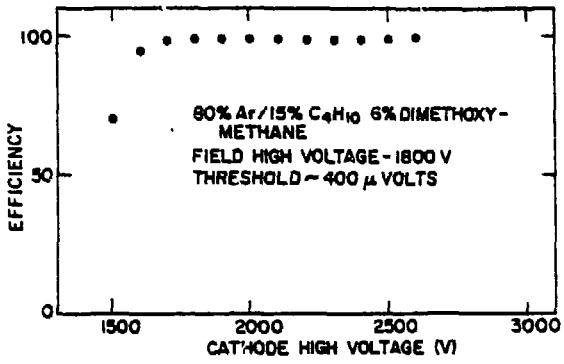

Fig. 7 High voltage plateau for a typical drift chamber.

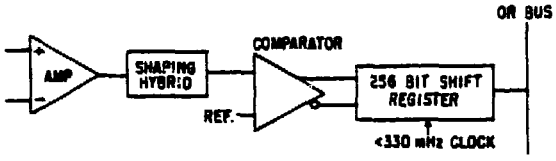

Fig. 8 Electronics block diagram. All of these components are mounted on the ICPC.

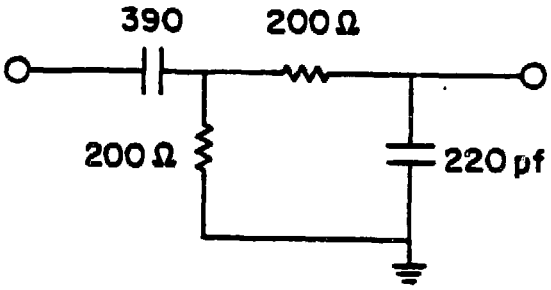

Fig. 9 Pulse shaping hybrid circuitry

network was hybridized to conserve space on the ICPC. A discrete implementation would be much less expensive. Table 2 lists relavent performance of the comparator IC. The device was designed with ≈ 6 mv of hysteresis to improve the circuit stability in large and somewhat noisy situations. The output level swings were determined by the CMOS digital delay-register drive requirements. An alternate version of this comparator having similar specifications but ECL output is available as MVL 406.[2]

The third IC in this drift chamber electronic system is a state-of-the-art device. It is functionally a 4-channel, 256-bit shift register (SR) that is fabricated with the CMOS silicon-on-sapphire (SOS) process.[3] It is capable of acquiring data at > 330 MHz. Figure 10 is a block diagram of the internal structure of one channel. To achieve the required speed, the device is internally an 8 phase register. This is the maximum speed each phase runs is 330 MHz ÷ 8. To provide practical external clock risetime and amplitude levels, the clocking is done with a 4-phase clock driver. This clock driver then must run at no more than 330 MHz ÷ 4 or 83 MHz, a much simpler task than clocking at up to 330 MHz. A consideration of great importance in a multiphase shift register is the relative delay between the clock

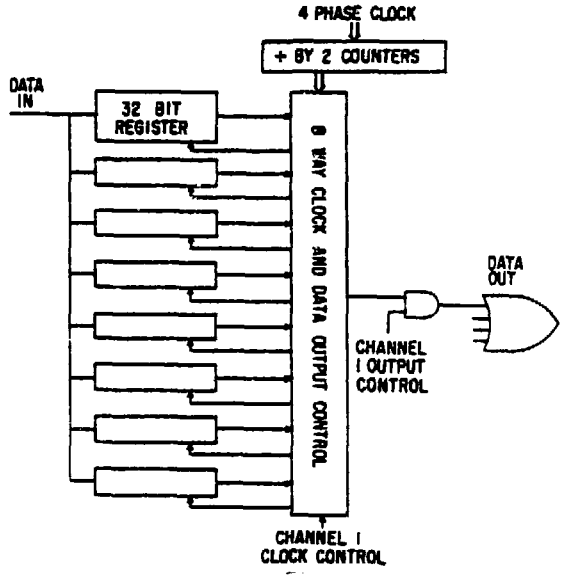

Fig. 10 Single channel of the 8 phase shift register.

pulses and the time data is actually acquired in each of the 8 phases. This has been measured at 250 MHz to be 4 ± .5 ns in absolute range on a large number of devices. The standard deviation of this variance, a number of greater importance in drift chamber applications, is ± .3 ns.

The 4-channel SR with control (enabling) circuitry is shown in Fig. 11. During data acquisition, 4 "ones"

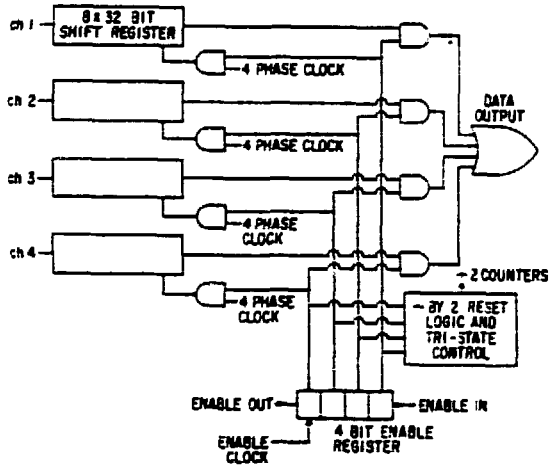

Fig. 11 4 channel shift register with enable circuitry.

are in the enable register. This allows the 4-phase clock to drive all 4 channels of the SR. The data is acquired by running this 4 phase clock at 250/4 = 62.5 MHz. Precisely 1 μs after an event of intarest has occurred, the 4-phase clock is stopped. Channels with data will then have a string of "ones" somewhere in the last 32 elements in the SR, the position of the furthest 1 being a precise measure of the drift time for that drift chamber cell. Table 3 gives some important specifications for this shift register. Data is extracted by use of the enable circuitry which allows selection for clocking of one channel only and gating of the last register element onto a common "OR" bus. Once a channel

has been selected for readout, the 4-phase clock is turned on at < 20 MHz for 3½ primary ticks and the "OR" bus data is digitized by an encoder common to one whole plane of the chamber. In this way the data from a whole X plane (273 anodes) appears on a single coax cable. In addition, 2 cables bring the 4-phase clock to the plane and an additional enable-in coax and enable-clock coax completes the communication with the plane. Thus data and control for 273 (or more for larger chambers) is compacted to 5 coax cables. It should be noted that the enable and clock cables are common for the whole module. Figure 12 is a picture of an ICPC containing the electronics for 64 channels.

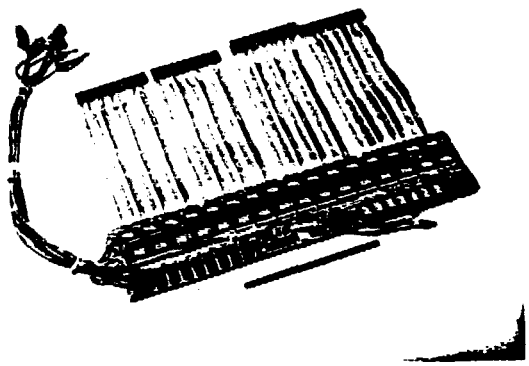

Fig. 12 64 channel ICPC with input pigtail

Test Results

Pulser

Each ICPC has a capacitively coupled strip across the input lines to the amplifier. To test the overall system timing variations, a pulse is applied to this strip. The rise time and amplitude of this pulse simulate a drift chamber signal of > 40 ua. With this pulser scheme it is possible to measure the reference time t_o for each channel. With only moderate care in component selection it is possible to maintain the t_o variation on a plane to within 4 ns. In addition, one has a quantization error which for the case where the clock is unsynchronized to the pulser or clock stop pulses should on average produce an rms of .34 time bins (4 ns each) if there are no other sources of timing jitter. The actual measured rms value averaged over a typical plane (273 wires) was .44 time bins.

Pulser data was taken over a period of several weeks and the t_o's for each channel were compared. No shift of more than .25 time bins was observed. This remarkable stability is of course expected. Having measured it, it is most reassuring and would suggest that operation of much larger drift chamber systems for ISABELLE experiments is viable.

Particle Tracks

As of this writing, 6 full modules have been built, but there has not been a beam of particles available from the AGS. Therefore all track reconstruction has been done from cosmic ray triggers. Most planes will operate with a comparator threshold of 2 ua as referred to the input. Under these conditions little pickup of the 4-phase clock is observed. When clean single tracks (μ's) are observed, the pattern recognition already finds unambiguous point-slope in 70% of the events with only 2 modules. This is without B field. We expect similar results with 3 modules in a B field.

Relevance to ISABELLE Detectors

The MPS II project, in addition to its obvious physics potential, may be regarded as a prototype test-bed for an ISABELLE detector. The event rate loading objectives are similar. At MPS II the raw beam of 10^7 particles passes through the active area of the drift chambers. If this region can be made to work efficiently, as it is designed to do, then a major step will have been made to handling the 10^7 events/sec rate expected at ISABELLE. This was a major design consideration and should be optimized by an appropriate selection of the filter network parameters because otherwise the system is dc coupled and deadtimeless.

The compact packaging this highly integrated system uses would make detectors of > 10^5 drift wires feasible. With propagation delay selection, t_o's can be matched to better than 2 ns so that individual channel t_o corrections need not be made. The time measurements are done strictly digitally by a common clock so that only one drift time-to-digital slope parameter is required for the whole system. Finally this highly integrated electronics should prove very reliable since there is an average of less than 1.5 active components per channel.

TABLE 1

BNL TRA401
AMPLIFIER CHARACTERISTICS[2]

Characteristics	Minimum	Maximum	Units
Input Type	True Differential		
Input Noise (RMS)		0.25	uA
Input Resistance		80	ohms
Input Protection		1.13×10^{-4}	J
Transfer Impedance	17		Kohms
Delta Transfer Impedance	-10%	+10%	
Gain Stability		0.25	%/°C
Output Impedance		50	ohms
Rise Time		4.4	nsec
Max. Linear Output	1.2		Volts
Propagation Delay		10	nsec
Delta Propagation Delay		1.5	nsec
Temperature Range	0	50	°C
Supply Currents			
+5.5 V ± .1		65	mA
-2.5 V ± .1		45	mA

TABLE 2

BNL MVL400
DISCRIMINATOR CHARACTERISTICS[2]

Characteristics	Minimum	Maximum	Units
Input Resistance	3		Kohms
Input Z Threshold Control	1.5		Kohms
Threshold Control Range (1:1)	0	1.5	Volts
Threshold Hysteresis	6	10	mV
Threshold Match		5	mV
Crosstalk between Inputs of Channels		-40	dB
"0" Logic Level		1.8	Volts
"1" Logic Level	+3.5		Volts
Output Response Time		4.4	nsec
Slewing		3	nsec
Double Pulse Resolution		20	nsec
Input Capacitance		6	pF
Propagation Delay	14.5	17.5	nsec
Operating Temperature	0	50	°C
Supply Currents			
+5 V		200	mA
-5 V		22	mA

TABLE 3

4 CHANNEL 256-BIT SHIFT REGISTER

Clock Frequency (Effective)	DC to > 330 MHz
Phase to Phase Delay Match	< 1 ns
Maximum Readout Frequency (with 16 way or tie)	> 20 MHz
Power Dissipation at 250 MHz	< 200 mw

References

1 Members of the MPS Group are: A. Etkin, K.J. Foley, M.A. Kramer, S.J. Lindenbaum, R.S. Longacre, W.A. Love, T.W. Morris, E.D. Platner, V.A. Polychronakos, A.C. Saulys, Y. Teramoto, C.D. Wheeler.

2 LeCroy Research, Spring Valley, New York.

3 Craig Wolfson, RCA, Solid State Division, Sommerville, New Jersey.