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A PRECISION CRYOGENIC TEMPERATURE DATA ACQUISITION SYSTEM*

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ABSTRACT

A Multiplexed Temperature Data Acquisition System with an overall precision of ±25 PPM has been designed using state-of-the-art electronics to accurately read temperature between 2.4 K and 600 K from pre-calibrated transducers such as germanium, silicon diode, thermistor or platinum temperature sensors.

INTRODUCTION

Included in the design of the BNL 24.8 KW helium refrigerator are about 400 temperature transducers of different types (diodes, germaniums, platinums and thermistors) used to read temperature between 2.4 K and 600 K. Due to the high accuracy demanded of these devices, an ultra high precision temperature data acquisition system is necessary to resolve small temperature differences.

Because of the high number of transducers, a multiplexed system is necessary to keep the system compact, thus reducing hardware costs while preserving the precision of the system.

A block diagram is shown in Fig. 1. It consists of four front ends (3 interfaced to the refrigerator and one at the compressor facility) which read temperature in analog form, digitize the signals and ship them to an 8086/8087 based microcomputer. There the raw data is linearized by use of corresponding polynomial coefficients and finally shipped to an ANATEC 11/34 process control computer for further processing. A maximum of 168 temperature transducers can be processed by one front end.

SYSTEM DESCRIPTION

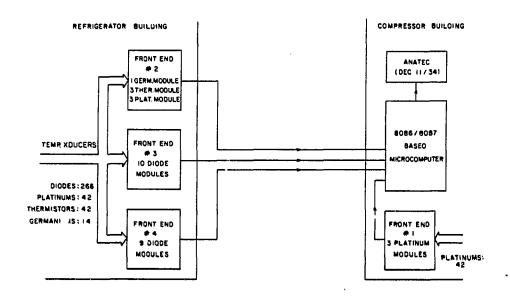
Front End Section

Each front end (Fig. 2) consists of a EURO-CARD crate which holds 12 analog input boards and a precision reference voltage module. A MULTIBUS

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ANALOG MUX 14 TEMP. XDUCERS MODULE #1 12 V/F INPUTS 8085 BASED MODULE MICROCOMPUTER 14 TEMP XDUCERS' ENA DECODER TO 8086/8087 SERIAL OUT BASED MICROCOMPUTER 12 ENABLE LINES 4 LINES 4 DECODER LINES 14 TEMP. MODULE

Fig. 1 - System Block Diagram

Fig. 2 - Typical Front End Block Diagram

XDUCERS

PRECISION

REF. VOLT

ENA DECODER

2.500 V

card cage contains an 8085/8232 microcomputer card and two digital cards interfacing signals between the microcomputer card and the analog modules.

Analog Section

An analog input board consists of low level voltage analog multiplexers, amplifiers, an ultra linear voltage to frequency converter and
optical isolators used to separate grounds between the analog and digital sections. The analog board can connect to a maximum of 14 temperature transducers of the same type since gain and offset are fixed on a
per board basis.

The precision reference voltage module delivers an ultra stable 2.5 volts to the 12 analog modules which in turn each produce a 10 µA constant current (1 mA in the case of platinum transducers). The constant current signal is multiplexed by 16 analog switches, holding the value to within a precision of about ±10 PPM. Fourteen of these outputs are connected to the temperature sensors via a 4 wire connection in the case of platinum and germanium transducers or 2 wire in the case of diodes and thermistors. The first of the other two multiplexers on the board is used for switching the constant current into a precision resistor to compensate for drift, and the second to compensate for amplifier drift and offset. An intentional V_{add} is added to the output voltage before the V/F converter to insure that offset and drift voltage is the same polarity as the signal since the V/F converter input is unipolar.

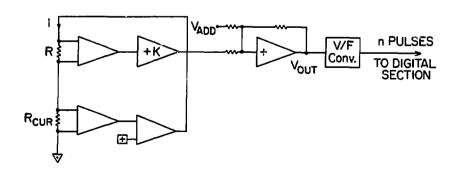
Fig. 3 shows a simplified representation of the analog circuit, in which I is the constant current and multiplexed R is either one of the 14 unknown transducers, the reference resistance, or the offset resistance. From Fig. 3:

$$v_{out} = K(RxI) + V_{(off + drift)} + V_{add} . \tag{1}$$

$$v_{zero} = v_{(off + drift)} + v_{add}.$$
 (2)

In case of R = Rref:

$$v_{ref} = K(R_{ref} \times I) + V_{(off + drift)} + V_{add}.$$
 (3)



V_{OUT} = K(Rx!) + V_(OFF + DRIFT) + V_{ADD}

Fig. 3 - Simplified Representation of the Analog Circuit

In case of R = Rx:

$$V_{Rx} = K(Rx \times I) + V_{(off + drift)} + V_{add}. \tag{4}$$

Subtracting (2) from (3) and (2) from (4) yields:

$$V_{ref} - V_{zero} = K(R_{ref} \times I)$$
 (5)

$$V_{Rx} - V_{zero} = K(Rx \times I)$$
 (6)

Dividing (6) by (5) yields:

$$Rx = \frac{v_{Rx} - v_{zero}}{v_{ref} - v_{zero}} \times R_{ref}$$
 (7)

Equation (7) shows that the precision of reading Rx (the unknown sensor) is related to the reference resistance $R_{\rm ref}$, and the precision of the V/F converter which translates $V_{\rm Rx}$, $V_{\rm ref}$ and $V_{\rm zero}$ into pulses sent to the digital section. The voltage to frequency converter used in the analog module exhibits a non-linearity of ± 2 PPM in the frequency range of 100 HZ to 6000 HZ. To make up for lost resolution, a dual counting technique is used as explained in Appendix A.

Digital Section

The digital section contains an 8085 precessor, an 8232 double precision floating point processor, 4 K bytes of program memory, 2 K bytes of data memory, counters, drivers and optical isolators. A memory resident program drives the analog modules, enabling the first of the 16 channels on all 12 analog boards. Amplifier offset is digitized (n_0) pulses and shipped to the digital section. The second channel is activated and encodes the reference resistor voltage which measures the value of the constant current (n_R) pulses. The multiplexer steps through the 14 temperature transducers one at a time which provides (n_x) pulses. After the 16 channels have been scanned, the cycle repeats itself.

The dual counter technique, 2,3 as described in Appendix A, will enable the V/F (n) Pulses and the high frequency (N) pulses to be read at the same time by the processor. A 6 MHZ high frequency clock is used to achieve a resolution of 1 PPM when the counter is gated for a 175 msec period.

By substituting equation (A1) in equation (7):

$$Rx = \frac{n_{x}/N_{x} - n_{o}/N_{o}}{n_{ref}/N_{ref} - n_{o}/N_{o}} \times R_{ref}.$$
 (8)

All mathematical manipulations are done by the 8232 floating point processor using 64 bit double precision arithmetic. The value, R_{ref} , is software trimmed in test, and later fixed in program memory.

The result of the calculation (Rx) for each temperature transducer is serially transferred to the 8086/8087 microcomputer in the form of a 64 bit floating point double precision number along with address and start, stop, and check bits. The check bits are encoded using the cyclic error detecting code defined by the 12th degree polynomial:

$$G(x) = x^{12} + x^{11} + x^3 + x^2 + x + 1$$
 (9)

A total of 89 bits per temperature transducer are transmitted to the 8086/8087 section at 0.5 megabaud rate. Isolated current loop connection permits communication up to a distance of 1000 feet.

8086/8087 Microcomputer Section

The microcomputer section consists of an 8086 Microprocessor, an 8087 Nume.ic Data Processor (NDP), 32 K bytes of static RAM and 120 K bytes of EEPROM of which 8 K bytes are reserved for program memory. The remainder of memory (112 K bytes) is used for temperature transducer linearizing polynomial coefficients which are generated while calibrating each transducer. Each transducer calibration curve occupies 320 bytes of memory divided into 4 segments, each consisting of one breakpoint value and nine coefficients AO through A9.

The 8086 processor is programmed to scan the 4 analog front ends. When a message is detected, the 8086 will check the validity of the message. The address is checked and the polynomials associated with this address are evoked by the 8087 NDP which determines the proper segment and evaluates the temperature from the polynomial:

$$T_{x} = A_{8}(R_{x})^{8} + A_{7}(R_{x})^{7} + A_{6}(R_{x})^{6} + A_{5}(R_{x})^{5} + A_{4}(R_{x})^{4} + A_{3}(R_{x})^{3} + A_{2}(R_{x})^{2} + A_{1}(R_{x})^{1} + A_{4}$$
(10)

The temperature is placed in 16 bit form and transmitted with a 9 bit address to an ANATEC PDP-11/34 processor along with 12 redundant bits for error checking, and one start and 3 stop bits for synchronization.

ANATEC - 11/34 Interface Section

The process computer interface hardware contains 4 K bytes of static RAM in which Tx engineering units data is placed from the 8080/8087 microcomputer section. Each temperature value occupies 16 bits of memory of which 14 bits are mantissa and 2 are decoded for floating decimal point position. The process computer reads and unpacks the word, decodes and places the temperature data in internal float tables which are accessed by the control system.

CONCLUSION

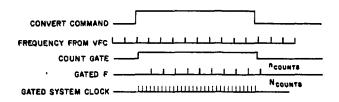
A very high precision multiplexed system for reading temperatures between 2.4 K and 600 K is described. The overall precision of the system is greater than ±25 PPM including variations with time and temperature. The data acquisition system is self calibrating, eliminating the need for adjustment and fine tuning.

Future improvements will increase system precision to ±16 PPM and the polynomial coefficients will be placed on hard disk memory for flexibility. Changing polynomial coefficients will become a simple task when replacement of a temperature transducer becomes necessary. Also front end capacity will be extended to accommodate a maximum of 224 transducers.

APPENDIX A

High Resolution A/D Converter2

The most straightforward method of achieving 1 PPM resolution is to use a 0 to 1 MHZ V/F converter and simply count the number of pulses in a one second period. Unfortunately, 1 MHZ V/F converters with



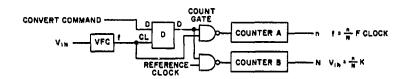


Fig. Al - V/F Converter Timing Diagram

nonlinearities in the PPM range are simply nonexistent. An alternative is to use a low frequency V/F which produces (n) pulses and to feed clock pulses (N), at a rate of 1 MHZ or higher into the counting process. A D-type flip-flop can be harnessed to the count gate of a dual counter scheme, to synchronize the clock with the V/F converter pulses as in Fig. Al. The input voltage will then be proportional to the ratio (n/N) of the numbers generated by both counters:

$$V_{iN} \propto (\frac{n}{N})$$
 (A1)

V/F converter LM 331 exhibits a nonlinearity of ± 2 PPM or better between 100 HZ and 6 KHZ, thus by restricting its output to that range, and by using the dual counter technique, high resolution and accuracy can be gained with low frequency V/F converters.

ACKNOWLE DGMENTS

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REFERENCES

- J. H. Sondericker, Production and Use of High Grade Silicon Diode Temperature Sensors, "Advances in Cryogenic Engineering, Vol. 27," Plenum Press, New York (1982) p. 1163.
- R. A. Pease and L. Distaso, V/F Converter and Microcontroller Produce High-resolution ADC, <u>Electronic Design</u>, September 13, 1980.
- B. Trump, VCF's take their place in A/D Conversion, Electronic Products, January 1, 1985.
- 4. W. W. Peterson and D. T. Brown, Cyclic Codes for Error Detection, Proceedings of the IRE, January 1961.