Fermi National Accelerator Laboratory

FERMILAB-Conf-92/148

# A Pipelined Multiranging Integrator and Encoder ASIC for Fast Digitization of Photomultiplier Tube Signals

R.J. Yarema, G.W. Foster, J. Hoff, M. Sarraj and T. Zimmerman

*Fermi National Accelerator Laboratory*
*P.O. Box 500, Batavia, Illinois 60510*

May 1992

To be presented at the Second Annual Conference on Electronics for Future Colliders, Chestnut Ridge, New York, May 19-21, 1992.

Operated by Universities Research Association Inc. under Contract No. DE-AC02-76CHO3000 with the United States Department of Energy

## Disclaimer

# A PIPELINED MULTIRANGING INTEGRATOR AND ENCODER ASIC FOR FAST DIGITIZATION OF PHOTOMULTIPLIER TUBE SIGNALS

R. J. Yarema, G. W. Foster, J. Hoff, M. Sarraj, T. Zimmerman

Fermi National Accelerator Laboratory
PO Box 500, Batavia, IL, 60510

Presented at

The Second Annual Conference
on Electronics for Future Colliders,
Chestnut Ridge, New York,
May 19-21, 1992

# A PIPELINED MULTIRANGING INTEGRATOR AND ENCODER ASIC FOR FAST DIGITIZATION OF PHOTOMULTIPLIER TUBE SIGNALS*

R. J. Yarema, W. Foster, J. Hoff, M. Sarraj, T. Zimmerman
Fermi National Accelerator Laboratory

**ABSTRACT**

A new full custom chip is being designed using the Orbit 2 micron "BiCMOS" process to provide a wide range fast digital readout of Photomultiplier Tubes. The goal is to obtain a digitized PMT signal with a 18-20 bit dynamic range and 8 bits of accuracy in a floating point number format every 16 ns. The chip is DC coupled to a PMT and uses a four-way gated integrator and encoder to form a 4 bit binary number which is the exponent of the floating point number. Simultaneous processing of the PMT signal on binary weighted scales provides a pipelined analog signal to a single FADC which generates the floating point number mantissa. The current state of development of this new chip and results from several test chips are presented in this paper.

## Introduction

Future collider and fixed target experiments require new approaches to detector instrumentation. One approach being worked on at Fermilab [1] is to digitize fast photomultiplier tube signals in the base of the PMT and use digital storage techniques to provide a subsequent digital delay for formation of the level 1 trigger in the experiment. The key to the project is the design of a full custom chip called the Digital Photomultiplier Chip (DPC). The purpose of the chip is to accept current pulses directly from a PMT without an intervening noisy cable and generate a digital number which represents the total charge (energy) deposited from the PMT each clock period. The chip must work over a very wide dynamic range and provide digital information every 16 ns.

Design of the chip was initiated in the Orbit 2 micron CMOS process which also has vertical NPN transistors. To use the NPNs in this chip design, a high frequency model of the transistors was developed from test structures [2]. Fabrication of the first chip design using the model was completed on two different foundry runs. There was excellent correlation between the model and the actual performance of the device. Based on the success of the first chip, the design has continued in the Orbit process.

## Principle of Operation

The DPC operates by taking a current pulse from a PMT, adding that current to a fixed bias current, and then completing four distinct steps. First, the total current is divided into 10 binary weighted current pulses (I, I/2, I/4, .... I/512) which are integrated on 10 separate capacitors as shown in Figure 1. Second, a comparator for each capacitor compares the capacitor voltage to a fixed reference and sets a latch at the output of the comparator. The fraction of comparators which are set indicates the range of the input signal. For very small PMT input signals, none of the latches are set. As the input signal

*Work supported by the U. S. Department of Energy under contract No. DE-AC02-76CHO3000.

increases, the I through I/512 latches are set sequentially. Third, the 10 comparator outputs are encoded by a 10 to 4 Gray code encoder to provide the 4 bit exponent of the

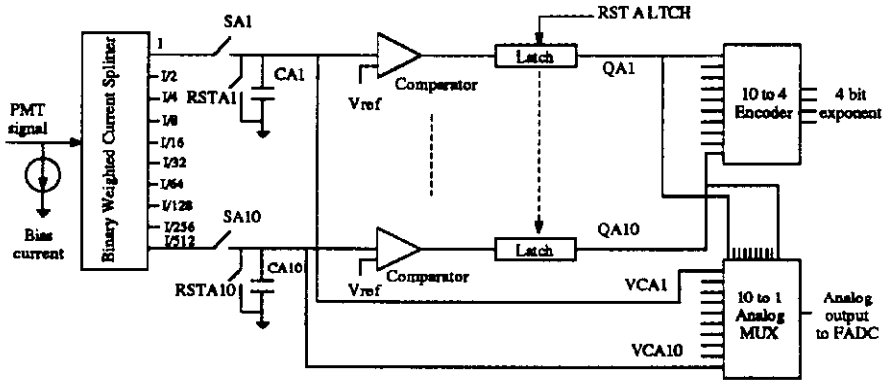


Figure 1 - Simplified DPC Block Diagram

floating point number which represents the PMT signal amplitude. At the same time, the outputs of the comparators are used to select via an analog multiplexer the appropriate capacitor voltage to be buffered for digitization by a flash ADC. Fourth, the capacitor voltage is reset and the cycle is repeated.

For the circuit shown in Figure 1 to function properly, the compare, output multiplexing, and reset would have to occur in zero time. Obviously, that is not possible. To get around this problem, the operations described are pipelined. Since there are four operations, it is natural to use a four stage pipeline. Thus instead of one capacitor bank, set of comparators, 10 to 4 encoder, and analog multiplexer, there are four of each as shown in Figure 2. In four sequential time intervals, four sets of current switches (SA, SB, SC, SD) direct the binary weighted outputs of the splitter to the A, B, C, and D capacitor banks respectively for integration. The compare and latch, output buffering and multiplexing, and capacitor reset functions are pipelined. Since there are now four time slices present in the chip at all times, additional digital and analog multiplexers are necessary as shown on the right side of Figure 2. The multiplexers deliver the correct digital and analog information to the outputs two clock ticks after it actually occurred. All of the timing signals, including the additional multiplexer signals, are generated by a signal control generator shown in the lower left side of Figure 2.

At the present time, the FADC is thought to be an 8 bit commercial device. However, consideration is being given to incorporating the FADC directly on the DPC. A 2-stage FADC is a candidate here because of the pipelined nature of the input signal.

To help understand operation of the circuit, it is useful to examine how the circuit responds with a bias current and the presence of an input signal. One of the functions of the bias current is to provide a minimum current in the splitter to keep the transistors in a reasonable operating region. The bias current, however, performs another function- namely, to insure that the analog output signal on the range of interest is always between -1 and -2 volts so that a single range FADC can be used. Figure 3 shows the encoded 4 bit exponent and the analog signal which are output from the PDC as a function of input current for a chip with 18 bits of dynamic range and 8 bits of accuracy.

The bias current is divided between the binary weighted output currents as follows: I=64ua, I/2=32ua, I/4=16ua, I/8=8ua, etc. As the input current level increases, the range of interest increases from the I range to the I/2 range up to the I/512 range. When there is no input current, the 64 ua bias current is integrated for 16 ns on a 1 pf capacitor to provide a -1 V output. Since the comparator references are set for -2 V, none of the comparators are set and the 4 bit exponent is 0000. The FADC range is set for operation from -1 to -2

V. At -1 V, the FADC output is 00000000. For convenience, the current pulse from the PMT is assumed to be a 10 ns wide rectangular pulse. A PMT pulse of 100 ua for 10 ns

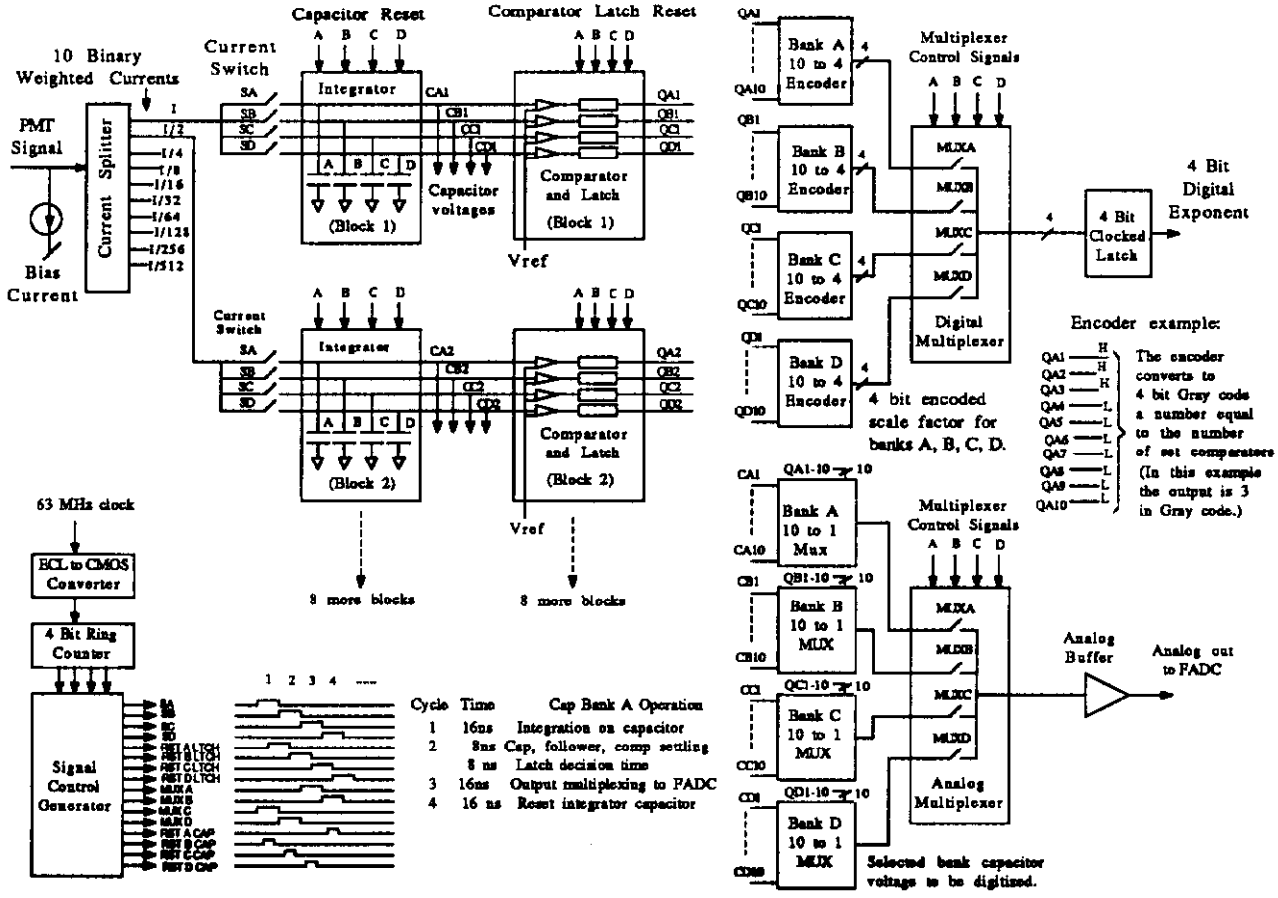


Figure 2 - Complete DPC Block Diagram

integrates -1 V on the 1 pf storage capacitor. The bias current and 100 ua pulse combine to integrate -2 V on the storage capacitor. Thus as the input current increases from 0 to 100 ua, the exponent remains fixed and the FADC output increases to 11111111. The sensitivity on the lowest scale is 400 na/bit. When the capacitor voltage on the most sensitive scale exceeds -2 V, the first comparator is set causing the 4 bit exponent to change to 0001. At the same time, the range of interest is changed to I/2. A bias current of 32 ua for 16 ns and I/2=50ua for 10 ns gives an analog voltage of -1 V at the low end of the I/2 range of interest. As the input current increases from 100 ua to 300 ua, the output of the FADC increases from 00000000 to 11111111. As the input current increases from 300 ua to a maximum of about 100 ma, the pattern of changing 4 bit exponents, ranges of interest, and FADC outputs continues as shown in Figure 3. The combination of 4 bit exponent and 8 bit FADC output combine to form a wide range floating point number which represents the magnitude of the PMT pulse.

In the actual implementation of the circuit, the FADC range is set to be slightly wider than -1 to -2 V in order to accommodate slight variations in chip processing. Thus a few bits of range from the FADC will be lost. Calibration of the chip is accomplished by varying a known DC input current and running the raw output data through a lookup table which corrects for slope, offset, and nonlinearity errors on each scale.

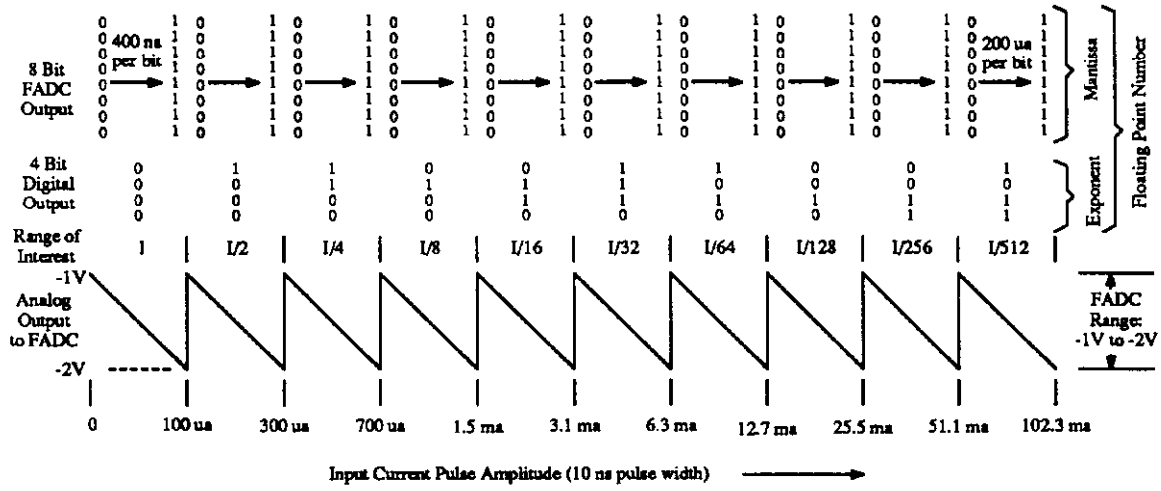


Figure 3 - Analog and Digital Outputs From the DPC for Different Input Currents

## Circuit Operation

Operation of the major blocks shown in Figure 2 are examined in the following sections.

*Current Splitter*

The most critical subcircuit in the DPC and the only one required to operate over a 20 bit dynamic range is the current splitter. The splitter is the circuit which takes the PMT current and bias current, which is set by a current mirror via an external resistor, and converts it into 10 binary weighted currents for subsequent integration on pipelined capacitor arrays. Parallel bipolar transistors with collector outputs grouped in a binary fashion are used in a common base configuration to generate nine current ranges from I/2 to I/512. The tenth current range on the present design is derived by multiplying the current in the I/2 range to form I. Thus, the total range of the splitter circuit is I to I/512. The topology used for the I/2 to I/512 ranges is three cascaded 8-transistor common base current divider sections, which have identical transistors paralleled to form three binary weighted outputs and a carry output which feeds the next 8-transistor section. (See Figure 4.) This arrangement is a compromise between the number of output ranges per section and the number of cascaded sections. All of the transistors used in the splitter section are identical devices with 8 x 8 micron emitters. (Larger components are formed by paralleling the smaller devices.)

Unfortunately, a simple common base amplifier configuration with PMT capacitance at the input has the problems of poor frequency response and high input impedance at low input currents. To improve this situation, the first divider section is included as part of a feedback amplifier. The input feedback amplifier is a current amplifier with a total closed loop gain of almost one (the common base has a slight current loss due to base current). In a simple way, it can be viewed as an eight transistor common base pass element, with a feedback circuit driving the base of the pass section to improve speed and input impedance. The required open loop gain is provided by a large NMOS (3000/2) transistor driving a polysilicon load resistor (275 ohms) which feeds the bases of the pass transistors. A MOSFET is used as the input gain element instead of a bipolar for two reasons: 1) the bipolar transistors formed in the Orbit 2 micron process have large collector

resistance which would result in small phase margin in the feedback amplifier and thus poor stability, and 2) the somewhat unpredictable base current would add to the input current, which is undesirable. In order to preserve adequate phase margin, the pole formed at the load resistor node must be kept as high as possible. Therefore, a cascode structure is used for the input transistor, and an emitter follower is used to drive the pass transistor bases.

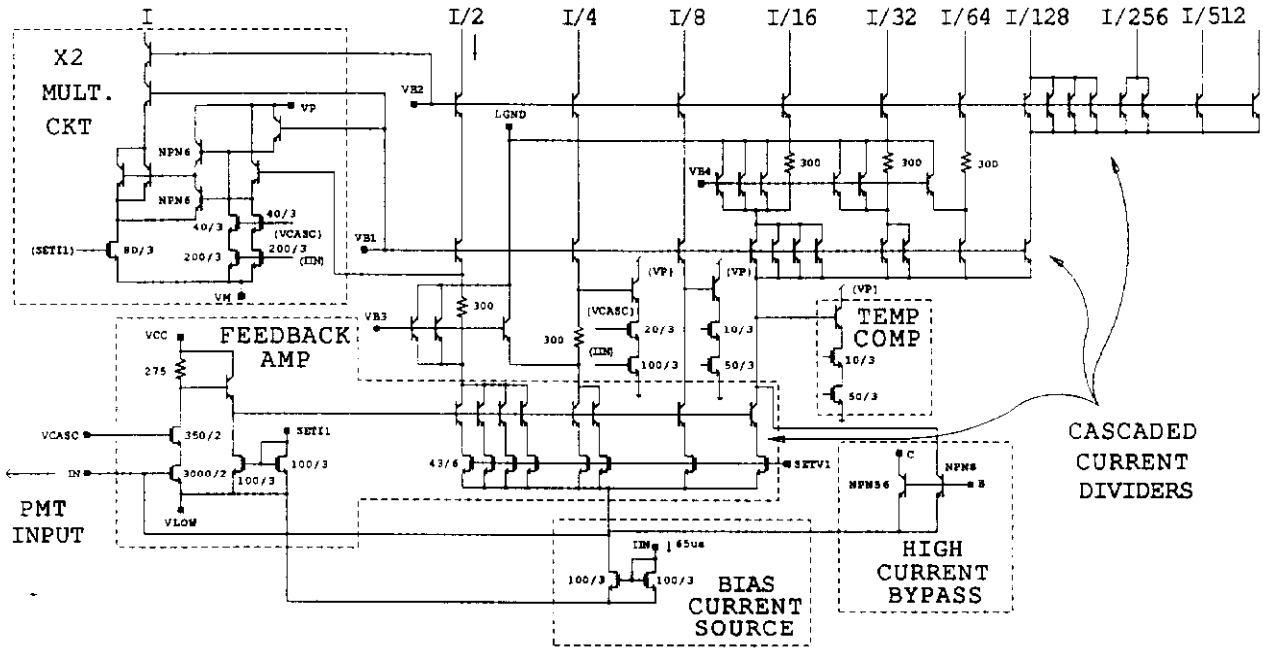


Figure 4 - Current Splitter

At large input currents (> 10 ma), however, the current carrying capacity of the pass transistors in the feedback amplifier is exceeded and problems arise. A large bipolar common base transistor is therefore added to the input, and biased in such a way that it shunts large currents around the feedback amplifier at current levels where the feedback amplifier is not required. Thus the feedback amplifier is used to derive the low current output ranges while the large bipolar is used to shunt excess current around the feedback amplifier for higher currents. The transition between high and low current operation takes place smoothly without any affect on the circuit performance.

The large NPN transistor is actually composed of 56 + 8 minimum size transistors, to allow sufficient current handling capability. The NPN base is brought to an external pin to allow the base voltage to be externally set and allow a low impedance bypass to be added to prevent excessive ringing at high currents. Normally, the base voltage is set to approximately 0.5 volts higher than the quiescent input emitter voltage. Under this condition, the large NPN conducts no significant current for PMT inputs less than 2 ma, which covers the range of interest from I to I/8, served by the feedback circuit. Typically, 1/8 of the feedback amplifier pass transistor current is fed to the subsequent ranges (I/16 to I/512) and therefore, to be consistent, only 1/8 of the large NPN transistor current is passed to the next stage. For this reason, the large NPN bypass transistor is actually divided into two parts to allow 7/8 of the shunt current to be dumped and the remaining 1/8 combined with the "carry" output of the first section of the splitter cascade.

In order to turn on the large NPN and shunt large currents, the input (emitter) voltage must go negative enough to forward bias the emitter-base junction. In other words, the input of the feedback amplifier must have enough impedance to develop a reasonable voltage drop for large input currents. A MOSFET (43/6) is placed in the emitter of each

splitter leg in the feedback amplifier to act as a variable degeneration resistor and allow adjustment of the large NPN turn on characteristics.

Currents passing through the highest current ranges (I/128 to I/512) must pass through one transistor in each of the three cascaded 8-transistor common base current divider sections. Additional pass transistors are placed in the I/2 to I/64 current ranges, so that each output passes current through an equal number of transistors. Thus the base current loss error for all ranges is equalized and the errors due to the Early effect are minimized.

The number of ranges that can be realized in a current divider depends on several things. The upper limit on the input current for 64 transistors designed with the Orbit process is about 100 ma. If a higher current design were attempted, more parallel transistors would be required and the frequency response would be degraded. Integrator capacitor size also affects the number of realizable ranges. A smaller capacitor requires a smaller current to integrate to a given voltage, thus small integrating capacitors are desirable for maximizing dynamic range (given a fixed upper current limit). However, the integrator capacitor value should be about 1 pf or larger, to limit the effect of voltage dependent parasitics. This combination of constraints on the divider design yields a maximum of nine outputs, or bits, for the Orbit process. The dynamic range can be widened , however, by adding current multipliers at the low current end. The increase in delay and risetime due to the multiplier must be minimal. The present design has a X2 amplifier driven by the I/2 output leg, extending the range to 10 bits. In theory, more multiplier stages can be added.

Current multiplication (X2) is achieved by impressing the buffered base and emitter voltages of one of the single pass transistors in the I/2 output leg of the splitter across a double transistor base-emitter junction. Twice the I/2 current will flow out the double transistor collector, since its Vbe is the same as the I/2 single transistor Vbe. In order that the loading on the I/2 output be minimal, minimum size emitter followers are used as the initial buffers. These drive larger emitter followers, which in turn drive the transistor used to set the I output current. The large emitter followers are connected in series to insure that they each carry nearly the same current, so that their base-emitter drops will be nearly identical. In this design, some multiplication error exists due mainly to the Early effect. A modified multiplier has been designed to remove most of this mismatch.

One interesting property of the multiplier circuit is that it can be used to compensate the divider outputs for drifts in the DC bias current due to the temperature dependence of transistor beta. If the pass transistor beta decreases, tending to decrease the output DC bias current, the multiplier emitter followers will draw more base current. If the multiplier is designed properly, the two effects will completely cancel. To achieve this effect on the other outputs of the first divider section, dummy emitter followers connected to current sources are added to each of the legs in the first current divider section.

*Current Switch, Integrating Capacitor Banks, and Analog MUX*

Each splitter output (I to I/512) feeds a four way current switch (SA, SB, SC, SD) which steers the current to a block of four pipelined capacitors as shown in Figure 2. The current switches are made up of emitter coupled bipolar transistors driven at the bases by ECL-like levels which are derived from a four stage ring counter. The current switch collectors distribute the current in pipeline fashion to the integrators. Each integrator circuit consists of a poly-poly capacitor (0.75 pf), an NPN emitter follower buffer, an NMOS clamp (100/2), and an NMOS reset switch (30/2) as shown in Figure 5. The buffer is necessary to drive the comparator and analog multiplexer. A bipolar follower is preferred over a MOS follower because of its speed, and its ability to achieve a voltage gain of nearly one. Also, the bipolar buffer presents a nonlinear capacitance which is used to very nearly cancel the nonlinear capacitance of the current switch collector. The base current of the bipolar causes a slope on the capacitor voltage that results in a small constant offset voltage to the FADC.

The clamp transistor exists to prevent any current switch transistor from saturating due to a large current pulse. An NMOS is used for the clamp since the parasitic capacitance it presents is much less voltage dependent than that of a bipolar. Finally, the reset switches (RSTA, RSTB, RSTC, RSTD) are simply NMOS transistors connected across the

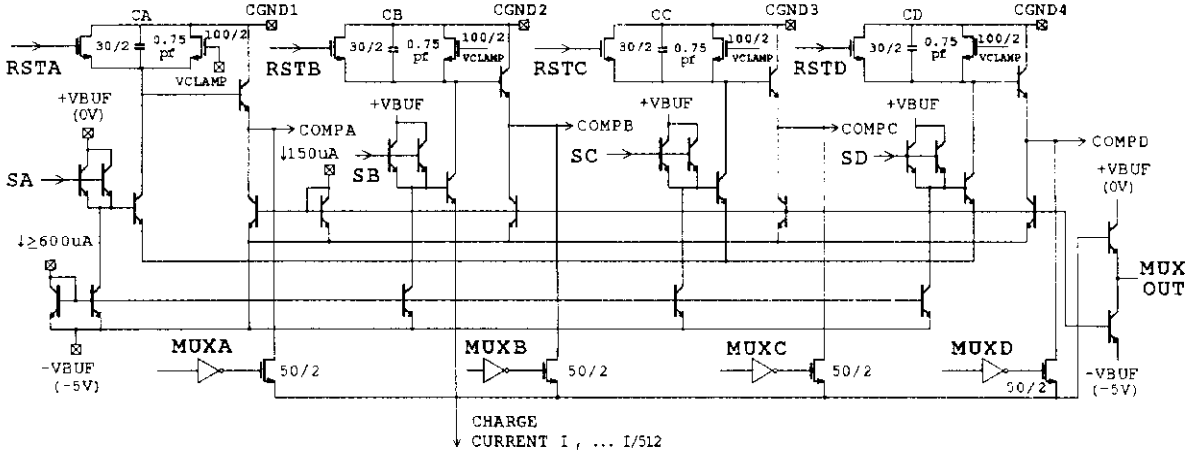


Figure 5 - Current Switch, Capacitor Block, Analog Multiplixer

integrating capacitors. The switch is sized to to assure that the largest possible capacitor voltage can be reset to 1 mv accuracy within 10 ns. An NMOS is much preferred over a PMOS due to its inherent lower resistance for a given geometry, and much less voltage dependent parasitic capacitance (due to a highly back biased source-substrate junction).

At the bottom of Figure 5, the analog MUX switches (MUXA, MUXB, MUXC, MUXD) which are used to route the capacitor voltage to the FADC are shown. All of the circuitry shown in Figure 5 is repeated ten times, once for each of the current ranges.

*Comparator and Comparator Latch*

Each block of buffered capacitor outputs from the integrators is fed to a block of high speed, low power comparators and latches as shown in Figure 2. The comparator and latch schematic which is shown in Figure 6 is similar to the circuit described by G. M. Yin [3]. The circuit has a differential input stage followed by a latch stage which has three parts: 1) a high speed regenerative latch with a reset, 2) a level converter stage, and 3) an output buffer. During a typical cycle, the regenerative latch is being held reset at a point

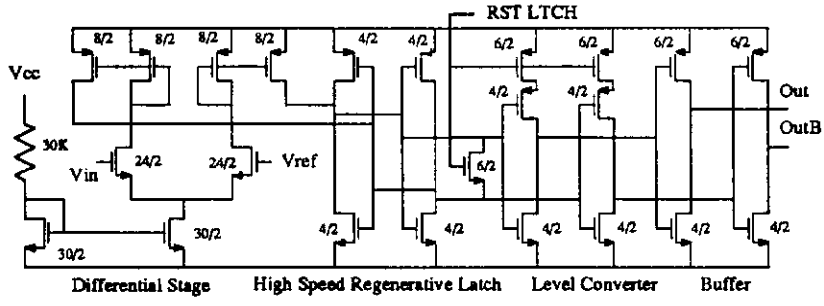


Figure 6 - High Speed Comparator

midway between the two rails while charge is being accumulated on an integration capacitor. Meanwhile, the level converter generates a logic low to be transmitted through

the buffer to the encoding logic. When the differential stage output is to be sampled, the latch reset is released and the high speed regenerative latch drives the level converter to the appropriate high or low condition. Simulation results show a worst case reset and compare time of 5-6 ns in response to a couple of millivolts of differential input voltage. Once the regenerative latch has responded to the integrated capacitor voltage, the encoders generate the appropriate digital code and the latched outputs are used to select the appropriate capacitor voltage for digitization.

The layout of the differential latch is symmetric to avoid loading mismatches at the output of each stage. Also, minimum size transistors have been used to to reduce parasitic capacitances at the output. Offsets in the differential stage are not a significant problem since the comparators merely control where a change in range of interest occurs. A slightly wider FADC range easily compensates for this effect. The circuitry in Figure 6 is repeated forty times (once for each integrator) on the final chip.

*Encoder and Digital Multiplexer*

One output from each of the 10 comparator blocks shown in Figure 2 is routed to one of four encoders. One encoder is designated for each of the four capacitor banks (A, B, C, D) which are pipelined to sample 4 sequential time intervals. The encoders take ten comparator signals and produce a 4 bit Gray code number which represents the number of comparators which has been set as shown in the example on the right side of Figure 2. The four bit encoder outputs pass through a digital multiplexer and a clocked latch to output the encoded exponent from the DPC.

## Chip Test Results

To test performance, four different test chips have been designed. The first chip had the I/2 to I/512 current divider. The second chip incorporated a X2 multiplier scale along with the current divider to give a binary weighted 10 way current splitter. The third added a four way current switch on the I/2 scale, an analog multiplexer to output the

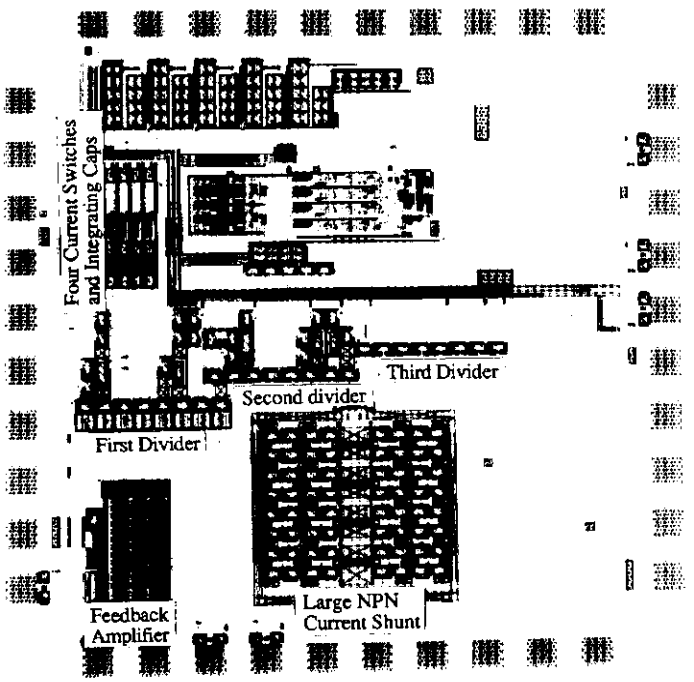


Figure 7 - Current Splitter Layout

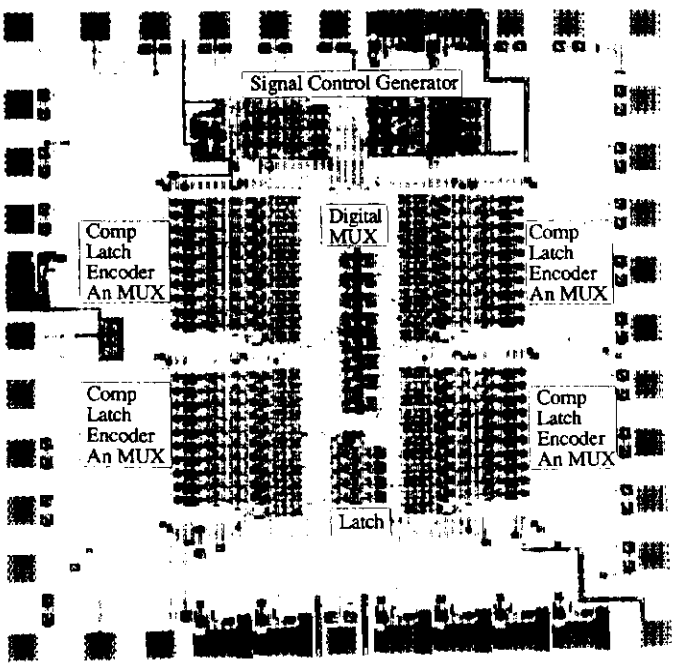


Figure 8 - Encoder/Multiplexer Layout

integrator voltages for digitization by a FADC, and an ECL to CMOS clock converter with a 4-bit ring counter to operate the 4 way current switch. The fourth chip had all the comparators, latches, encoders, multiplexers, and a signal control generator for a complete device. The first three chips have been fabricated, tested and found to be fully functional. The fourth chip is in fabrication. Figure 7 shows the layout of the third chip and Figure 8 shows the layout of the fourth chip. In principle, these two layouts are merged to form a complete device approximately 3 mm by 3 mm in size.

Tests on the first chip showed that 1) the I/2 to I/512 current division was very accurate, 2) the divider had low sensitivity to temperature variations, and 3) that the divider had the necessary fast transient response. Also, the feedback amplifier used on the lower output current ranges and the high current bypass worked very well with no crossover problems. The accuracy of the current division was checked by injecting a well known current into the divider circuit. Ratios of the individual measured output currents to the total measured output current matched the predicted ratios with less than a 1% error in all cases, indicating good bipolar matching. The total of the output currents from all the ranges was 96% of the input current. (The 4% current loss is due to base current loss in each of the cascaded dividers.) This implies a transistor beta of 118, since the current travels through essentially four common base transistors (three transistors in the current divider and one in the current switch).

In order to check the transient response of the divider, a current injector was built with a fast discrete transistor capable of supplying 0-90 ma with rise and fall times of about 3 ns. Figure 9 shows the current divider output on the lowest current range (I/2) and on the highest range (I/512). On the lowest range all of the current is being handled by the

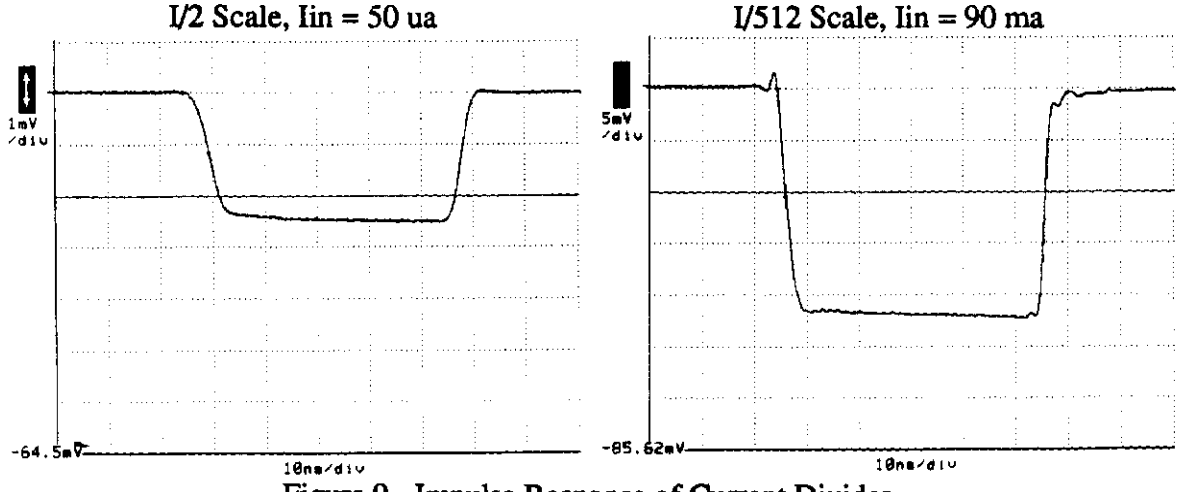

Figure 9 - Impulse Response of Current Divider

feedback loop and on the highest range almost all the current is being handled by the high current shunt. In both cases, the response is excellent. (The slope on the bottom of the pulse response is due to the current injector circuit, not the current divider).) The output signal delay was found to vary from 2 to 4 ns across the ranges from I/2 to I/512. Results from the second chip confirmed that the spread in divider current delay is only about 2 ns for the ranges from I/2 to I/512. Minimization of the spread in delay is important because the current switches of all the scales are driven from a common clock.

The multiplier circuit, used to generate the I scale from the I/2 scale, was evaluated on the second chip. The I scale was found to closely reproduce twice the current on the I/2 scale. There was however an additional 1 ns of delay, and the gain of the multiplier stage varied by 2% resulting in a slightly nonlinear response. A modified multiplier design has been designed and simulated with SPICE, and is predicted to have linearity better than 0.5%. An additional property of the modified design is that the delay of the multiplier

output is about the same as that of the I/2 output, thus keeping the total output delay spread of the complete splitter to about 2 ns.

The splitter circuit has excellent temperature stability. Tests show that for a constant externally supplied DC input current, no measurable change in the divided output current occurs over a 35 °C temperature range. If the integrator is operated using the on-chip input DC source, a 1% shift in final voltage is observed over 35°C. About half the shift is due to variation in input current which is caused by the Vt shift in the curent mirror. This effect can be be reduced if necessary.

A test of the linearity of the DPC was performed by applying an accurately measured variable DC input current and measuring the the integrator final value on the I/2 scale. Good linearity is desired from -1 to -2 volts (the region where the FADC must work). Figure 10 shows the deviation in millivolts from a perfectly straight line for the I/2 integrator capacitor output voltage to the FADC. The error is very small, less than 1 mv peak to peak. This implies that a complete lookup correction table is not needed for errors generated within the DPC and that a simple slope and offset correction is all that is needed for calibration.

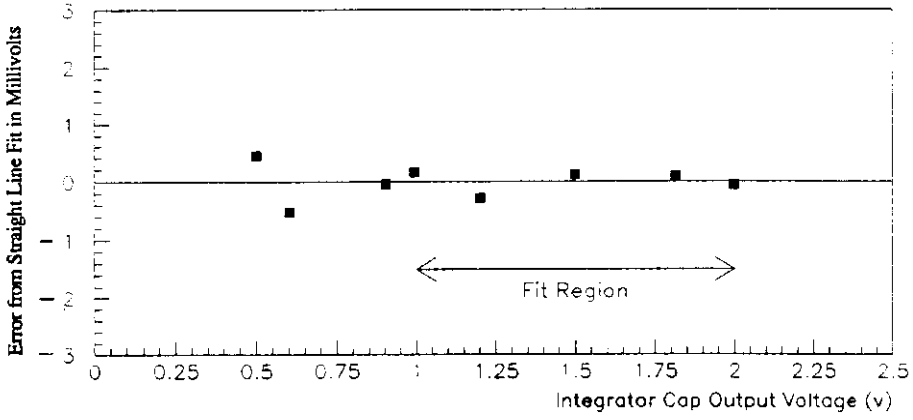


Figure 10 - Linearity Error in Millivolts on the I/2 scale

Noise seen on the integrated capacitor voltage is primarily determined by the collector current shot noise in the common base pass transistors and gate jitter on the most sensitive current scale. For outputs I/2 to I/512, over a wide range of currents, the output noise was always less than 1 mv rms. Noise at the multiplier output was slightly higher at 1.5 mv rms due to additional noise sources in the multiplier circuit. In the test setup, the gate rms pulse jitter was less than 10 ps.

Crosstalk between the 4 capacitors on a given current range was found to be relatively small. A large 100 ma pulse was injected into one capacitor while observing the effect on a small capacitor voltage on the I/2 range. Two effects were observed: 1) a small coupled voltage step and 2) damped ringing. The 4 mv step was caused by a shared ground connection and will be removed in all future designs. The ringing which is proportional to the magnitude of the input current, appears to be caused by substrate coupling to a large NPN buffer used to drive a pad for measurement purposes.

Capacitor matching between the four capacitors on the I/2 range was checked on the third chip. A maximum gain error of 0.5% was found between the four capacitors. The error, however, was systematic and is expected to be improved in future designs.

## Summary

Several test chips have been fabricated to demonstrate the feasibility of digitizing PMT signals at high speeds over a very wide dynamic range. Test results on all the chips

have been positive and no inherent problems with the technique have been uncovered. A complete pipelined 18 bit range DPC is expected to be fabricated soon. Work on expanding the range to 20 bits is continuing.

**Acknowledgements**

The authors would like to thank Cathy Neuman-Holmes for her early design and simulation work on the current divider circuit. Also we would like to thank Bill Williams and Al Dyer at Fermilab for their wirebonding and circuit board construction assistance which made testing the various chips possible. And finally we would like to thank Issy Kipnis at LBL and Rick Van Berg at the University of Pennsylvania for providing bipolar test structures for the Orbit process which allowed us to develop our bipolar model.

**References**

[1] G. W. Foster, et. al., "Baseline Implementation of the Digital Phototube Readout System for the SDC Calorimeter," Fermi National Accelerator Laboratory, September 3, 1991.

[2] T. Zimmerman, "An Approximate HSPICE Model for Orbit Low Noise Analog Bipolar NPN Transistors," Fermilab TM-1748, July 1991.

[3] G. Yin, et.al., "A High Speed CMOS Comparator With 8-bit Resolution," IEEE Journal of Solid State Circuits, Vol. 27, No. 2, February 1992, pp. 208-211.