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DP-944

AEC RESEARCH AND DEVELOPMENT REPORT

DESCRIPTION OF A TEMPERATURE MONITOR FOR LARGE REACTORS

PART III, PERFORMANCE

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Printed in USA. Price $2.00
Available from the Clearinghouse for Federal Scientific and Technical Information, National Bureau of Standards, U. S. Department of Commerce, Springfield, Virginia

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Instruments
(TID-4500, 37th Ed.)

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by

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January 1965

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CONTRACT AT(07-2)-1 WITH THE
UNITED STATES ATOMIC ENERGY COMMISSION

ABSTRACT

A prototype temperature monitor has been tested successfully. The monitor can scan large numbers of thermocouples, at the rate of 24,960 per second, to gain and process information on the temperatures of coolant streams in a nuclear reactor. The monitor incorporates extensive digital logic to provide read-outs and temperature alarms plus self-normalization and self-checking capabilities. The present study was primarily concerned with the performance of the analog and scanning systems. Two different input commutators were used with the prototype, one consisting of 104 pairs of single pole relays and the other of 104 transistor switches. Reliability has been excellent; there were no electronic failures in about 500 days of operation and only 10 relay failures after 6×10^8 contact closures, for each relay. Accuracy of the signals was better than ±0.25% of full scale readings.

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DESCRIPTION OF A TEMPERATURE MONITOR FOR LARGE REACTORS

PART III, PERFORMANCE

INTRODUCTION

Two earlier reports in this series, DP-834 and DP-836, described the design philosophy and prototype construction of a coolant-temperature monitor for a large nuclear reactor. The prototype monitor consists of coupled analog and digital systems, as shown in Figure 1. Signals from the thermocouples measuring the coolant stream temperatures are scanned at high speed by a commutator-multiplexer system and are then converted to digital readings. These digital outputs pass through a series of digital logic circuits which provide a visual data display and a series of alarm functions for abnormal temperature conditions. A magnetic drum is used to supply the timing pulses for the system and to provide the necessary memory capacity for the logical operations. The system is self-normalizing, and incorporates extensive self-checking features to detect malfunctions. The prototype monitor has been in operation in the laboratory since May 1, 1963. This report presents the results of accuracy and reliability tests that have been made since that time.

SUMMARY

Tests of the digital system were restricted to a demonstration that the system logic will accomplish its design purpose. Tests of the analog system were much more comprehensive; in part because this system determines the over-all accuracy of the monitor and in part because one of the purposes of building the prototype monitor was to investigate different types of commutator circuitry. Two different types of commutators were used in the prototype: one based on relays as the low-level switches and the other based on transistors. A special program for an IBM-704 computer assisted in the reduction of data from the analog system. Tests were made for accuracy (noise and linearity), for rejection of a common-mode AC signal superimposed on the individual thermocouple systems, for signal resolution, for the effects of crosstalk and temperature changes, and for long-term stability. Results are given in the following table. Both commutators performed very satisfactorily, but the relay commutator gave somewhat better performance in the accuracy tests. In the long-term stability tests covering some 500 days of continuous operation, there was only one failure with the solid state commutator (due to an initially defective transistor).

Ten relays out of a total of 208 failed in the relay commutator. The higher reliability of the transistor system has led to the specification of solid-state commutators for the reference monitor design.

	Relay Commutator	Solid-State Commutator
Noise in system output		
Best channel	±0.08% full scale	±0.10% full scale
Worst channel	±0.15% full scale	±0.22% full scale
Linearity	Within ±0.07% full scale	Within ±0.07% full scale
Common-mode rejection ratio	10^7:1 at 60 cps	10^7:1 at 60 cps
Resolution (nominal)	0.05% full scale	0.05% full scale
Crosstalk	0.03% full scale	0.03% full scale
Temperature coefficient	0.01% full scale/°C	Better than 0.015%(a) full scale/°C
Long-term stability	Better than 0.05% full scale/month	Better than 0.15% full scale/month

(a) Using selected components.

DISCUSSION

System Components

A block diagram of the prototype monitor is shown in Figure 1. A more detailed diagram and a functional description, are given in a preceding report in this series, DP-836.

In determining the accuracy of the system, major emphasis was placed on the analog portion. The digital portion of the system produces only "second order" errors such as "round off" errors in division, which can be made as small as desired by increasing the size of the registers in the arithmetic unit. The system performance is therefore defined as the performance of the analog portion, from the system inputs to the output of the analog to digital converter.

Some of the system specifications are:

Sampling rate	10 samples/input-sec
No. of inputs	2496
Word length	40 microseconds
Full scale input voltage	7.73 millivolts
Resolution	1/2047 full scale

A diagram of the analog system is shown in Figure 2. The prototype system is identical to the "full scale system" except that the prototype has two commutators instead of 24.

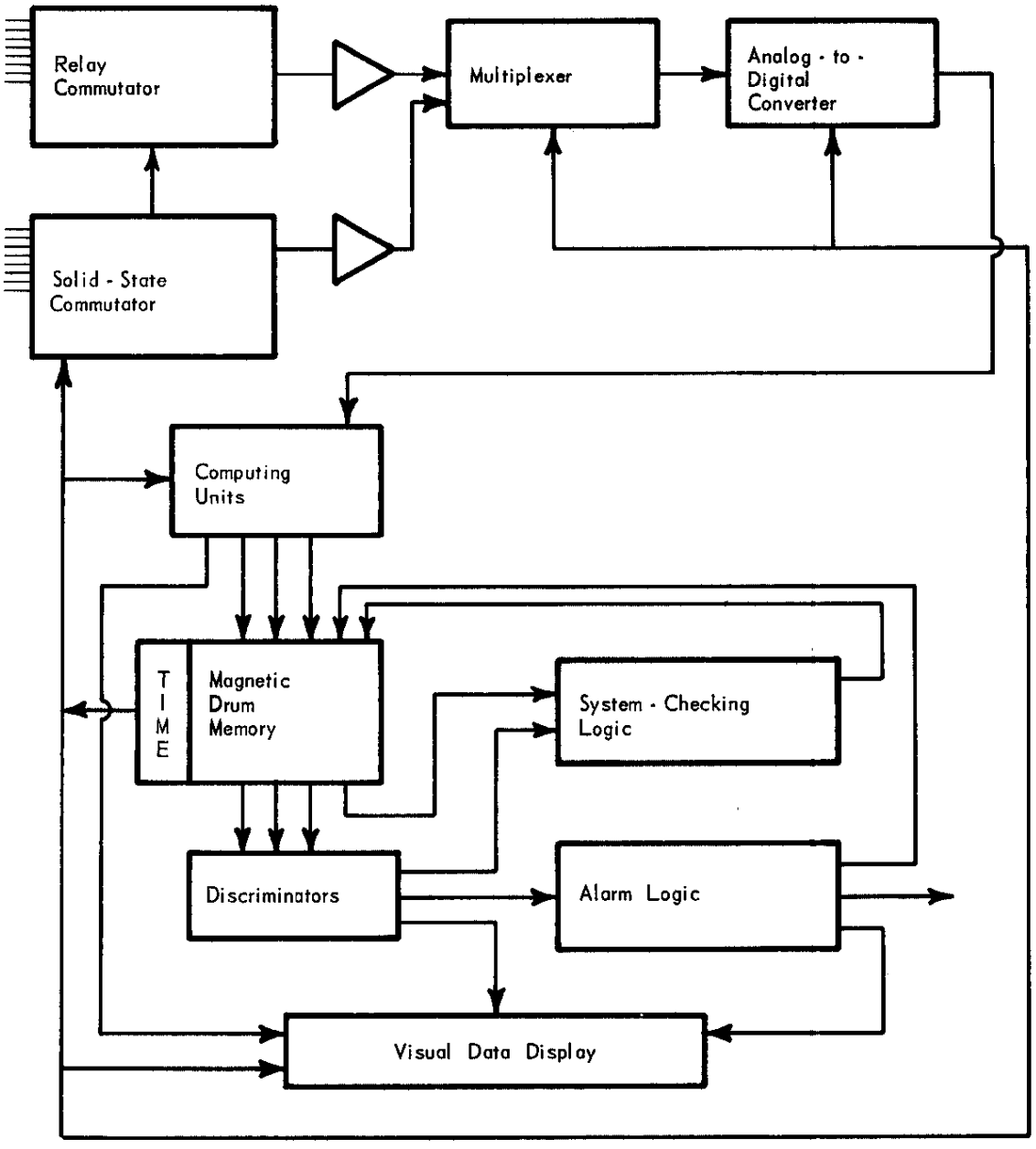

FIG. 1 SIMPLIFIED BLOCK DIAGRAM OF PROTOTYPE MONITOR

In discussing pertinent features of the analog system, it is convenient to consider the functional parts and to discuss these individually. Using Figure 2 as a reference, we will trace the signal path starting at the signal source.

The system was designed to operate from grounded thermocouples via long connecting cables. The worst condition expected for the signal source is shown in Figure 3. The unbalanced resistance is due to the unequal resistance of the wires making up the thermocouple, while the capacitance is the result of the long multiconductor connecting cable.

INPUT FILTER

In order to limit the noise in the input signal, a filter is used in each of the inputs to the system. These filters are 2-section RC filters which respond to a step input, as shown in Figure 4. This response time was selected to be significantly less than the 0.5-second response time of the thermocouple and to be commensurate with the sampling rate of the system.

SIGNAL COMMUTATION

The 2496 input capacity of a full scale system is achieved by multiplexing the output signals from 24 commutators, each of which has 104 individual two wire inputs. In the prototype system two different low-level switching schemes were tested, thus two commutators were required. To make the prototype represent the final system as closely as possible, regardless of the low-level switch chosen, the differences in timing and addressing the switches were resolved within the commutators themselves. Thus, from an external electrical point of view, the two commutators are identical.

RELAY COMMUTATOR

Figure 5 shows the basic makeup of the relay commutator; 104 pairs of single pole relays (Bristol Synchroverter* C 1445-50) are used, split into two banks of 52 pairs each. The two banks are sampled alternately by transistor switches that are identical to the ones used in the solid state commutator; the switches are discussed in that section. This "hybrid" scheme was adopted to ease the requirements on the pickup and dropout times of the relays. The sampling rate in each commutator is 1040 per second, which would normally allow only 0.961 millisecond for the operation of each relay. If the contact closures of two relays were to overlap, a serious error could result from the

*Registered trademark of Bristol Co., Aircraft Equipment Division, Waterbury, Conn.

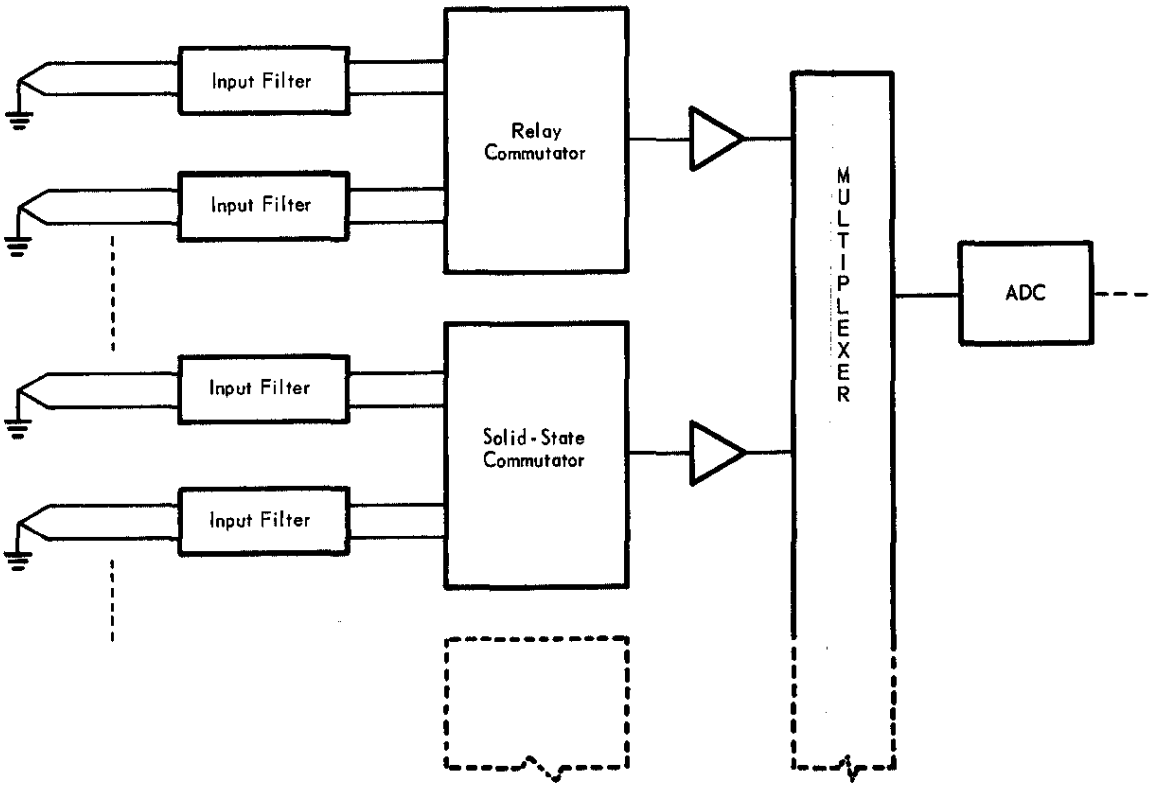

FIG. 2 BLOCK DIAGRAM OF ANALOG SYSTEM

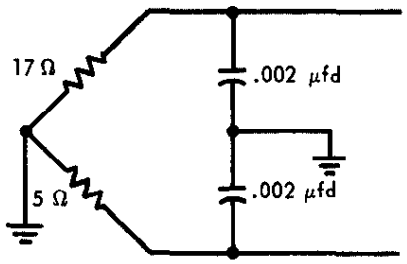

FIG. 3 THERMOCOUPLE EQUIVALENT CIRCUIT FOR WORST CONDITIONS

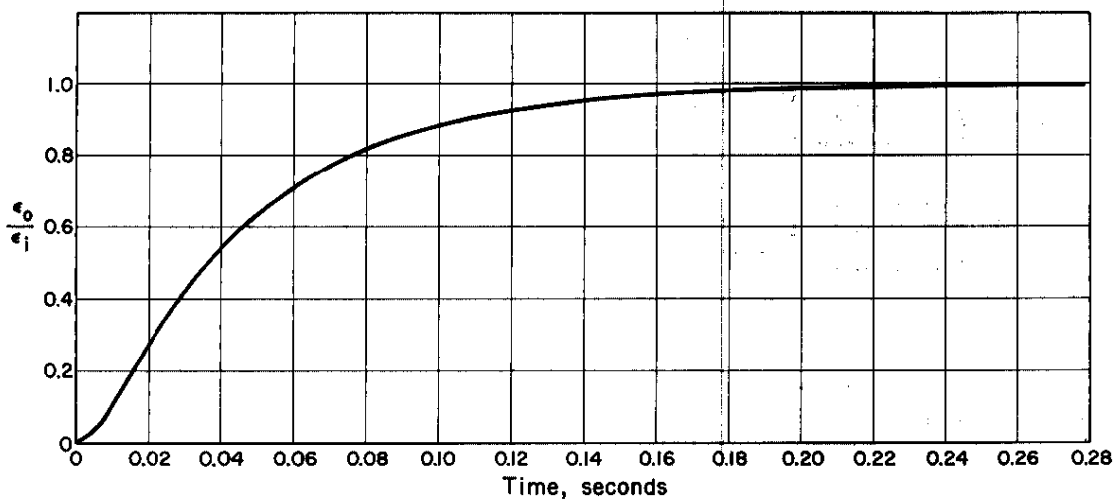

FIG. 4 RESPONSE OF INPUT FILTER TO AN INPUT STEP

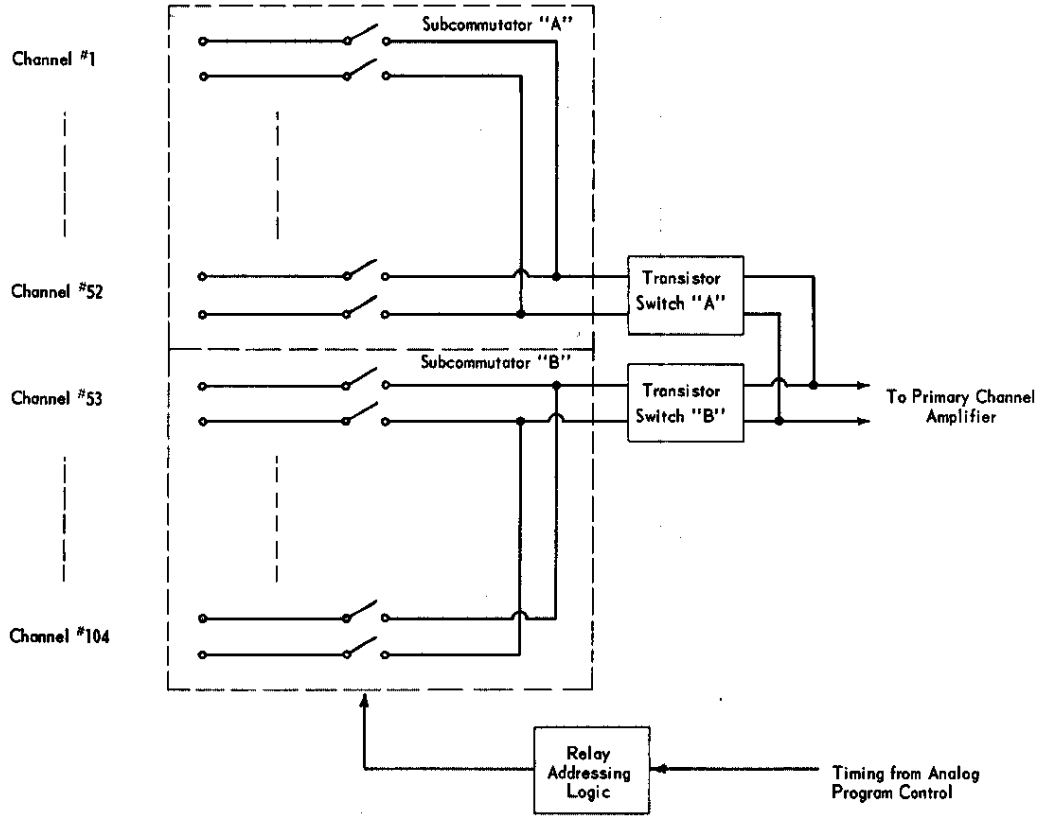

FIG. 5 RELAY COMMUTATOR BASIC LAYOUT

equalization of voltage between the two associated input filters. By using the "hybrid" arrangement the allowed time for operation is doubled, which provides a large margin of safety against overlap. In addition, the common mode current due to the parallel capacitances of the "open" relays is reduced by a factor of two.

Because one purpose of the prototype testing was to determine the type of relay and transistor switches best suited for this particular service, it may seem inconsistent that both types were used in the same commutator. This was done because of the advantages cited above, and with the knowledge that if the transistor switch stability proved to be inadequate, the data from the relay commutator could be corrected by using one input in each subcommutator to introduce a reference signal. The deviations of the reference signal from its initial value would be added to or subtracted from the other 51 inputs in a subcommutator to produce data free of the variations caused by the transistor switch. However, because adequate stability was evidenced by the transistor switch, this alternative was not required.

The relays receive their drive pulses from an 8 x 13 matrix. The rows and columns of the matrix are driven from transistor circuits that act as a "limited current" source, thus producing the high rate of acceleration necessary for short pickup times but limiting the total force applied to the armature to a value consistent with the lowest over-all noise generation.

The transistor switches sample only the final part of the relay contact closure (defined as the 80 μsec immediately preceding the cut-off of drive current to the relay coil). Figure 6 shows the time relation of these various drive pulses in the commutator.

SOLID-STATE COMMUTATOR

The transistor switches in the solid-state commutator are arranged in 8 groups of 13 switches each, as shown in Figure 7. This arrangement was used to limit the size of the leakage current from the "off" switches. An interesting feature of the commutator is the use of a coupling transformer in each input signal path. The transformer, while requiring the use of one additional transistor switch per input, enabled a high common mode rejection to be obtained through the use of electrostatic shields on the primary and secondary windings. In addition, a voltage gain of 2 was taken in the transformer, reducing the noise specification on the input stage of the low-level amplifier.

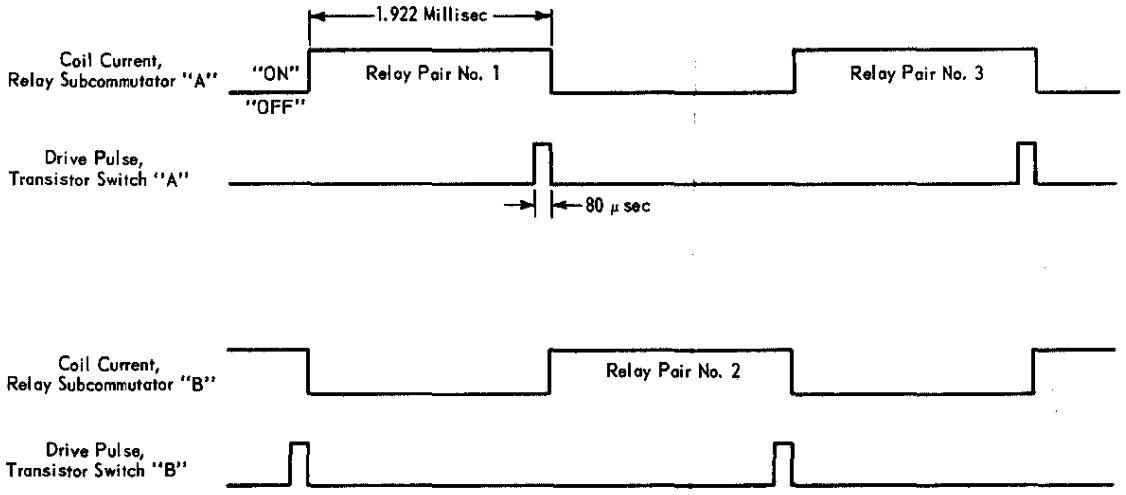

FIG. 6 TIMING OF RELAY COMMUTATOR

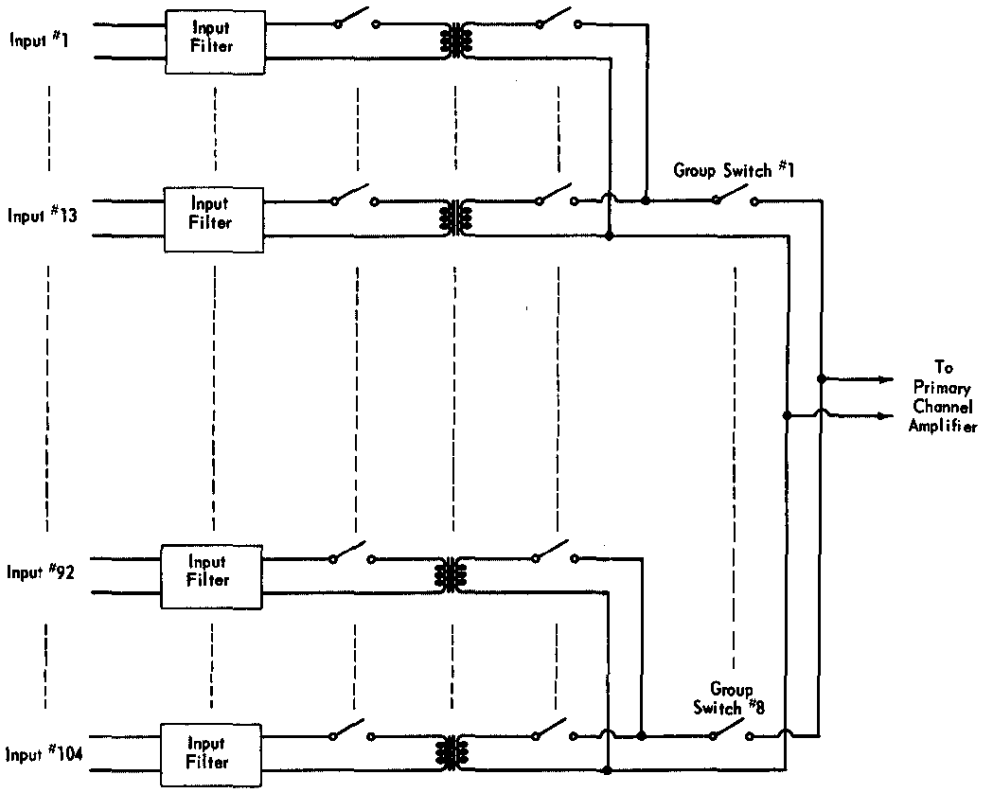

FIG. 7 SOLID-STATE COMMUTATOR SUBCOMMUTATION ARRANGEMENT

The basic element in the solid-state commutator is the transistor switch. The type of switch used in this system consists of two transistors in the "inverted" connection. The merits of this connection have been discussed by R. L. Bright[1]. The characteristics of the switch are shown in the following table.

"On" resistance	$<30\ \Omega$
"Off" resistance	$>3 \times 10^7\ \Omega$
Voltage offset	adjustable to zero μv
Leakage current	$<10^{-9}$ ampere

The switch (shown in Figure 8) generates its own "off" bias by means of CRI and C_1. During the "on" portion of the cycle, C_1 charges to the value of the voltage across CRI (0.5 volt); when the drive pulse ceases, both CRI and the collector-base junctions of Q_1 and Q_2 are reverse biased by this voltage. Because the leakage currents are very small and the time between drive pulses is only 0.1 second, the reverse bias voltage thus produced is essentially constant. Voltage offset, produced by differences in the two transistors, can be reduced to a negligible value through the adjustment of R_2. Q_1 and Q_2 are 2N1429 transistors selected for low leakage and matched for V_{ce} versus i_{bc} to within 300 μv.

Resistors R_4 and R_6 are twice the value of R_5 to minimize transient switching "spikes". This is more easily seen in the simplified circuit in Figure 9, where the stray capacitances Cs_1 and Cs_2 associated with the drive transformer have been included. By forming a bridge circuit with the stray capacitances and the current limiting resistors, the switching transients are reduced by a factor of approximately 10.

The drive transformer receives an 80 μsec pulse from a single transistor operating as a saturated switch. Drive currents in the two analog switching transistors are approximately 1 ma.

The over-all noise and common mode rejection of a system are greatly dependent on the way in which the shielding and grounding are handled. Figure 10 shows the shielding connections and ground isolation of one input in the solid state commutator. Because the system was designed to operate from unshielded input cables, the internal wiring was arranged so that the input wire with the lowest impedance to ground shielded the other wire. The group switches (refer to Figure 7) are identical with the secondary low-level switch; both

[1] Bright, R. L., "Junction Transistors Used as Switches." Trans. AIEE, Vol. 74, (Commun. and Electronics, No. 17) p. 111 (March 1955).

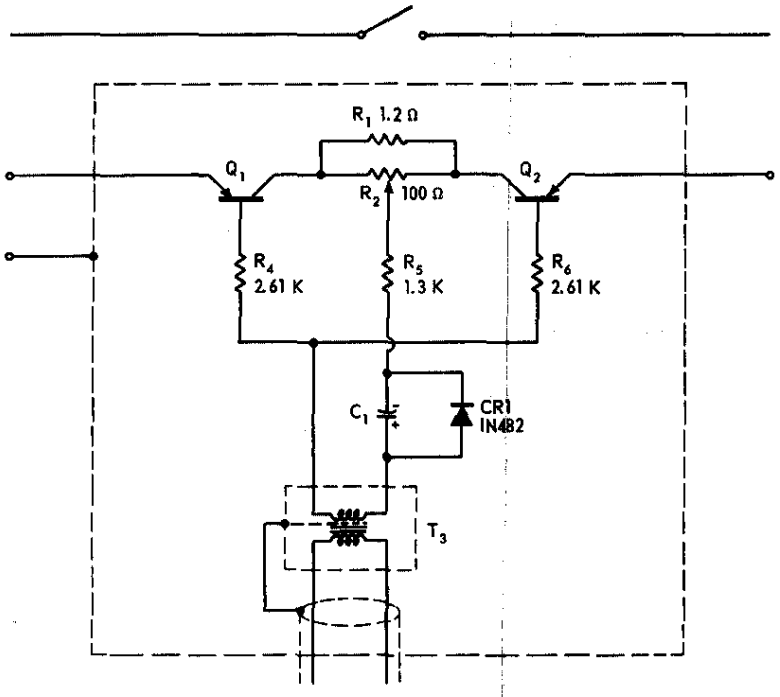

FIG. 8 SCHEMATIC DIAGRAM OF TRANSISTOR SWITCH

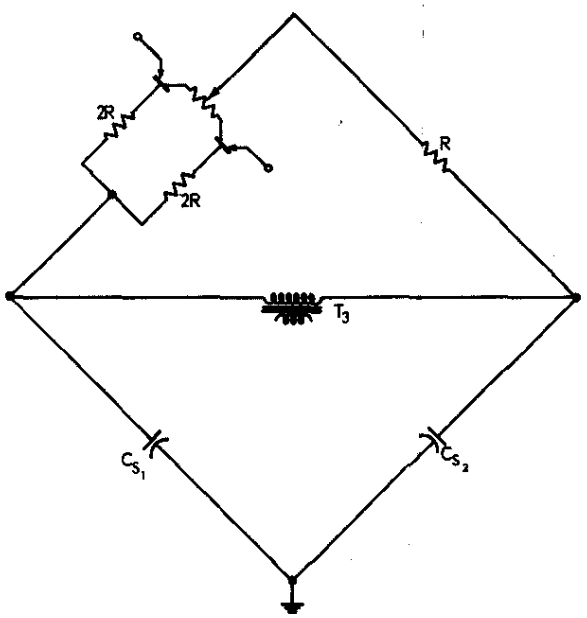

FIG. 9 SIMPLIFIED CIRCUIT FOR TRANSISTOR SWITCH

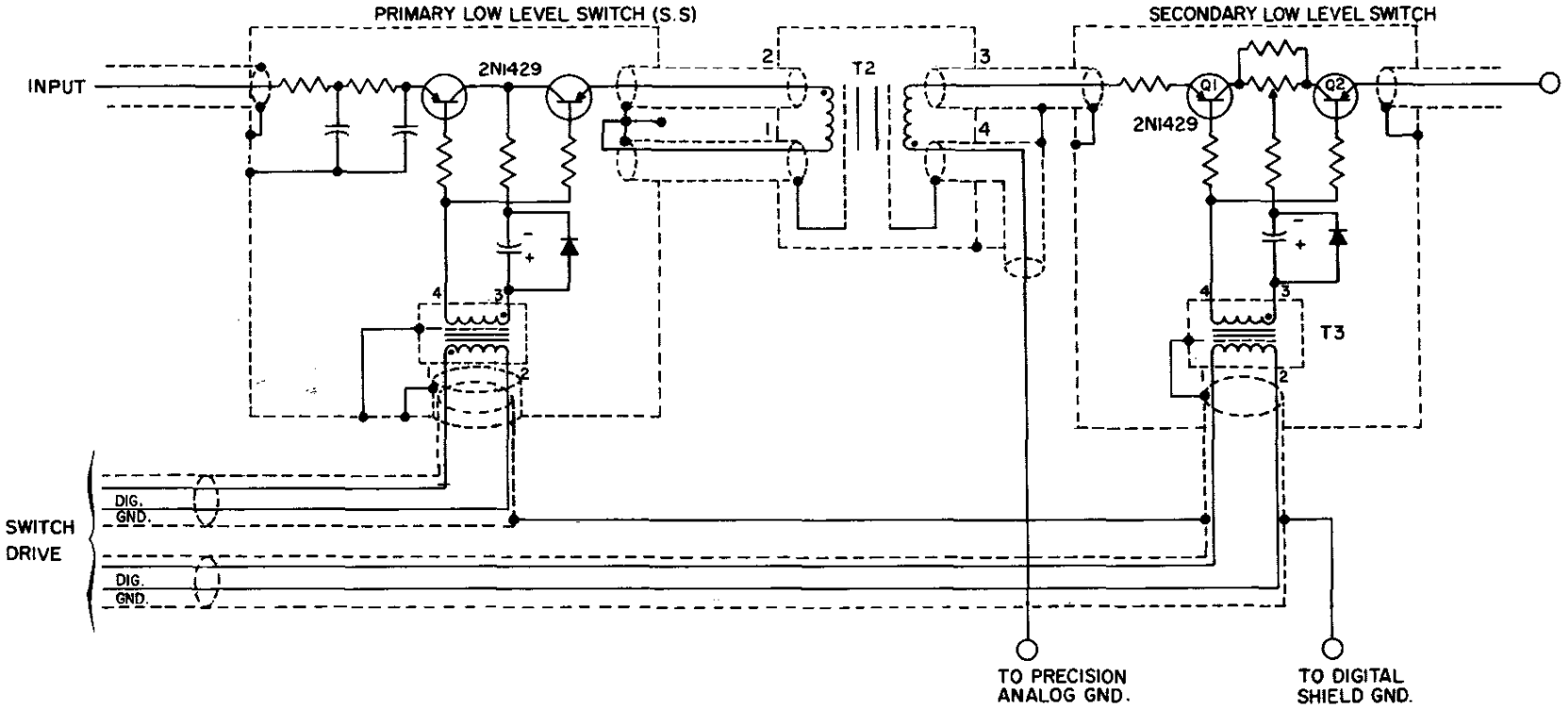

FIG. 10 SOLID-STATE COMMUTATOR GROUNDING AND SHIELDING IN INPUT CHANNEL

types have an "offset" adjustment that the primary low-level switch does not have. The "offset" of the secondary low-level switch is adjusted to compensate for both itself and the primary low-level switch, and the group switches are adjusted so that the offsets of the groups are equal, and as close to zero microvolts as possible. Addressing of the 104 inputs in the commutator is accomplished through the use of an 8 x 13 matrix in a manner similar to that employed for the relay commutator except that, as noted earlier, the final drive pulses to the transistor switches are only of 80 microseconds duration.

PRIMARY CHANNEL AMPLIFIER

Although shown separately in Figure 2, the primary channel amplifiers, one for each commutator, are physically built into the commutators. These amplifiers have a voltage gain of 500, adjustable ±5%, and have a -3 db bandwidth of approximately 50 kc. They are dc-coupled internally, but, in order to circumvent the serious long-term stability problems inherent in a direct-coupled system, a capacitor is used to couple the output of each amplifier to the multiplexer. To provide a "virtual" direct coupling, the amplifiers are dc restored. This is done by connecting restoration switches, as shown in Figure 11. These are transistor switches very similar to the ones used in the solid state commutator, except that the high level dc-restore switch uses germanium fused-junction transistors to obtain the very low "on" resistance necessary to discharge the output coupling capacitor. The dc-restore switches are driven with one phase of a 12.4 kc square wave. The other phase (180°) of this square wave is used to provide the drive pulses for the transistor switches in the commutator, thus ensuring proper synchronization between these switches (i.e., commutator switch is "on" when dc-restore switch is "off").

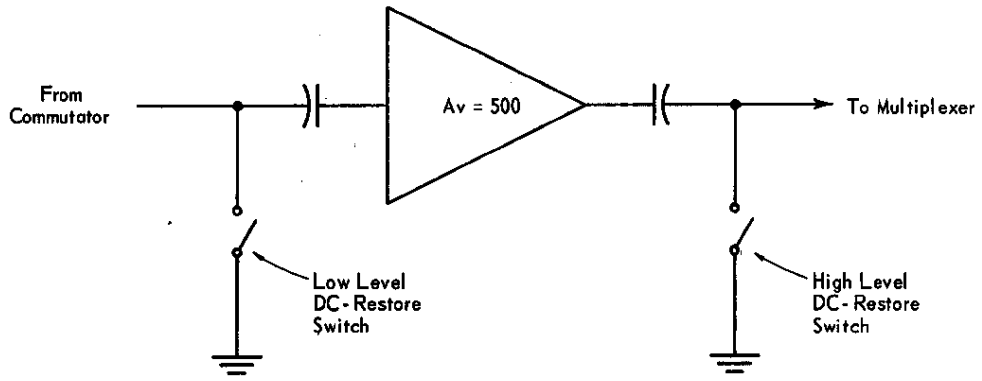

FIG. 11 COMMUTATOR PRIMARY CHANNEL AMPLIFIER

The use of a dc-restored amplifier places primary reliance for the long-term stability on the low-level dc-restore switch. It is believed that this is a better solution than to use a straight dc amplifier even if it should be necessary to provide a temperature controlled environment for the switch (for our conditions this has not been necessary).

MULTIPLEXER

Each primary channel amplifier feeds its output signals to a high-level switch in the multiplexer. In the multiplexer the signals from each of the 24 commutators are interleaved and connected sequentially onto a single line. Although the signals from the commutators and primary channel amplifiers are 80 μsec wide, the scanning rate of the system (≈25 kc) permits a word length of only ≈40 μsec. The multiplexer switches are so synchronized with the rest of the system that they close only during the last 40 μsec of the signal period. Thus the first 40 μsec may be regarded as a "settling" period during which all of the switching transients are allowed to die out. The multiplexer switches are also of the same general type used in the solid state commutator, except that the B_{veb} ratings of the transistors are higher owing to the fact that the signal is now in the 5-volt range.

ANALOG-TO-DIGITAL CONVERTER (ADC)

The ADC is a successive approximation type in which the input signal is digitized to an 11-bit binary number. The decision time is 2.78 μsec per bit so that only 30.6 μsec out of the total of 40 are needed for the conversion. The output of the ADC is the interface between the analog and digital parts of the system. All of the system performance data given in the succeeding section of this report were obtained at this point.

Data Gathering

A large amount of data was required to characterize the performance of the system. Each of the 208 inputs had to be treated separately, and a number of data points were obtained for each input under each of the various test conditions. In general, the data were taken in the form of histograms.

Two methods were used for obtaining the histograms. In the first method, the output of the ADC was recorded on magnetic tape and was subsequently reduced to usable form on an IBM-704 computer. Each reel of tape (≈2400') contained approximately 2200 data points for each of the 208 inputs. The computer program sorted these data and arranged them in the form of 208 histograms, printed out as a row of numbers showing the number of times each possible bit combination in a 64-bit range was digitized. Because the "turn-around" time for this method of data taking was approximately 1 day, it was not always convenient to use, especially when an attempt was being made to set up appropriate experimental conditions. For certain measurements, therefore, a second method was used. In this method, a specially constructed set of glow-tube scalers enabled counting the number of digitizations of each bit combination in a 14-bit range. Data from the ADC were gated to the scalers for only a single selected input so that only one histogram could be obtained at a time. Since the scanning rate of the system is 10 points/input-second, data were accumulated in the scalers at the rate of 600 points/minute.

System Performance

The system performance can be adequately described by these six parameters: (1) accuracy (noise in output), (2) linearity, (3) common mode rejection, (4) resolution, (5) crosstalk, and (6) stability (temperature - time). Each of these parameters was measured using the data-gathering methods described previously.

ACCURACY

Internally generated noise will be the principal source of error for a single reading under normal system conditions. The noise output of the prototype system was measured by connecting the inputs to simulated thermocouple sources. Each simulated thermocouple was wired according to the circuit in Figure 3. With a constant input potential the system output was recorded and finally reduced to the form of histograms. Figures 12 and 13 show such histograms for typical channels in the relay and solid-state commutators, respectively. Because the full range of the system is 7.731 mv, and the range of the ADC is 2047 bits, each bit is equal to 3.777 μv, referred to the input of the system.

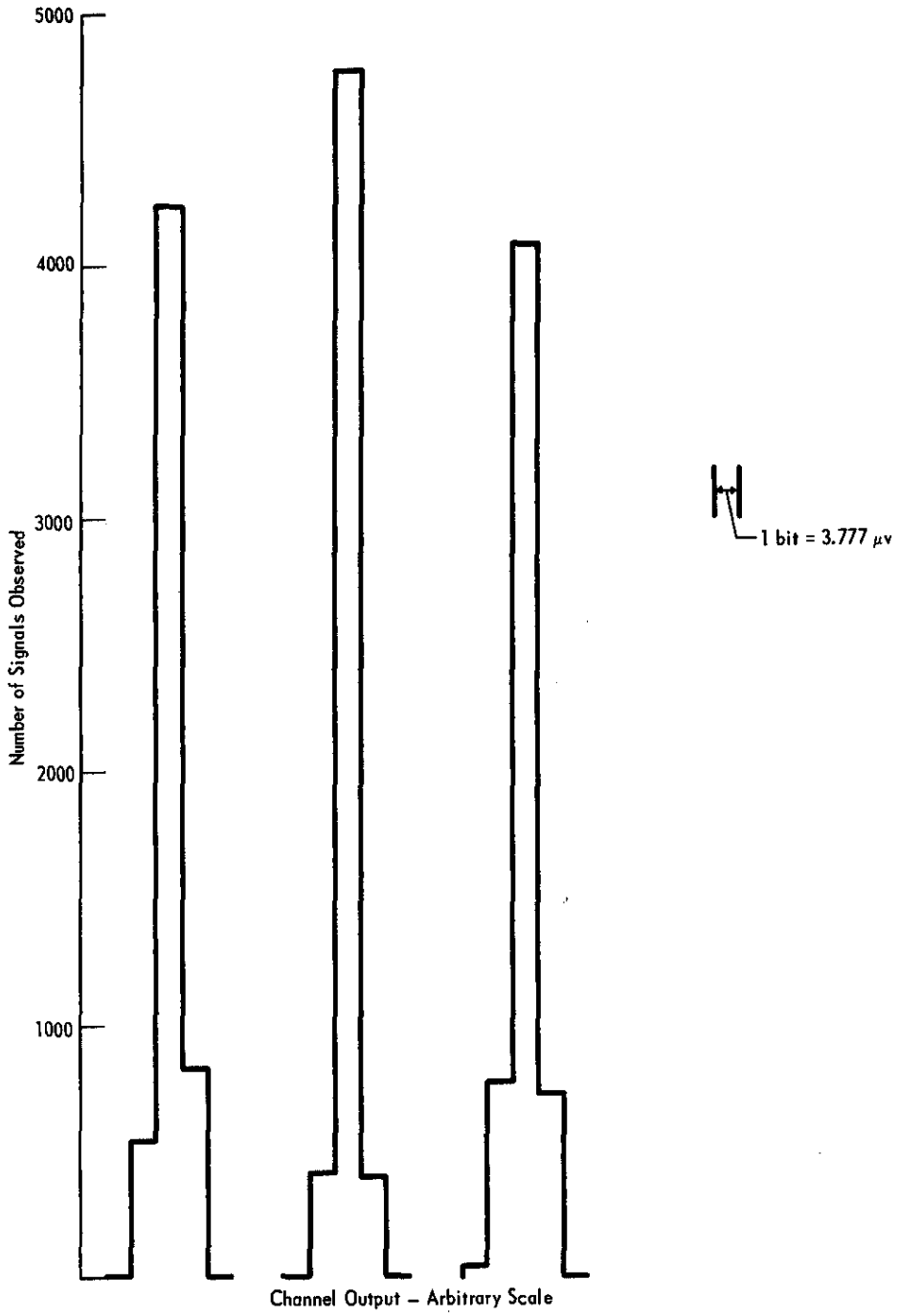

FIG. 12 OUTPUT FOR THREE TYPICAL CHANNELS IN RELAY COMMUTATOR
(Each histogram contains 5620 observations for a constant input signal)

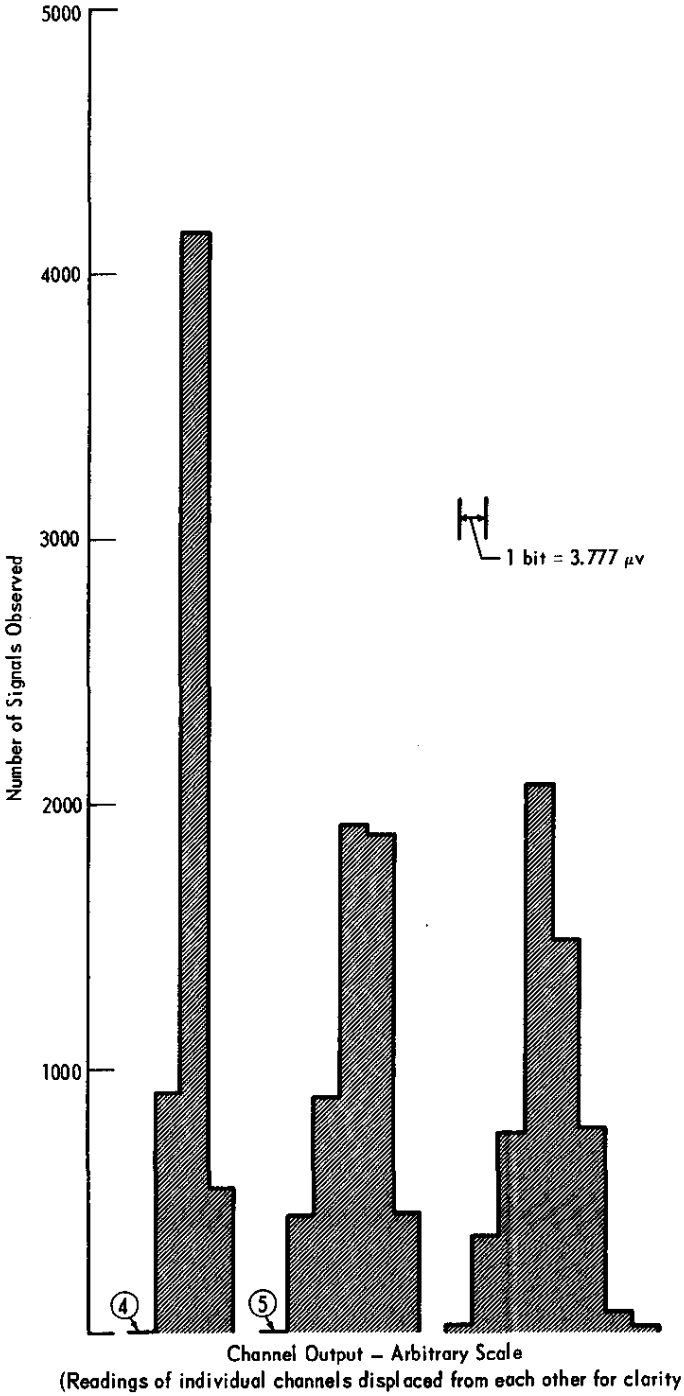

FIG. 13 OUTPUT FOR THREE TYPICAL CHANNELS IN SOLID-STATE COMMUTATOR
(Each histogram contains 5620 observations for a constant input signal)

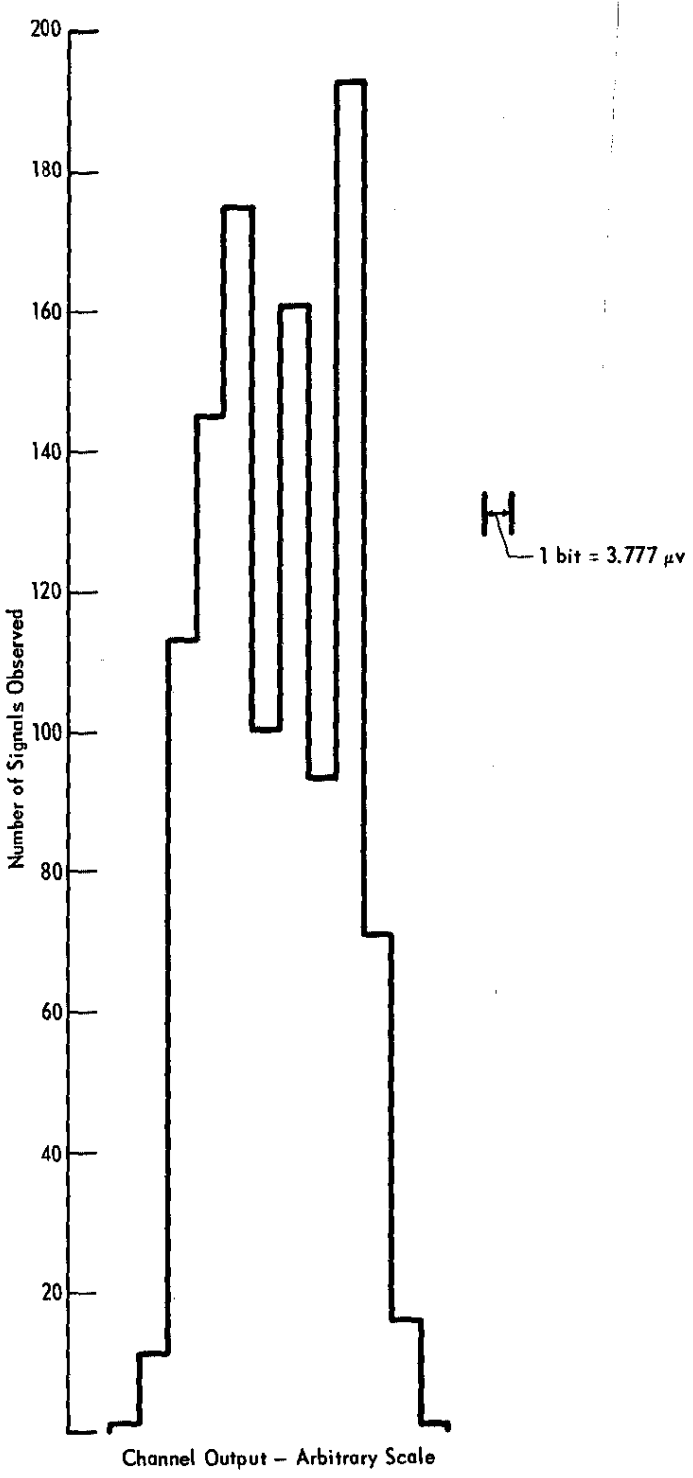

FIG. 14 HISTOGRAM OF OUTPUT FOR A CHANNEL CONTAINING COHERENT NOISE

In taking these data, a problem arose with certain channels in the solid-state commutator. A histogram for one of these channels is shown in Figure 14. The type of distribution shown is typical of a signal having "coherent" as well as random components. The coherent noise appeared as the result of the physical construction of the solid-state commutator, in which a film of paint was used as insulation between the analog and chassis grounds. In those channels where the paint film had been damaged enough to permit contact across it, the output signal contained coherent noise. There were 14 such channels in the commutator and, because the method of construction used would have necessitated disassembly of the entire commutator in order to correct these "ground loops", the data from these channels were discarded.

By determining the total width, in bits, of each of the histograms for the individual channels in a commutator, new histograms can be formed. These new histograms show the number of channels having histograms of width n, as a function of n. These "peak-width" histograms for the solid state and relay commutators are shown in Figures 15 and 16, respectively. A comparison between the figures shows that the relay commutator channels are more uniform and have, in general, a lower noise level than the channels in the solid-state commutator. However, the maximum error in the worst channel of the solid-state commutator is only ±4.5 bits or ±17 μv, from the input of the system to the output of the ADC. By itself this is a very acceptable performance. It does not, of course, include the effects of common mode voltages, temperature, or aging, which are considered along with linearity in the following sections.

LINEARITY

The linearity of the system was measured by taking 2200 observations of the output of each channel for each of 6 accurately known voltage inputs. From these data, several typical channels in each commutator were selected, and the median of each of the histograms was calculated. Using the values for the lowest and highest input voltages as the 0 and 100% points, respectively, the deviation of the remaining points from a straight line was plotted. Some of these results are shown in Figure 17. These measurements show a deviation no greater than that expected from the ADC alone (±1.5 bits).

COMMON MODE REJECTION

To test the common mode rejection of the system the commutators were connected to thermocouple simulators via 100-foot long multiconductor cables. Each input was connected to a separate set of resistors

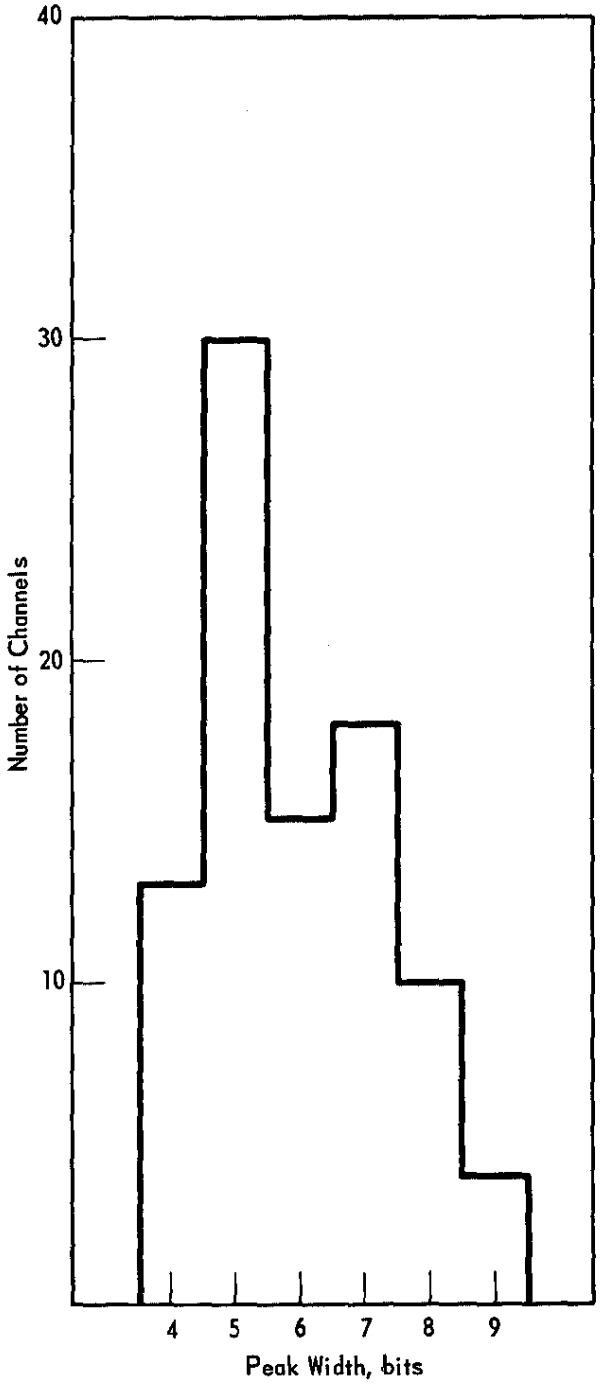

FIG. 15 PEAK WIDTH HISTOGRAM FOR THE SOLID-STATE COMMUTATOR

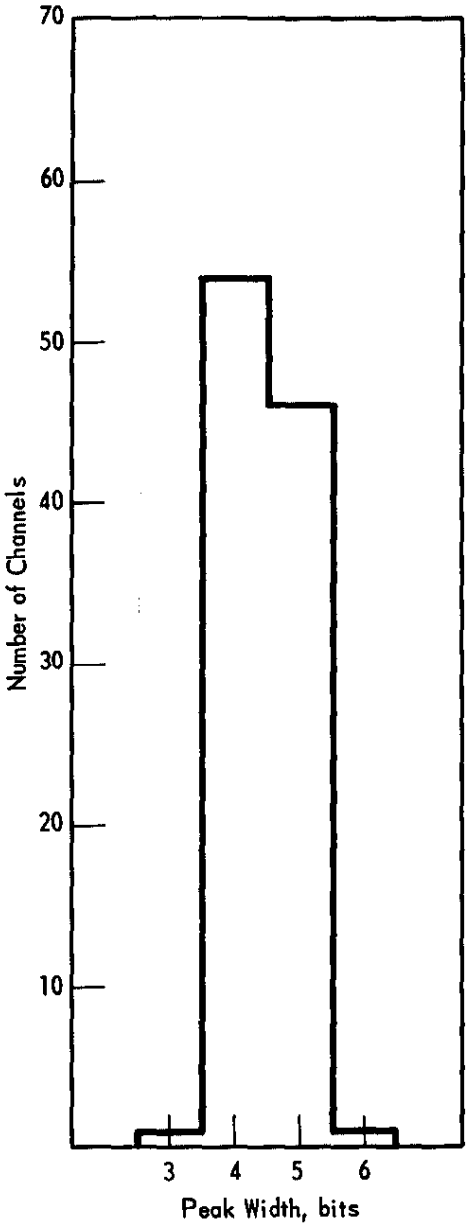

FIG. 16 PEAK WIDTH HISTOGRAM FOR THE RELAY COMMUTATOR

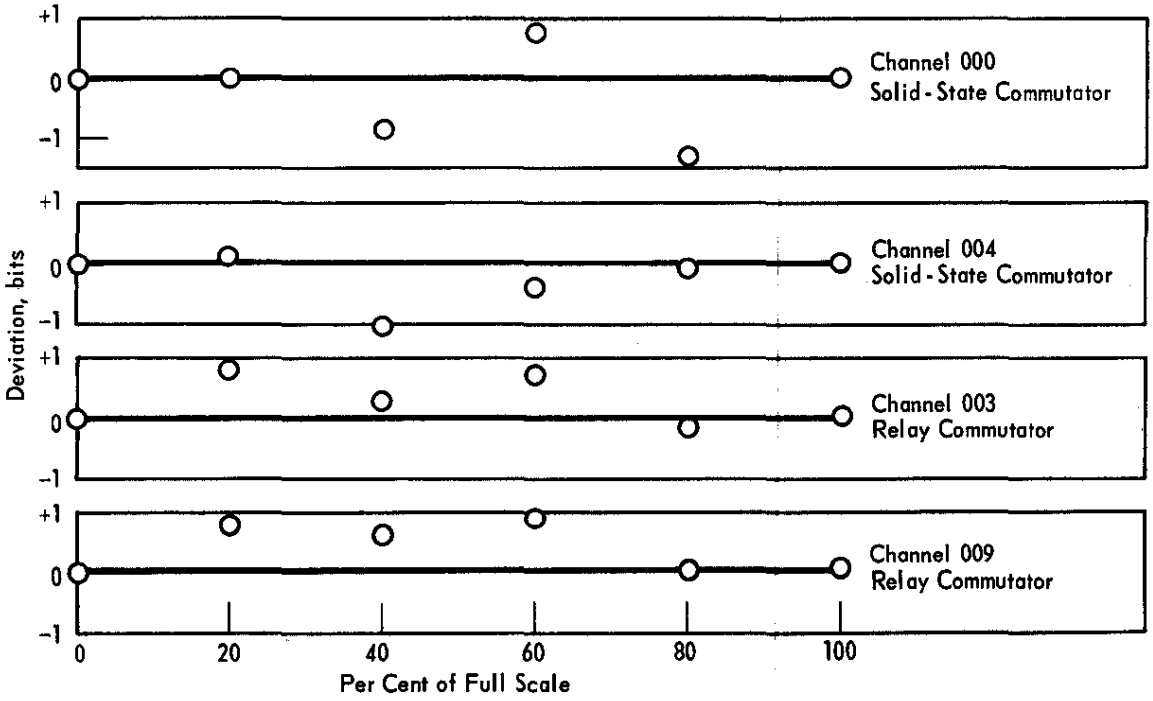

FIG. 17 DEVIATION FROM LINEARITY IN SOLID-STATE AND RELAY COMMUTATORS

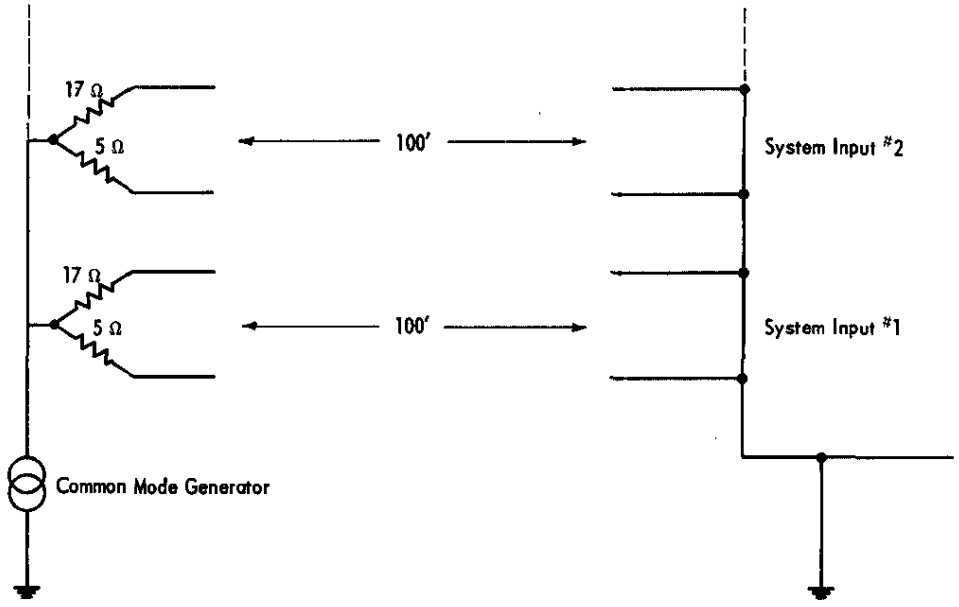

FIG. 18 INPUT CONFIGURATION FOR COMMON MODE REJECTION MEASUREMENTS

simulating the characteristics of an actual installation. Figure 18 shows the experimental setup. Sine waves from an audio oscillator were used to generate the common mode voltage. In all measurements the output of the oscillator was 12 volts RMS (33.84 volts peak to peak). Measurements were made at 0, 60, 120, 300, and 480 cps. Figures 19 and 20 show the effect of common mode signals on typical channels in the solid state and relay commutators, respectively. Since the common mode signal is converted to a differential mode signal by unbalanced capacitive reactance in the system, the effect is proportional to frequency. At 480 cps the data for the solid state commutator show two well developed maxima, one on each side of the original maxima for no common mode signal. A reasonable estimate of the amount of alternating differential mode signal can be obtained by subtracting the total histogram width at 0 cps from the total histogram width of the frequency in question. This difference, converted to volts, will be close to the peak-to-peak value of the alternating differential mode signal. When this is done for the solid state commutator, the common mode rejection ratio is 1.5×10^6 (123.5 db) at 480 cps. This extrapolates to a value of 1.2×10^7 (141.6 db) at 60 cps, which agrees reasonably well with the measured ratio of 8.9×10^6 at 60 cps. The data for the relay commutator, shown in Figure 20, reveal a distortion (asymmetry about the midpoint) of the histograms at the higher frequencies. This is indicative of poor differential linearity in the ADC. Because this distortion was not in evidence for the solid-state commutator, it must be supposed that this is an additional effect of the common mode signal in the relay commutator. To estimate the common mode rejection ratio, we took the width of the 480-cps histogram to be twice the half-width measured from the middle to the extreme upper end. This produced a common mode rejection ratio for the relay commutator that was the same as that obtained for the solid-state commutator.

Under the measurement conditions normally encountered, a realistic common mode signal would be about 1 volt, or less, and primarily 60 cps, thus the common mode rejection ratios measured for this system are high enough that errors from this cause will be completely negligible.

RESOLUTION

The nominal resolution of the system is 1 bit, or 3.777 μv. To measure the system resolution, the input voltage was raised one bit at a time and histograms were taken at each step. Some typical results from this test, shown in the following table, show an average resolution of 1 bit, as expected, with small differences due to the differential linearity of the ADC.

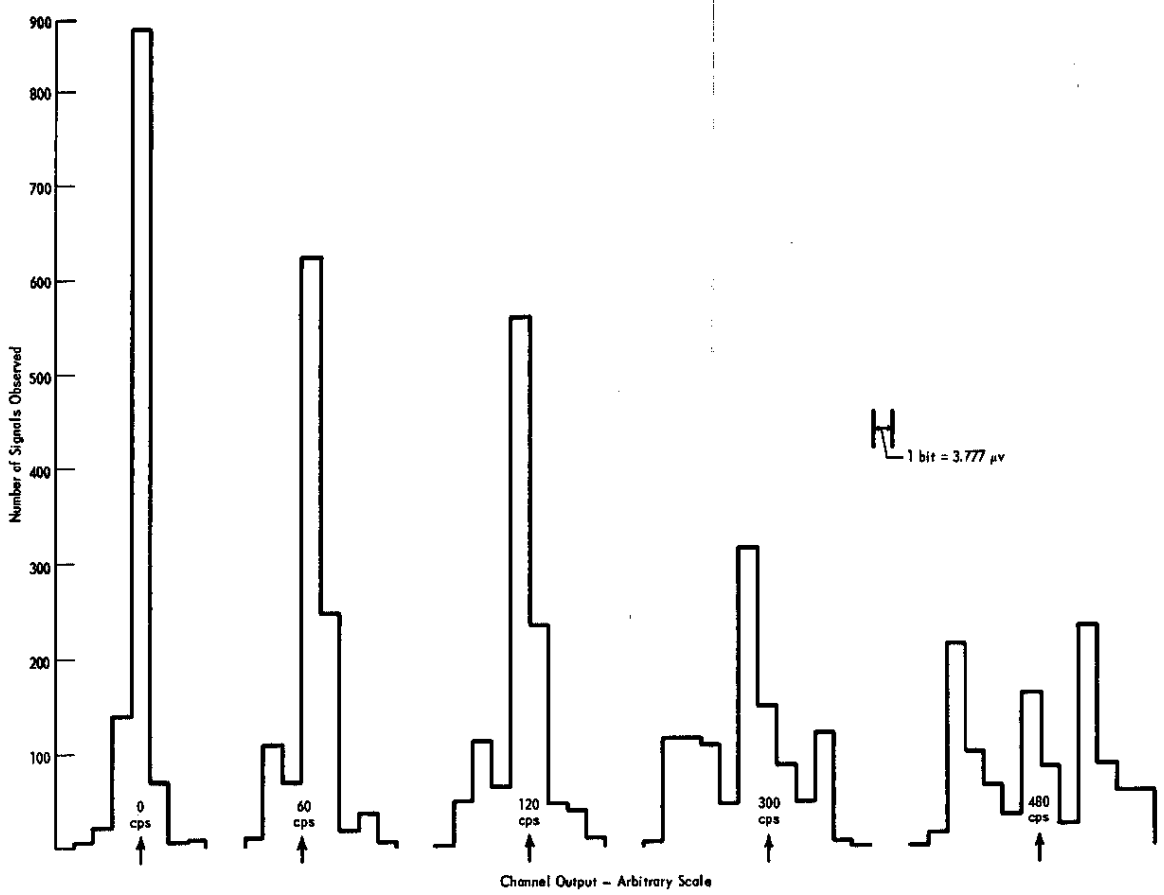

FIG. 19 EFFECT OF COMMON MODE SIGNALS AT DIFFERENT FREQUENCIES IN SOLID-STATE COMMUTATOR

(Arrow points to same bit position in each distribution)

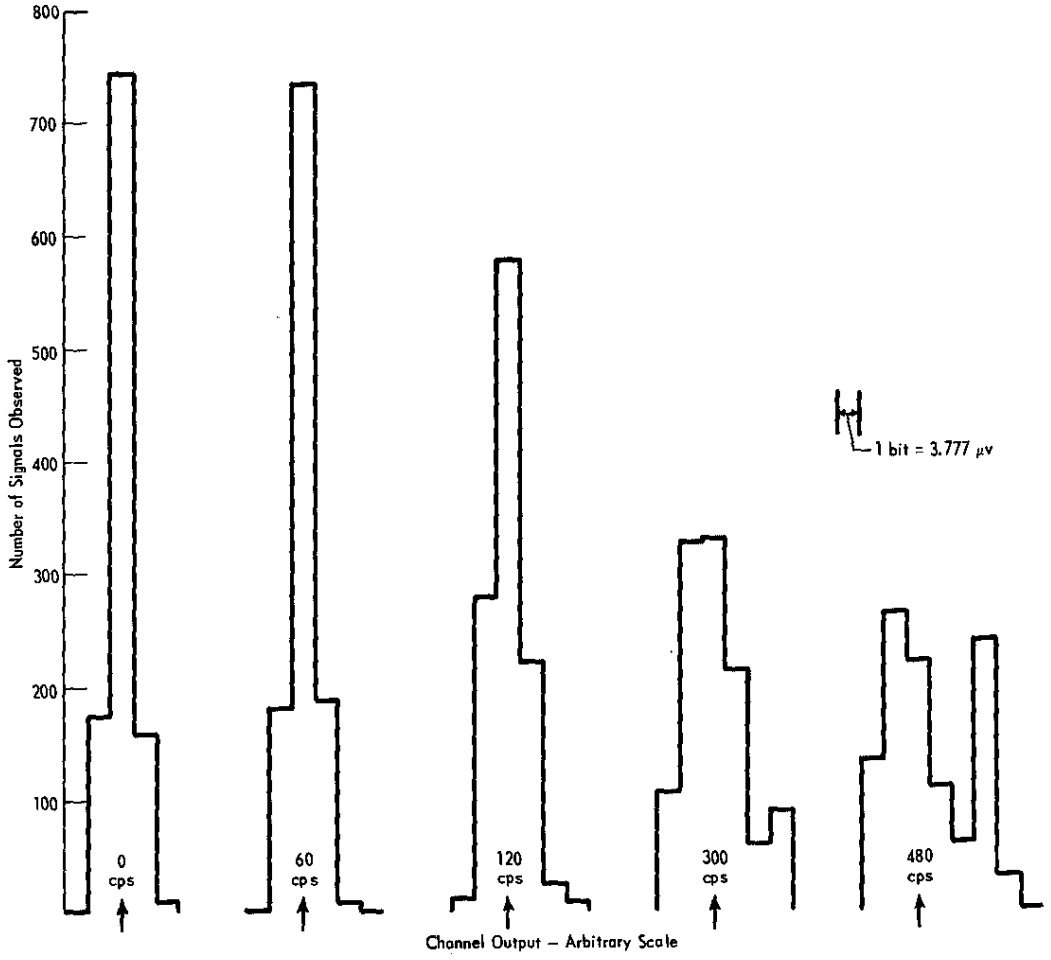

FIG. 20 EFFECT OF COMMON MODE SIGNALS AT DIFFERENT FREQUENCIES IN RELAY COMMUTATOR (Arrow points to same bit position in all distributions)

Resolution of Relay and Solid State Commutators

Input Change, bits	Output Change, bits	
	Relay Commutator	Solid State Commutator
0	0	0
1	1.13	1.37
2	2.04	2.17
3	2.95	3.11

CROSSTALK

Crosstalk is the effect on one channel of the signals in all other channels of the system. In systems that are directly coupled, crosstalk can arise from deficient insulation between the input circuits which permits leakage current from the "off" channels to cause a potential drop of measureable magnitude in the "on" channel. In the present system where only a virtual direct coupling is used, the major contribution to crosstalk is incomplete discharge of the coupling capacitors by the dc-restore switches. The worst condition arises when all inputs but one are at full scale.

The measurement of crosstalk was made by selecting an input and taking data for two cases; (1) all other inputs have the same potential as the selected one, and (2) all other inputs are raised to a potential equal to the full scale of the system. The difference, if any, in the magnitude of the signal on the selected channel for the two cases is due to crosstalk. Results of this test for several channels in the solid state and relay commutators are in the following table. In all cases, crosstalk adds an error of less than 0.5 bit to the selected channel output.

Crosstalk Measurements

Channel No.	Median Value[a] All Channels At Same Potential	Median Value[a] All Other Channels At Full Scale	Difference In Bits
Solid-State Commutator			
000	0.69	0.38	-0.31
004	.54	.48	-0.06
033	.44	.05	-0.39
Relay Commutator			
000	.71	.62	-0.09
001	.63	.52	-0.11
084	0.62	0.37	-0.25

(a) Median taken around an arbitrary zero value for reference input.

STABILITY

A system of this kind must consistently deliver a constant output signal for a constant input signal — for periods of minutes or months.

The short-term stability of the system is demonstrated in the following table, which shows the median values of histograms taken at two-minute intervals from a channel selected at random.

Short-Term Stability Data

Time, min.	Median Channel Reading,[a] bits
0	0.80
2	0.79
4	0.82
6	0.77
8	0.76

(a) Median taken around an arbitrary zero value for reference input.

The response of the system to environmental factors, chiefly temperature, affects both the long and short term stability. The laboratory in which the tests were conducted is temperature controlled by an ordinary thermostat to approximately 24°C ±0.5°C. By turning the controller off, the laboratory was allowed to come to an equilibrium temperature of 27.7°C. Data was taken before the temperature rise and at equilibrium at the higher temperature. Some of the results of this test are shown in the following table. Because there are only two transistor switches in the relay commutator, one for the odd inputs and one for the even inputs, the data in the table are arranged to show any differences between the odd and even channels. The table clearly shows that the even-numbered channels have a higher temperature coefficient than the odd-numbered channels. The transistors for the low-level switches were not matched for temperature tracking because it was planned to provide a constant temperature oven for the switches if it proved necessary. In the meantime, matched pairs of transistors that track to within 50 μv over a 100°C span have become commercially available. In any event, the data for the solid-state commutator show that with a modicum of selection, a temperature coefficient of ±2 μv/°C, or less, could be obtained.

Temperature Coefficient Measurements

Channel	Temperature Effect, μv/°C	Channel	Temperature Effect, μv/°C
	Relay		Solid-State
27	-0.06	00	+0.03
31	+0.06	11	-0.04
37	-0.11	16	-0.29
57	+0.35	25	+2.69
81	-0.13	32	-0.12
83	-0.09	49	+0.39
38	+0.63	74	+0.69
58	+0.20	85	+1.96
80	+0.24	90	+1.91
82	+0.38	91	+0.17
94	+0.35	93	-0.14
96	+0.13	94	+0.77
		95	+2.06
		96	-7.71
		97	-0.08
		98	+3.26

The behavior of the transistor switches over periods of months is of interest because differential "ageing" of the two transistors comprising a switch will produce an offset voltage in series with the signal. To determine the long term stability of the system, histograms of the system output for several channels were taken daily over a period of 5-1/2 months. The median values of these histograms, referred to an arbitrary "zero", are plotted as a function of time in Figure 21. There is some correlation between the temperature variations during the test period and the variations of the individual channels. The cause of the upward shift near 8/19/64, observed in all channels, is not known. Channel 004 in the solid state commutator also shows an erratic, although small, variation whose cause is unknown. Such rapid changes are, however, unlikely to be caused by ageing effects and may be due to a mechanical or electrical fault such as a corroded or improperly soldered connection. It has been mentioned before that it is impossible to determine the physical condition of the individual switches without disassembling the entire commutator. It should be borne in mind, however, that the variations seen in Figure 21 include changes due to any cause in the entire analog chain for these channels. Thus, the over-all stability is better than ±1-1/2 bit (±5.67 μv) over a 5-1/2 month period for these channels. Other observations made at intervals during this period indicate that these channels are representative of the entire system.

RELIABILITY

The reliability of the analog portion of the system has been excellent. The system has operated continuously since completion on 5/1/63. In this period (≈500 days) there have been no failures of electronic components. The relays in the relay commutator have now been in operation for a total of 16,500 hrs ($\approx 6 \times 10^8$ contact closures each). During this time there have been 10 relay failures (out of a total of 208). The first three failures occurred after 1700 hours of operation, the fourth after 4000 hours, the fifth and sixth after 5000 hours, and the remaining four during the last 11,000 hours.

There has been only one transistor failure in the solid-state commutator. This occurred at the time the system was started up, and was the result of a defective hermetic seal on one of the switching transistors.

CONCLUSIONS

From the results of these tests it has been concluded that this system is capable of performing to the original design intent, i.e., the speed, accuracy, and reliability of the system enable it to provide "continuous" temperature protection for a nuclear reactor having up to 2496 coolant channels.

Although the relay commutator has been demonstrated to have somewhat less noise in its output and a greater uniformity between channels than does the solid-state commutator, the choice for a full scale system would almost certainly be in favor of transistor switching. The reason for this choice would be primarily that of over-all reliability. While the relays have performed very well in this respect, their failure rate is higher than it is for transistors, and the lower noise output of the relays will undoubtedly be approached with better switching transistors and other design improvements.

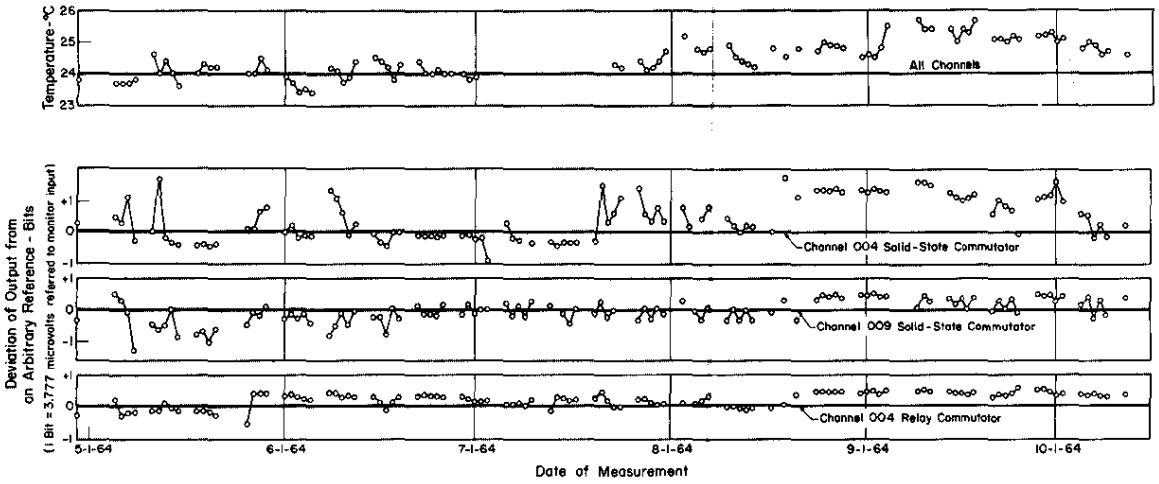

FIG. 21 LONG-TERM STABILITY OF MONITOR
(No data taken over weekends or holidays)