4:15pm - 4:30pm **Room 203**
DLTA13.3

Low-Voltage-Threshold Microlasers

J.L. Jewell[1], A. Scherer[2], M. Walther[2], J.P. Harbison[2] and L.T. Florez[2]
[1]*Photonics Research Inc., 350 Interlocken Pkwy., Suite 245, Broomfield, CO 80021*
1-303-465-6497
[2]*Bellcore, 331 Newman Springs Rd., Red Bank, NJ 07701*

We have reduced the voltage required for threshold in vertical cavity surface emitting lasers (VCSEL) to 1.7 V [1], the lowest yet reported for a CW-operating VCSEL [2,3]. Room-temperature current threshold was 3 mA pulsed, 4 mA CW. This advance in VCSEL technology leads to manageable heat dissipation for high packing densities. It was achieved in a structure which can be further optimized for high wallplug efficiency and high powers. Furthermore the thickness of the molecular beam epitaxially (MBE) grown portion of the structure was reduced by about 1.5 μm compared to conventional VCSELs, resulting in decreased MBE costs, significantly shallower processing depths and easier integration of VCSELs with transistors or other electronics. The (resistance x area) products of our VCSELs are nearly as low as those reported for high-power edge-emitting lasers. MBE was used to grow n-doped $Al_{0.15}Ga_{0.85}As/GaAs$ bottom mirror layers, the active region containing 3 GaAs quantum wells, and a 1-μm-thick p-doped top contact layer. 12 pairs of alternating SiO_2/Si_3N_4 layers formed a high-reflectivity mirror which completed the laser cavity. The reactive sputter-deposited mirrors produce reflectivities of 98.3% for 9.5 pairs [3]. Individual laser elements were defined by ion milling of mesas through the p-n junction, followed by planarization with SiO_2 to define the current path. Then, Au-Zn p-contacts were deposited around the mesa tops and alloyed for current injection. A final ion-milling step was used to isolate individual contacts. In this way microlasers with diameters ranging from 7.5-25 μm were fabricated and measured.

The p-side resistance is reduced by heavily Be-doping the top of the cavity and completely avoiding current flow through the well/barriers inherent in epitaxially-grown mirror/contact structures (Fig. 1). This configuration reduces the series resistance of 12-μm-diameter laser elements to about 70 ohms, averaged between the bandgap voltage, 1.45 V, and the 2.0 V operating voltage, which produced 8.5 mA (Fig. 2). Resulting (resistance x area) products are $<8\times10^{-5}\ \Omega cm^2$, nearly as low as the $<5\times10^{-5}\ \Omega cm^2$, calculated for high-power single-mode edge-emitting lasers [4]. The threshold currents and voltages of 12 μm diameter lasers were measured to be 3 mA and 1.7 V, respectively (Fig. 2). We measured peak powers >1 mW from 12 μm devices at 1% duty cycle with 20 mA. Although the measured quantum efficiency is not particularly high, this is most likely due to overly-high reflectance in the top mirror since the threshold current is reasonably low. Much higher powers and efficiencies are expected from similar, more optimized devices. Under CW operation the lasers show 4 mA threshold current.

Another advantage of this laser design over monolithic laser structures lies in the relaxation of accuracy required during crystal growth. Even if the cavity length is not tuned correctly to the quantum well emission wavelength and the bottom mirror reflectivity maximum, the top dielectric mirror stack can be redesigned to compensate for the inaccuracy. In this particular wafer, a large degree of such re-tuning was required (about one quarter wave, corresponding to about half a free spectral range, i.e. the maximum amount of re-tuning possible). This implies that if the epitaxial growth is accurate enough that the bottom mirror is highly reflecting at the gain wavelength, then it is possible to fabricate a laser. This tolerance is much wider than that allowed by the requirement in a monolithic structure to match the cavity resonance to the gain wavelength, perhaps ±3 % rather than ±1 %. This increased tolerance will increase wafer yield. Large adjustments complicate the laser design since the $GaAs/Si_3N_4$ interface actually reduces the mirror stack reflectivity.

We have shown that it is possible to obtain VCSELs from a hybrid design, with greatly reduced resistance allowing for lower operating voltages, and that the stringent accuracy requirements on the MBE crystal growth required for monolithic VCSELs are relaxed. In optimally-grown structures, we expect lower threshold currents, much higher wallplug efficiencies, higher powers and higher speeds than obtained with previous VCSEL designs [5].

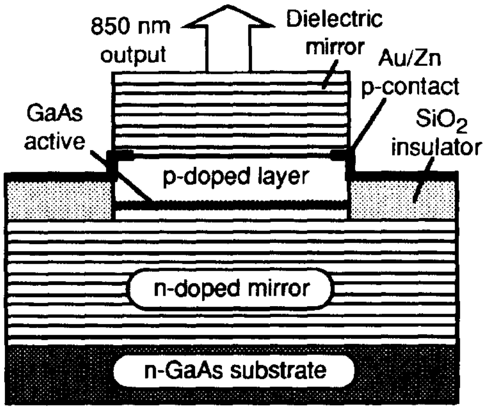

Fig. 1. Schematic of the VCSEL structure.

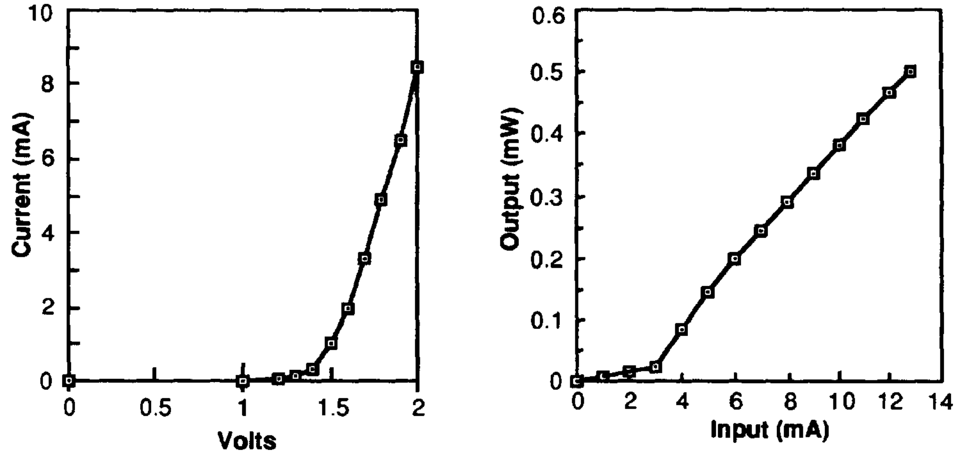

Figure 2. Characteristic I-V and L-I curves of a pulsed 12-μm-diameter VCSEL.

References

[1] A. Scherer, J.L. Jewell, M. Walther, J.P. Harbison and L.T. Florez, "Fabrication of Low Threshold Voltage Microlasers," Electron. Lett., to be published.

[2] E.F. Schubert, L.W. Tu, R.F. Kopf, G.J. Zydzik, and D.G. Deppe, "Low-threshold vertical cavity surface-emitting lasers with metallic reflectors," Appl. Phys. Lett. **57** 117 (1990).

[3] A. Scherer, M. Walther, L.M. Schiavone, B.P. Van der Gaag, "Reactive sputter deposition of high-reflectivity dielectric mirror stacks," J. Vac. Sci. Technol., to be published.

[4] Spectra Diode Labs SDL-5400 series (100 mW) has 4 Ω resistance in a 3-μm-wide by 400-μm-long area, or $4.8 \times 10^{-5}\ \Omega cm^2$.

[5] J.L. Jewell, J.P. Harbison, A. Scherer, Y.H. Lee, L.T. Florez, "Vertical Cavity Surface Emitting Lasers: Design, Growth, Fabrication, Characterization," IEEE J. Quantum Electron. **27** 1332 (1991).