Submitted to the 1997 GaAs REL Workshop, October 12th, 1997

Accelerated lifetime testing and failure analysis of quartz based GaAs planar Schottky diodes

R. Lin, I. Mehdi, A. Pease, R. Dengler, D. Humphrey, T. Lee, A. Scherer*, and S. Kayali

Jet Propulsion Laboratory
*California Institute of Technology

Address inquiries to:
I. Mehdi, M/S 168-314, JPL, 4800 Oak Grove Drive, Pasadena, CA 91109
Voice (818) 354-2001, Fax (818) 393-4683

ABSTRACT

Accelerated lifetime tests have been performed on integrated planar GaAs Schottky diodes that were bonded to quartz substrates up-side-down with a heat-cured epoxy. Results at 175°C, 200°C, and 240°C were analyzed using the Arrhenius-lognormal model. These tests predict a room temperature MTTF of $3x10^8$ hours, a value that is comparable to conventional high-frequency planar Schottky diodes. This result demonstrates that the use of an appropriate epoxy to obtain GaAs devices on quartz substrates does not significantly reduce the lifetime of the devices.

I. Introduction

For very high frequency applications, quartz is a desirable substrate material, because it has lower loss and lower dielectric constant than GaAs. One possible method of obtaining semiconductor devices on quartz substrates is to use a bonding agent such as epoxy. A technique, named QUID (for Quartz substrate Up-side-down Integrated Device), has been developed to produce GaAs Schottky diodes on quartz substrates for millimeter and submillimeter wave applications [1,2]. In this technique, planar GaAs Schottky diodes are mounted up-side-down onto quartz substrates for space-borne radiometers that operate at frequencies up to 640 GHz. After successful performance demonstration, it is now desirable to study the failure mechanisms associated with such structures.

Figure 1 shows a cross-sectional schematic of the QUID structure. The anode of the Schottky contact is made with a T-like structure at the end of a long strip of metal that extends over a central air gap. Two such diodes are arranged in an antiparallel configuration. Following the integration of the diode with the RF microstrip filter circuitry, the entire circuit is bonded upside-down onto a 50 micron thick quartz substrate with a heat-cured epoxy [3]. This bonding agent also fills the air gap under the fingers, and this may be a factor in the device's reliability. Finally, all of the GaAs substrate is etched except for two small mesas around the active region with the two planar diodes [4].

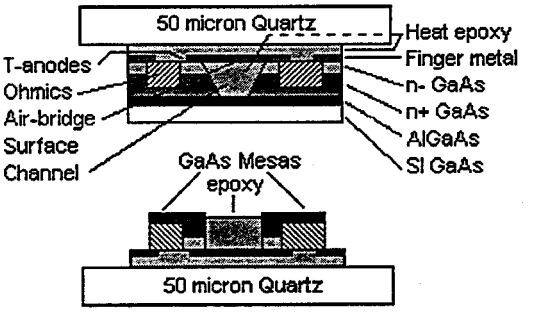

Figure 1: Cross-sectional schematic of the starting and ending point of the QUID process.

II. Accelerated Lifetime Procedure

The model used for the accelerated lifetime tests is the Arrhenius-lognormal model. This model is widely used for GaAs devices [5], and states that the failure times for a batch of devices have a lognormal distribution about the median time to failure (the time for 50% of the devices to fail). This median time to failure, in turn, is related to absolute temperature by the relation

$$t=t_0\exp(E_a/kT), \qquad (1)$$

where t is the mean time to failure, E_a is the activation energy measured in eV, k is Boltzmann's constant, and T is the absolute temperature.

An automated system was used to conduct the accelerated lifetime tests [6]. The QUID structures were placed unbiased in a nitrogen-purged high-temperature oven for an extended period of time. The temperature was slowly ramped up from room temperature with the devices already mounted inside the oven. Device IV characteristics were monitored *in-situ*, once every hour, with a computer-controlled data-acquisition system. Nominally fifteen devices, or thirty anodes, were tested at each of three temperatures: 175°C, 200°C, and 240°C. These devices were mounted onto ceramic chip carriers using two-part epoxy and gold wire bonds, and subsequently placed in a high-temperature wiring fixture designed to withstand 250°C.

In defining what constitutes a failure for the QUID structures, we use a failure criteria based on the DC IV characteristics that may help us predict the device's performance degradation at RF frequency applications. A device is considered to have failed if any of three conditions is met: (1) diode ideality factor, η, changes by 10%, (2) diode series resistance, R_s changes by 20%, (3) diode turn-on voltage, V_0 (voltage where current is 1 μA), changes by more than 20%.

The zero percentage change baseline for each of these three parameters is calculated by averaging a diode's parameter during the first few measurements at the test temperature. This is to smooth out some of the noise due to measuring errors. For each device, when any of its three parameters meets the failure criteria, the time since the beginning of the test temperature period is recorded. The failure times are plotted on a lognormal graph paper, and an apparent linear regression line is constructed to determine the median time to failure and the standard deviation at each temperature.

III. Results and Discussion

Figure 2 shows the lognormal distribution plots for the three lifetime tests. The standard deviation is 0.2 for the 175°C test, and 0.6 for both the 200°C and 240°C test. The three median times to failure are then plotted against temperature to give the Arrhenius plot, shown in Figure 3. The best-fit line, when extended to 23°C, gives an estimated mean time to failure at room temperature of 3×10^8 hours. This is comparable to the values obtained in previous studies of planar Schottky diodes at the University of Virginia [7,8]. Assuming a single failure mode is responsible at all three temperatures, the slope of the line gives an activation energy of 0.94 eV.

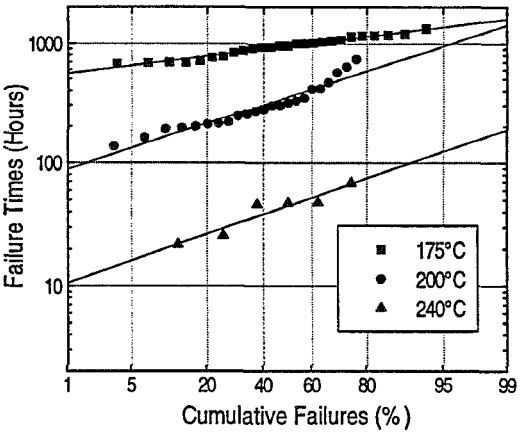

Figure 2: Device failures at 175°C, 200°C, and 240°C. Failure criteria is either $|\Delta\eta|>10\%$, $|\Delta R_s|>20\%$, or $|\Delta V_0|>20\%$.

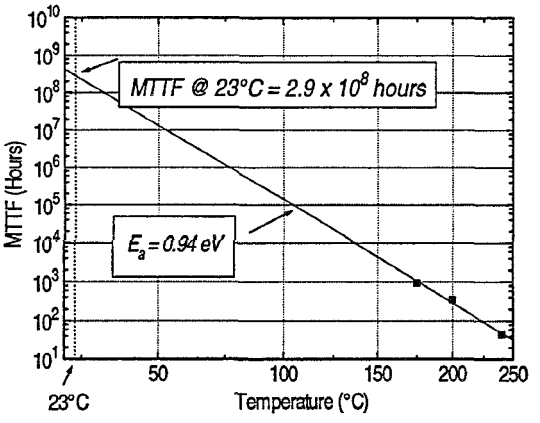

Figure 3: Arrhenius Plot for JPL 640 GHz QUIDs

It must be noted that the test performed at 175°C was not conducted with the same high-temperature fixture that was used in the other two tests, but with standard circuit boards. Data from this test showed that all devices experienced a common degradation cycle around 600 hours. Since such a behavior was not observed for the test performed with the high-temperature fixture, it is assumed that the unexpected behavior in the 175°C test data was caused by degradation of the circuit board rather than the QUID structures. This may also explain the lower standard deviation value for this test in figure 4. It is likely that the failure times at 175°C are under-estimated, and that we have calculated a conservative value for the MTTF at room temperature.

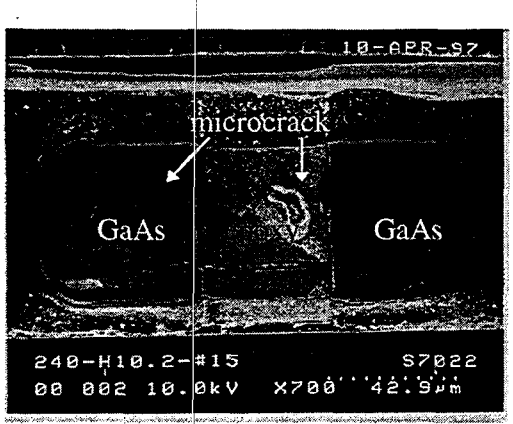

Figure 4: SEM photo of a QUID structure after 240°C lifetime test. This device failed catastrophically, and there is a crack in the epoxy and GaAs mesas.

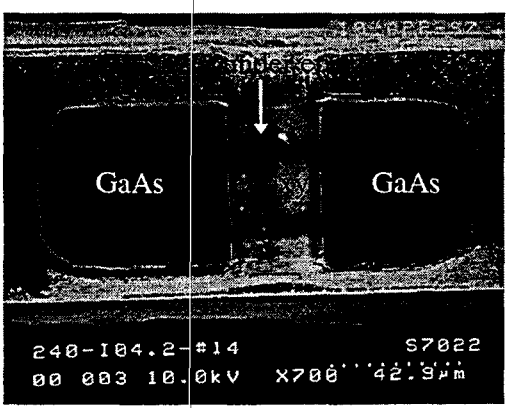

Figure 5: SEM photo of a QUID structure after 240°C lifetime test. This device degraded gradually, and shows no signs of cracks in the GaAs mesas.

An attempt was made to determine the mechanisms that were responsible for device failures. Following the accelerated lifetime test, devices were inspected with an optical microscope and a scanning electron microscope. The SEM analysis showed that there are at least two types of failure mechanisms, and that they are related to different failure paths. Figure 4 shows a device that failed catastrophically (that is, its IV characteristic changed abruptly), and figure 5 shows a device that failed gracefully (that is, its IV parameters slowly degraded before it met the failure criteria).

The observed crack in figure 4 seems to be along the length of the two fingers in the central epoxy region, and along a crystal plane in the semiconductor region, but no such crack is found in figure 5. If this mechanical deformation reached the Schottky contact region, it may have caused the abrupt electrical change. The high-temperature stress possibly caused a structural stress buildup before it was released in the form of a catastrophic crack. Currently we are investigating other non-structural failure mechanisms that might be responsible for the devices that failed with gradual degradation.

IV. Conclusions

Based on results from accelerated lifetime tests at three different temperatures, the 640 GHz QUID circuits were determined to have a room temperature MTTF of $3x10^8$ hours, with an activation energy of 0.94 eV. Based on the SEM inspections, it was shown that there is a correlation between cracks in the device structure and catastrophic failures in the electrical behavior. Other failure mechanisms are responsible for non-catastrophic failures, since structural deformation was not observed for all devices that failed with gradual degradation. Results from further reliability tests and failure analyses will enable us to better understand these mechanisms. The MTTF values obtained from this work show that the QUID process can be a useful technique to obtain GaAs devices on non-semiconductor substrates. This technique could also be useful for other applications where a dissimilar substrate is required.

V. Acknowledgments

The authors would like to acknowledge S. Martin for help in the device fabrication, B. Fujiwara for wire bonding, and K. Evans for the SEM images. We are also grateful to Dr. Peter Siegel and Karen Lee for technical discussion and for the support of this investigation. The research described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

VI. REFERENCES

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[2] I. Mehdi, T. H. Lee, D. A. Humphrey, S. C. Martin, R. J. Dengler, J. E. Oswald, A. Pease, R. P. Smith, and P. H. Siegel, "600 GHz Planar-

Schottky-diode subharmonic waveguide mixers," in *IEEE MTT-S 1996 Digest*, pp. 377-379.

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[4] I. Mehdi, M. Mazed, R. Dengler, A. Pease, M. Natzic, and P. H. Siegel, "Planar GaAs Schottky diodes integrated with quartz substrate circuitry for waveguide subharmonic mixers at 215 GHz," in *IEEE Intl. Microwave Symp. Digest*, pp. 779-782, 1994.

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[7] S. M. Marazita, "A Reliability and Failure Mechanism Analysis of Planar and Whisker-contacted GaAs Schottky Diodes," *B.S. thesis*, University of Virginia, 1994.

[8] J. L. Bowers, "Reliability of Planar GaAs Schottky Diodes," *M.S. Thesis*, University of Virginia, 1993.

Accelerated Lifetime Testing and Failure Analysis of Quartz based GaAs Planar Schottky Diodes

R. Lin, I. Mehdi, A. Pease, R. Dengler, D. Humphrey, T. Lee, A. Scherer, and S. Kayali

Jet Propulsion Laboratory

California Institute of Technology

This research was carried out under a contract with the National Aeronautics and Space Administration

We acknowledge the support of P. Siegel, K. Lee, K. Evans, and B. Fujiwara

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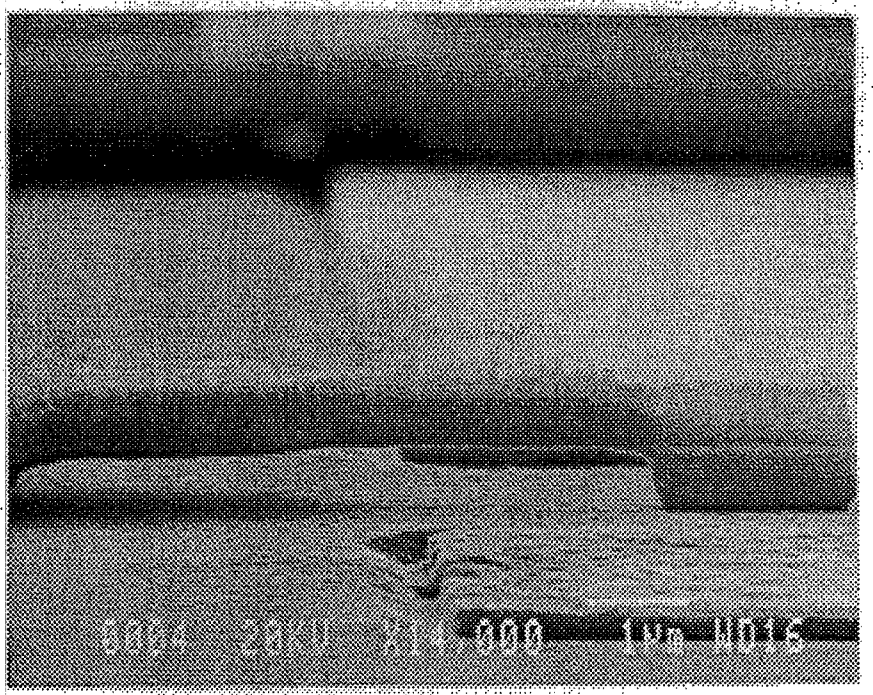
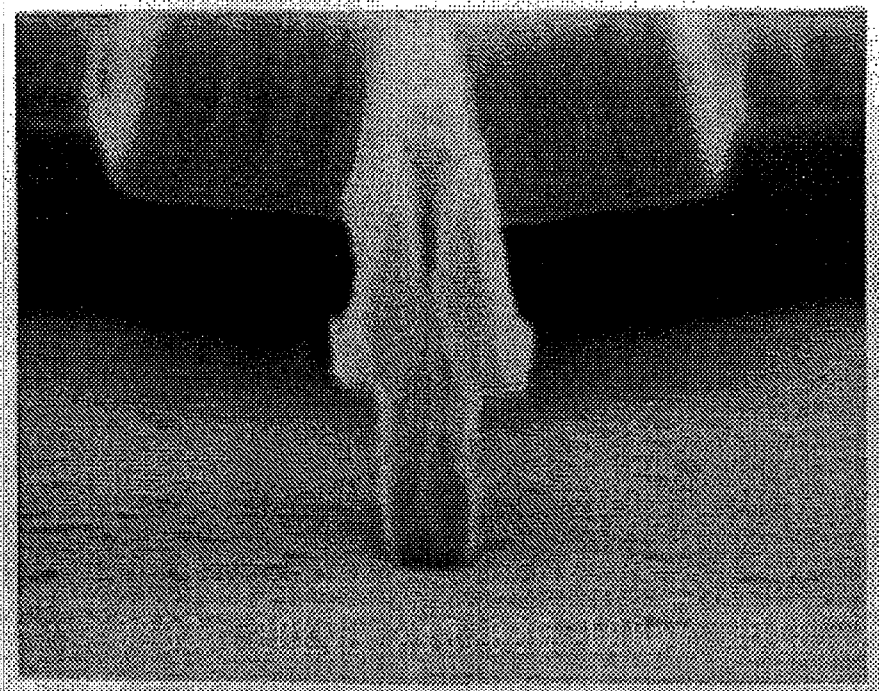
Introduction

- Planar Schottky diodes are being developed at JPL for various mm/sub-mm wave space-borne instruments.
- The diodes are utilized in a waveguide circuit and thus require a low-loss substrate.
- Quartz, because of its low-loss and mechanical robustness, is the preferred substrate.
- Technology has been developed that integrates GaAs planar Schottky diodes with quartz-based circuitry.

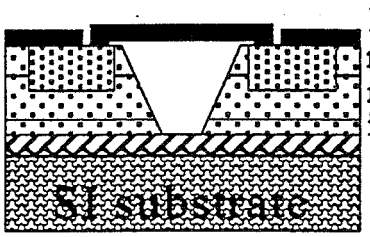
➡ *This technology has resulted in very sensitive subharmonic mixers up to 640 GHz*

JPL 640 GHz T-anodes

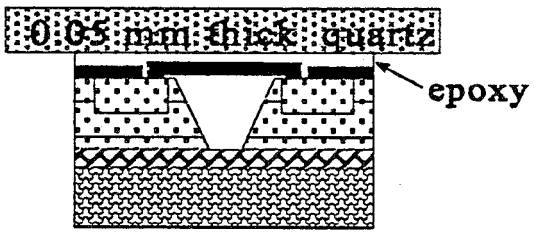




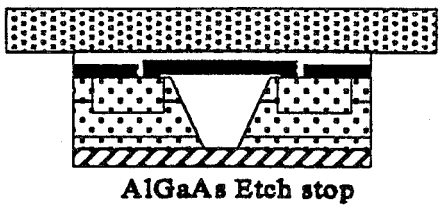
QUID (Quartz-substrate Up-side-down Integrated Device) PROCESS



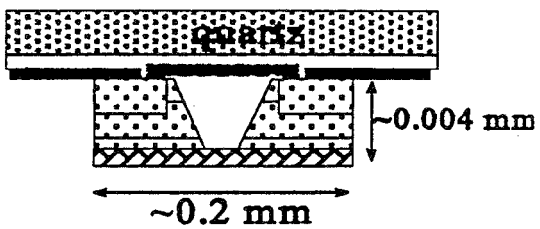
Completed planar Schottky diodes with surface channel



Up-side-down mounting with epoxy



Substrate removal



Backside alignment and etch

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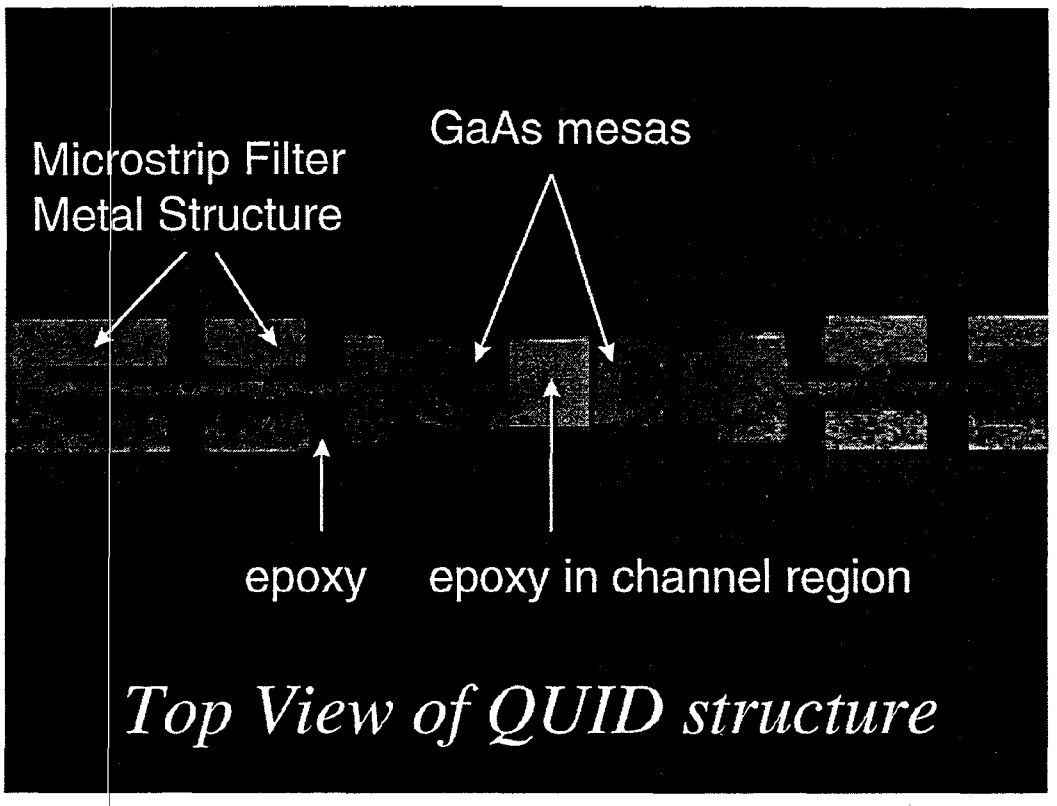
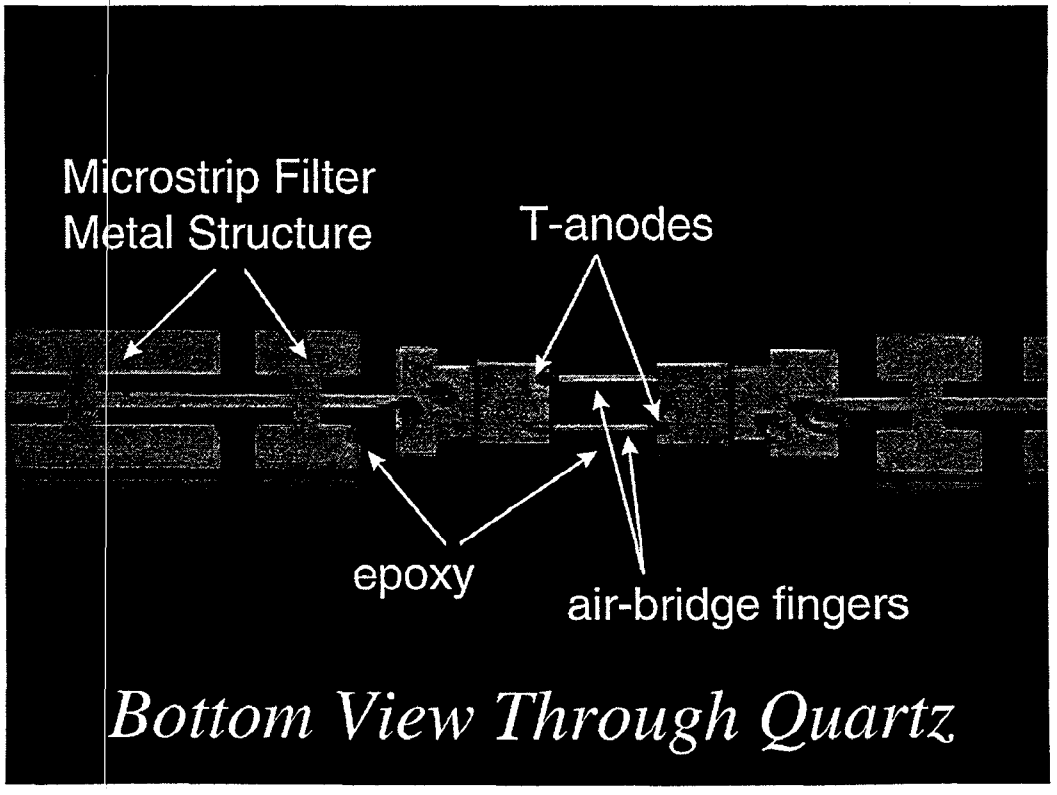
QUID Structure





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Reliability Issues

- No prior reliability data
- Mission lifetime is five (5) years
- Effect of **epoxy, finger length**, and other processing variations on reliability

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➡ Accelerated Lifetime Test

- *Model Used: Arrhenius-Lognormal*
- *Temperatures: 175°C, 200°C, 240°C*
- *Sample Size: nominally 30 anodes per temp.*

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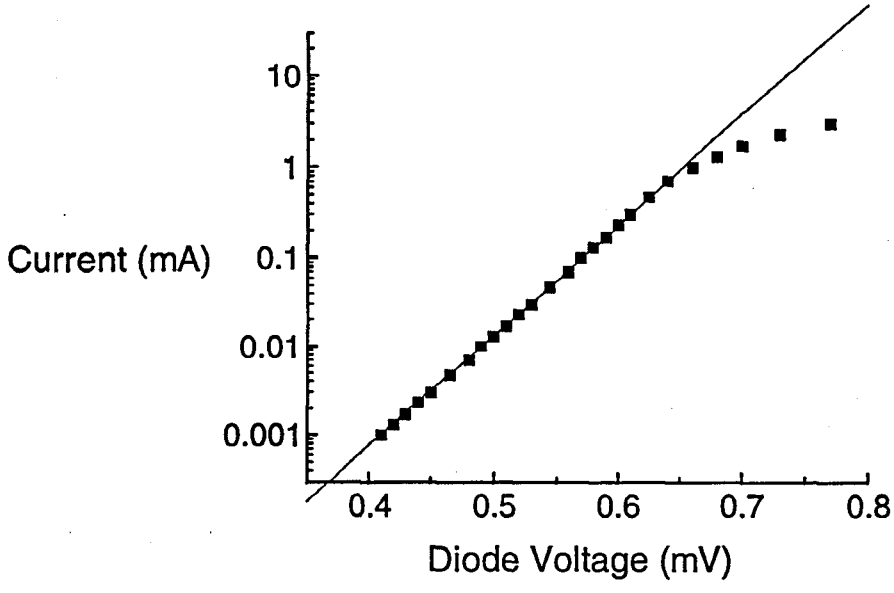
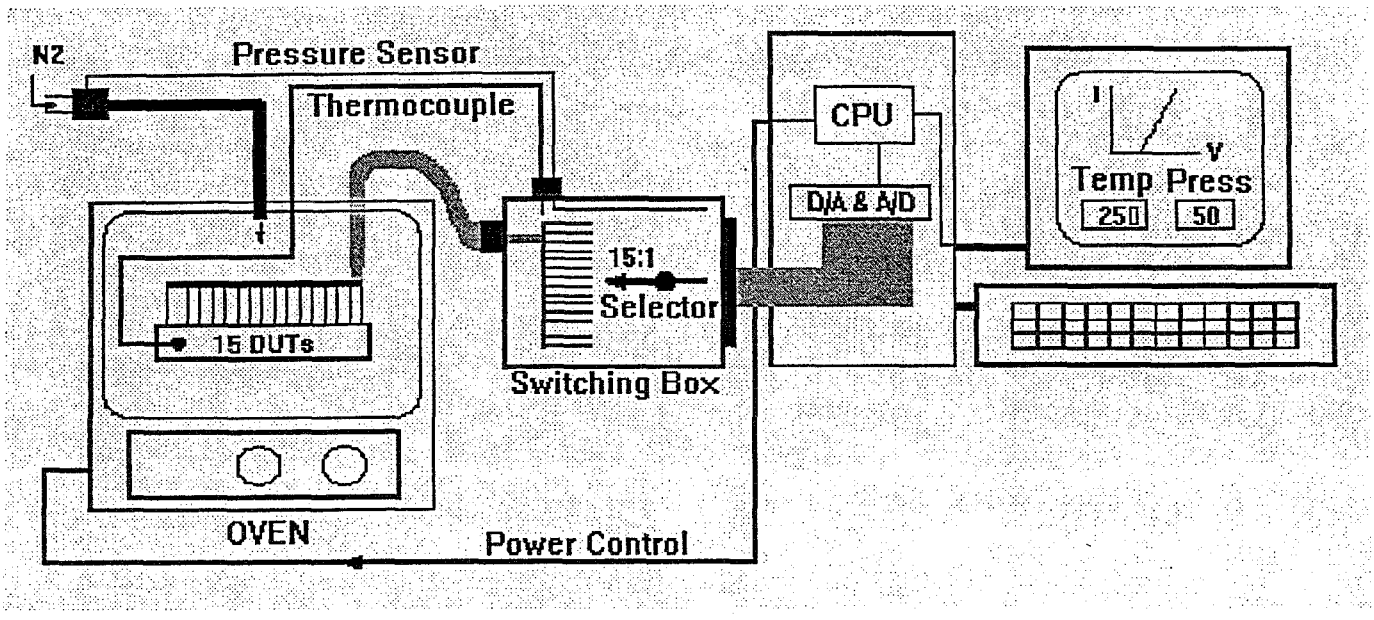
Failure Criterion

Typical Schottky diode I-V curve



Failure Criteria are based on degradation of DC I-V

1. Catastrophic failures:
   - *open, short, abrupt change in I-V*
2. Gradual degradation:
   - *ideality factor (η) changes 10%*
   - *series resistance (R_s) changes 20%*
   - *knee voltage (V_0) changes 20%*

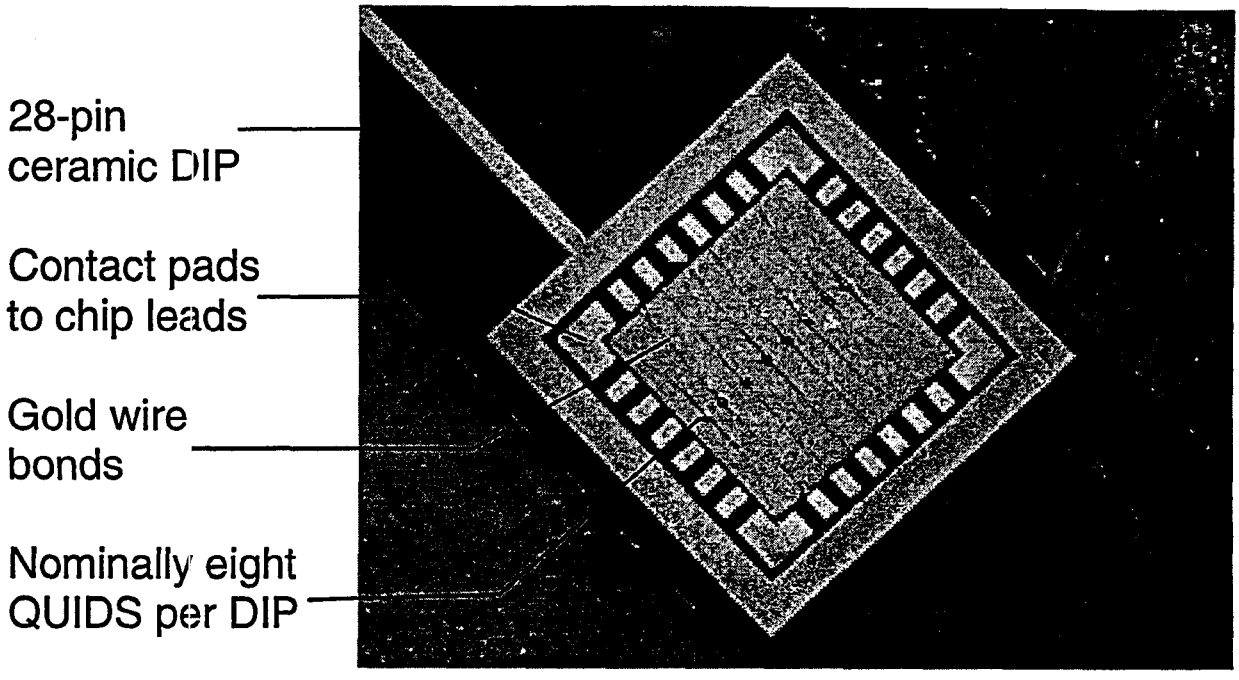


Automation Hardware

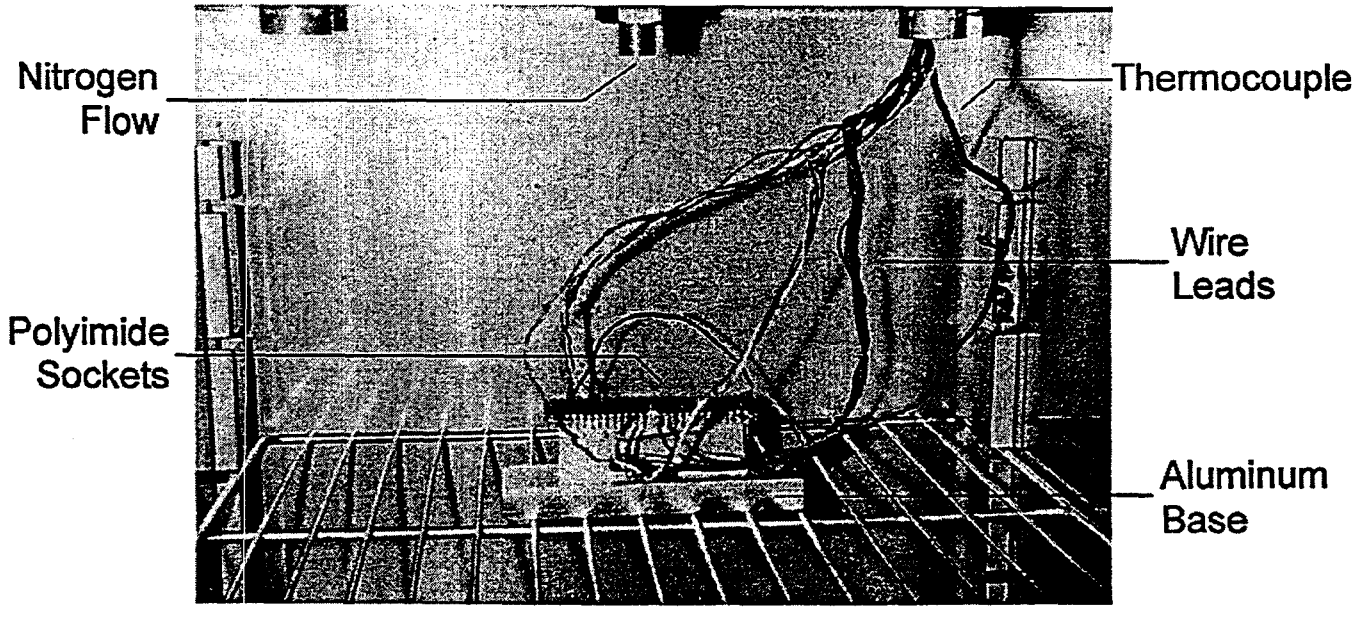
- Range: Ambient - 250°C
- Nominally 30 anodes per test
- In-Situ I-V Measurements
- Nitrogen Purged Oven

Automation Software

- temperature control
- timer
- IV data acquisition
- device switching between DUTs



640 GHz QUID Mixers Mounted on Chip Carrier for Thermal Lifetime Tests



High Temperature Mounting Fixture

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Data Collection and Analysis Procedure

1. Device I-V characteristics taken every hour
2. Device η, R_s, V_0 are tracked
3. Failure time = time when percentage change meets failure criteria (0% baseline = average of first 3-5 points)
4. Plot failure times vs. cumulative failures on lognormal scale
5. Plot median times to failure vs. temperature
6. Calculate MTTF and E_a from Arrhenius fit

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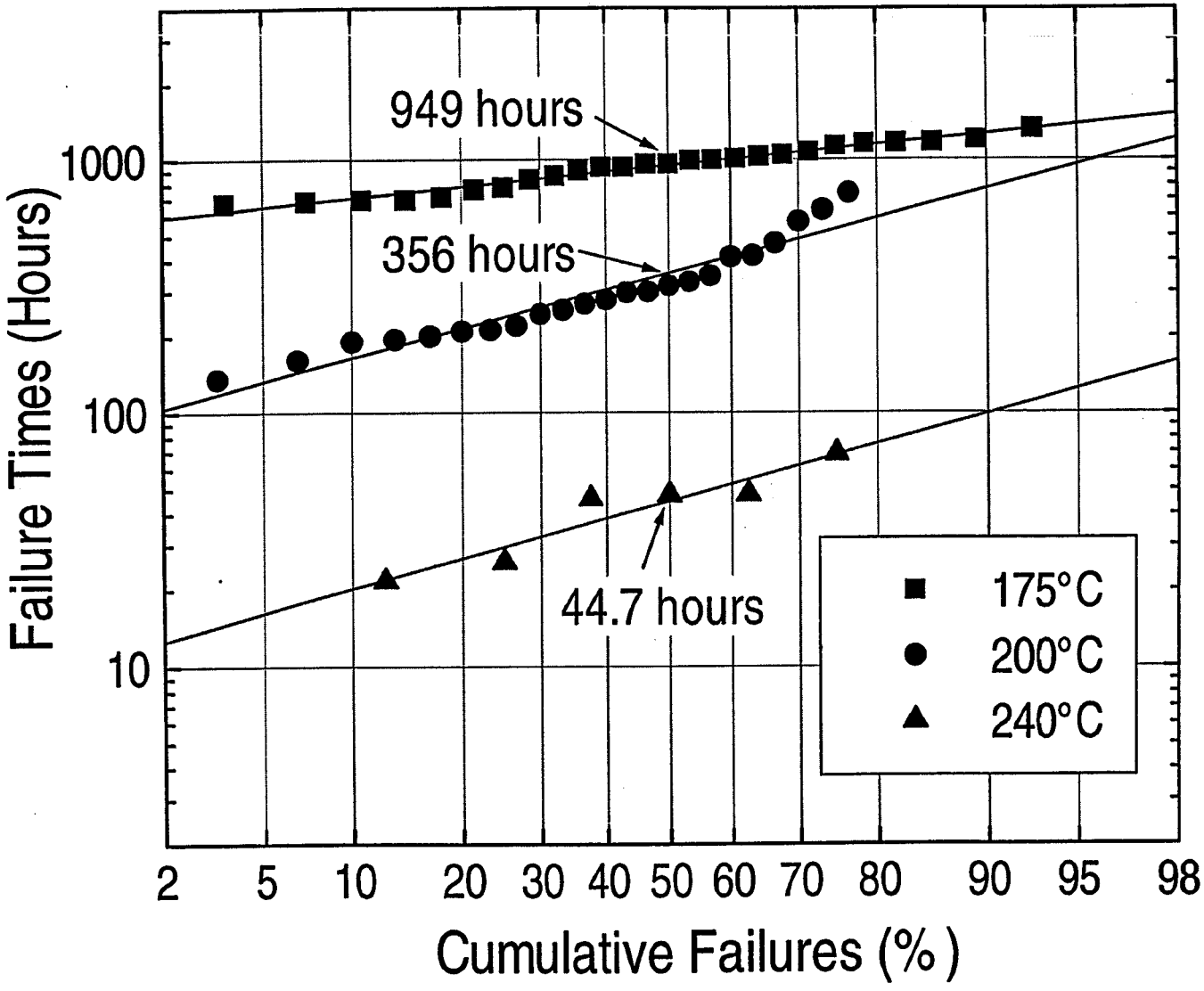
Lognormal Plot



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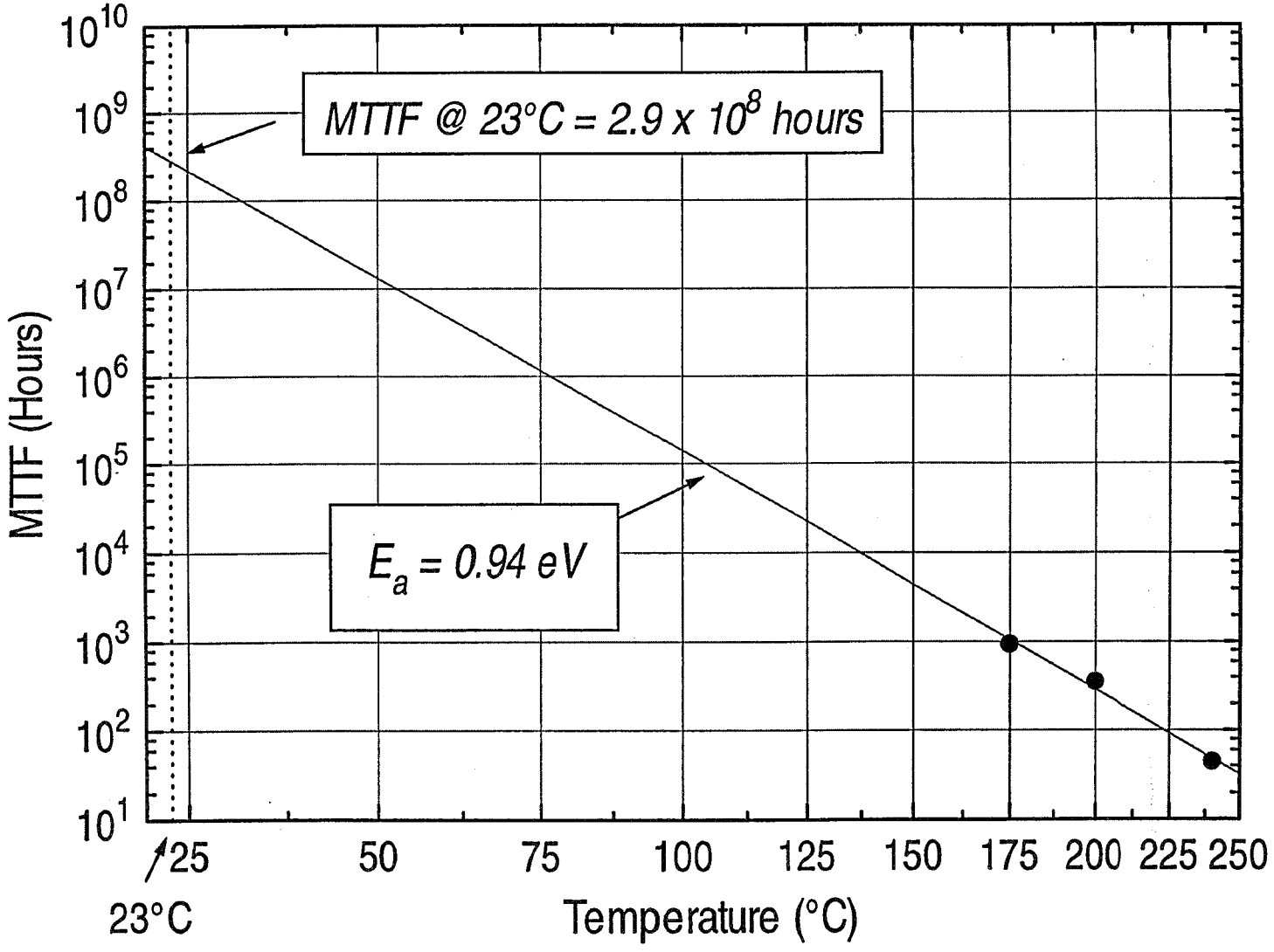
Arrhenius Plot



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Failure Analysis

Tools:

- *Visual inspection*
- *SEM inspection*
- *Electron Dispersive Spectroscopy*

Effect of temperature on

- *epoxy*
- *mechanical structure (fingers, GaAs mesa, T-anode, filter metal)*
- *quartz/epoxy/GaAs interface*
- *quartz/epoxy/Au interface*

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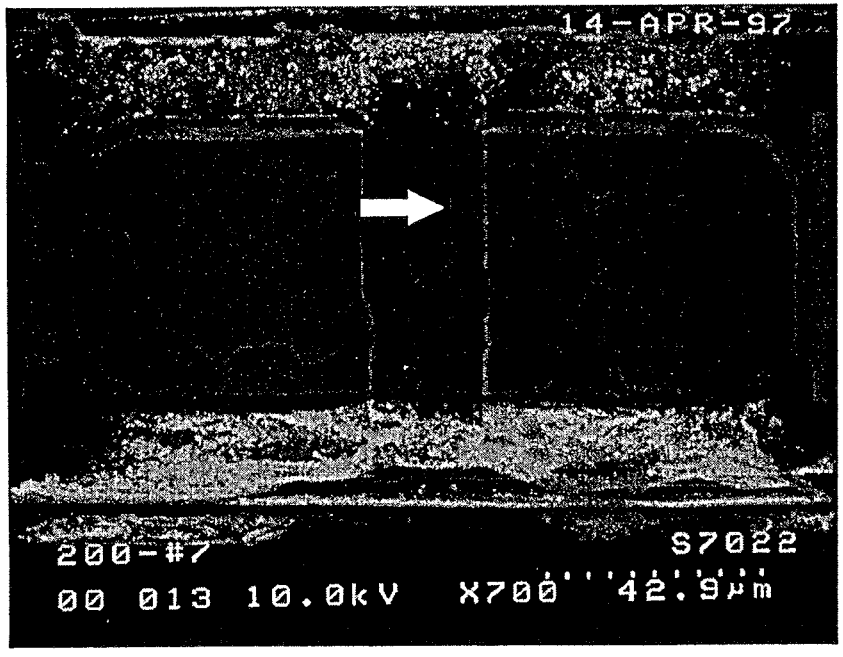
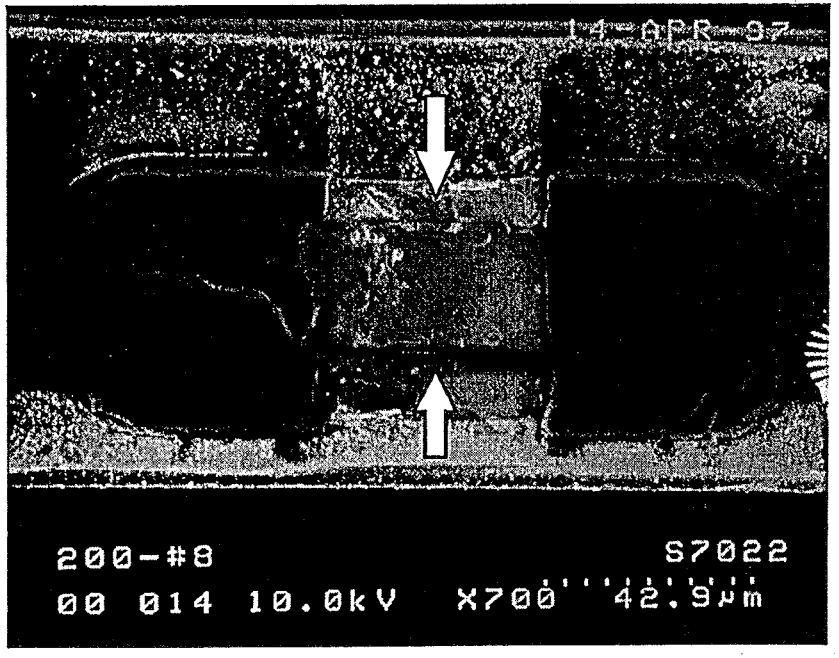
SEM Images from 200°C Lifetime Test

- Tested for >700 hours
- Observed cracks in epoxy region between GaAs mesas
- Device 7 is a catastrophic failure





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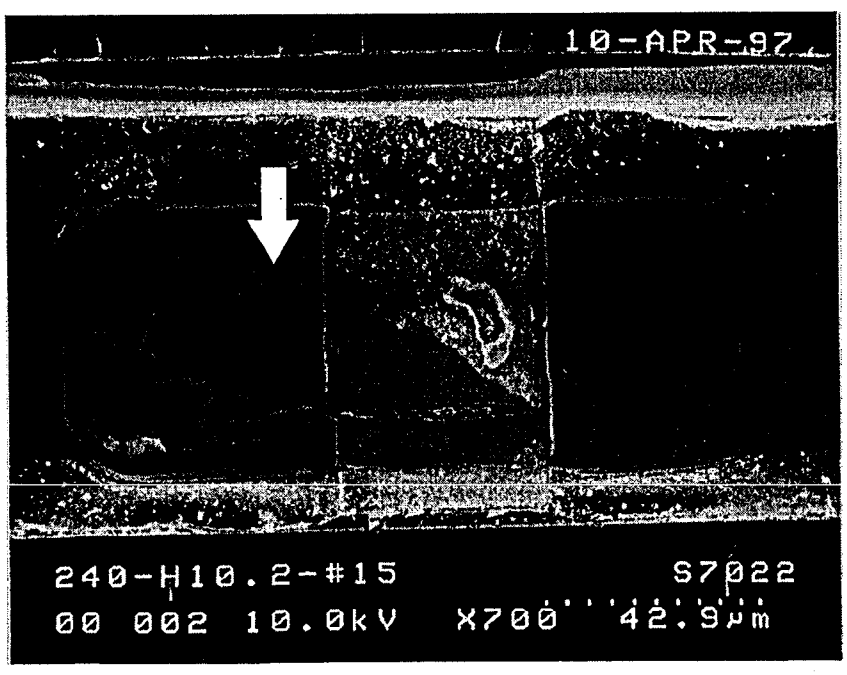
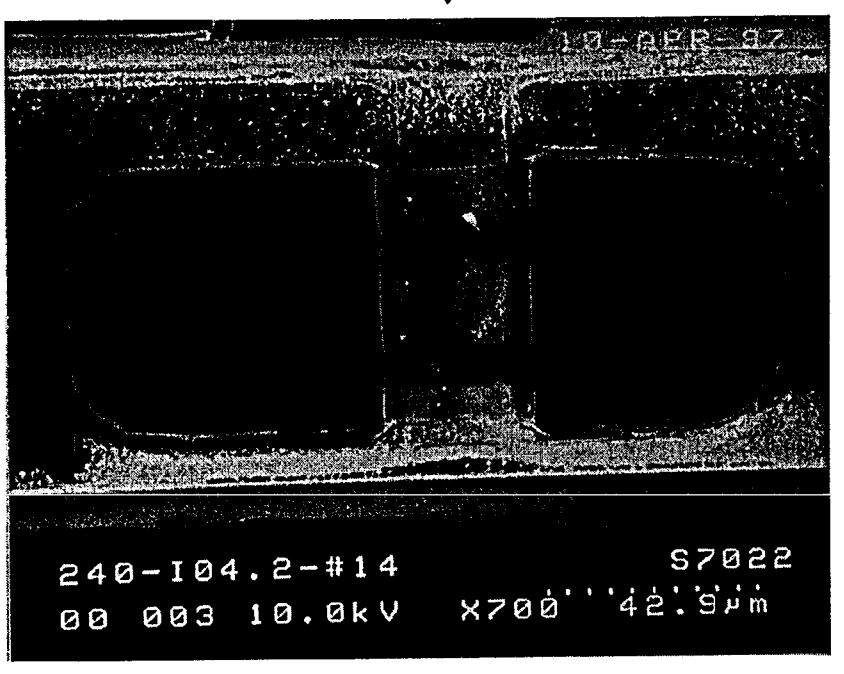
SEM Images from 240°C Lifetime Test

- Tested for >400 hours
- Observed cracks on GaAs mesas
- Device 14 failed by gradual degradation





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Conclusions

Accelerated Lifetime Test Result for 640 GHz QUIDs:

- *MTTF at room temperature: 3 x 10^8 hrs (>30,000 yrs)*
- *Activation Energy: 0.94 eV*

Two types of failures:

- *Catastrophic failure -- caused by cracks in epoxy or in GaAs crystal structure near anodes*
- *Gradual degradations -- caused by other non-structural failure mechanism*

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Current / Future Investigations

- Additional Accelerated Lifetime Tests
  - *Lower Temperatures*
  - *Confidence Bands*
  - *Other devices:*
    - Nitride passivated
    - Epoxy-etched
  - *Continuous DC Bias, RF Bias*
- Other Reliability Tests
  - *Step-Stress Test*
  - *Thermal Cycling Test*
  - *Electrostatic Discharge Test*