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Bolometric Detectors for the Planck Surveyor

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ABSTRACT

The High Frequency Instrument on the NASA/ESA Planck Surveyor, scheduled for launch in 2007, will map the entire sky in 6 frequency bands ranging from 100 GHz to 857 GHz to probe Cosmic Microwave Background (CMB) anisotropy and polarization with angular resolution ranging from 9' to 5'. The HFI focal plane will contain 48 silicon nitride micromesh bolometers operating from a 100 mK heat sink. Four detectors in each of the 6 bands will detect unpolarized radiation. An additional 4 pairs of detectors will provide sensitivity to linear polarization of emission at 143, 217 and 353 GHz. We describe the fabrication process used to meet the stringent mission requirements on sensitivity, speed of response and stability.

Keywords: Bolometers, Millimeter-wave, Planck

1. INTRODUCTION

Planck was selected in 1996 as the Medium Mission M3 of the Horizon 2000 Plan of the European Space Agency (ESA). The Planck mission is dedicated to the goal of imaging the Cosmic Microwave Background (CMB) with high angular resolution and sensitivity. To achieve this goal, Planck uses a 1.5 m, passively cooled (~50K) off-axis telescope and two focal plane instruments that together span a factor of ~ 30 in frequency, with 9 bands centered from 30 to 857 GHz. The Low Frequency Instrument (LFI) uses High Electron Mobility Transistor (HEMT) amplifiers in 4 bands at 30, 45, 70 and 100 GHz. The High Frequency Instrument (HFI) uses bolometric detectors in 6 bands at 100, 143, 217, 353, 545, and 857 GHz. The combined spectral coverage of the two instruments will allow precise separation of the faint patterns of CMB temperature and polarization anisotropy from the many astrophysical sources of foreground confusion, including synchrotron, thermal dust emission, and the Sunyaev-Zeldovich distortion of the CMB itself. Accurate measurements of the power spectra of the temperature and polarization anisotropy of the CMB angular scales of ~ 5' to a few degrees provide a uniquely powerful probe of the structure and evolution of the universe. In addition to

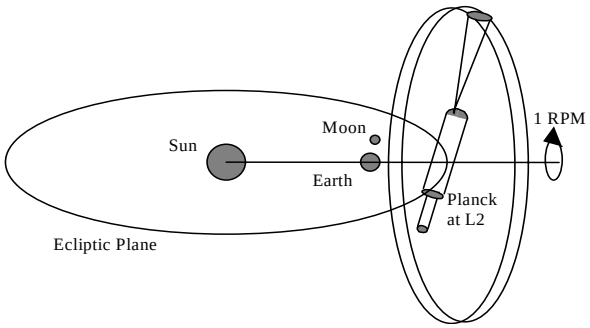

Figure 1. The Planck scan pattern

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this primary science goal the HFI, which will survey the entire sky with greater than 10' resolution, will detect tens of thousands of extragalactic compact sources of emission, with a high probability of discovering new classes of objects.

Planck is schedule to be launched in 2007 on an Arianne 5 launch vehicle into a halo orbit around the L2 libration point of the Earth-Sun system. From this vantage point – 10^6 km from the Earth opposite the Sun - Planck will scan the sky in close-to-great circles approximately orthogonal to the Earth-Sun axis, mapping the entire sky every 6 months. Careful shielding of the telescope from the Sun and the Earth allows the telescope to cool passively to ~ 50K, decreasing the background on the detectors to close to the astrophysical backgrounds in all of the mm-wave bands. The LFI and HFI observe simultaneously, sharing a large (~ 5^o diameter) focal plane. The 1 rpm scan rate sets a requirement on the minimum signal bandwidth of the detectors of 80 Hz ($5'/\theta_{beam}$), as well as a requirement that the detectors be stable on timescales on order of the 1minute rotation period

In this paper, we describe the process used to fabricate the bolometric detectors that are designed to achieve near background-limited performance at each of the 6 HFI bands. In order to achieve the necessary combination of sensitivity and thermal response time, the HFI bolometers must be operated from a heat sink temperature of ~ 100 mK. The necessity of cooling the detectors to this temperature drives the entire architecture of the HFI. A hydrogen sorption cooler cools the environment surrounding the HFI (including the LFI) from the ~ 50K of the passively cooled telescope to ~ 20K, and provides a heat sink temperature of < 19K for the HFI cooling chain. A Sterling cycle cooler provides cooling from 19K to ~ 4K. The 4K stage completely encloses the HFI, providing a heat sink for the feedhorns and infrared filters at the focus of the telescope, as well as forming a Faraday cage that shields RF interference that could dissipate appreciable power at the lower temperature stages. An open-cycle dilution refrigerator operating from the 4K heat sink provides further cooling at 1.6K and at 100 mK. The 1.6K stage is used to heat sink filters that block infrared emission that propagates through the horns. The 100 mK stage cools the focal plane, consisting of 36 re-concentrating feedhorn optics, band-defining lowpass filters, and 48 bolometric detectors. Twenty-four of the feeds (4 at each of the 6 bands) couple to a single bolometer that detects both linear polarizations. The remaining 12 feeds (4 at each of 143, 217 and 353 GHz) each couple to a pair of polarization sensitive detectors, each of which detects a single linear polarization.

In 1997, in response to an invitation by the HFI consortium, NASA selected JPL to develop the bolometric detectors for Planck. The original specifications did not include polarization sensitive bolometers. These have been developed (see Jones et al., this volume) beginning in 2000, in response to the growing desire to provide Planck with the highest possible sensitivity to CMB polarization [1].

JPL is responsible for delivering a total of ~ 100 detectors to the HFI, including several engineering model (EM) devices, 18 Cryogenic Qualification Model (CQM) devices (one + one spare of each of 9 types, and 72 Proto-Flight Model (PFM) devices (48 detectors + 50% spares). Each of the CQM and PFM devices will have undergone a full program of vibration and thermal qualification and electrical and optical testing at JPL before being delivered to the HFI project (see Holmes et al., this volume) [2].

2. DETECTOR REQUIREMENTS

The bolometric detectors in each band are required to achieve a Noise Equivalent Power (NEP) less than that due to statistical fluctuations in the photon background. This requirement sets an upper limit on the thermal conductivity G between the absorber and the heat sink, given by the relationship

$$NEP = \gamma(4kT^2G)^{1/2}$$

where T is the temperature of the heat sink and γ accounts for the contributions to the noise due to the finite sensitivity of the thermometer, and is of order 1.3 for the semiconductor thermistors employed in the HFI bolometers. A lower limit to G is determined by the requirement on the speed of response of the detectors, together with the relationship

$$\tau = \beta(C/G)$$

where C is the heat capacity of the detector and β, which accounts for the decrease in the effective thermal time constant due to electrothermal feedback, is on order of 1.6 for optimally biased semiconductor thermistors of the type employed in the HFI bolometers. These two requirements can be satisfied simultaneously only if the heat capacity of the device is less than

$$C_{max} = NEP^2/(4\,\beta\,\gamma^2 kT^2)$$

$\sim 1.0\ (\tau/5\ \text{msec})\ (NEP/(10^{-17}\ W/Hz^{0.5}))^2$ pJ/K for $\gamma = 1.3$, $\beta = 1.6$ and T = 100 mK. Table 1 gives the requirements on NEP, thermal time constant τ, and heat capacity C which are derived from the estimated background loading on each of the detectors, the 1 rpm scan speed, and the FHWM beamsize for each band.

Table 1. Required Bolometer Performance

Frequency [GHz]	Beamwidth [arcmin]	τ_{max} [ms]	Background [pW]	BLIP [aW/Hz$^{0.5}$]	G_{max} [pW/K]	C_{max} [pJ/K]
100	9	7.9	1.1	13	180	2.5
143	7	6.2	1.2	16	270	3.0
143 pol	7	6.2	0.6	11	130	1.4
217	5	4.4	1.2	19	270	2.1
217 pol	5	4.4	0.6	13	180	1.4
353	5	4.4	1.2	24	610	4.8
353 pol	5	4.4	0.6	17	310	2.4
545	5	4.4	4.8	59	3700	29
857	5	4.4	15	131	18000	140

In practice, the design value for the thermal conductivity G is set at least ~ 1.5 x below G_{max} in order to allow for margin in fabrication, and it is desirable to allow the realized value of G to fall as much as a factor of 2 below G_{max} in order to ensure high yields. Thus, the maximum allowable heat capacity may be as much as a factor of two below the values given in the table.

In addition to the thermal properties described above, the bolometers are required to have an impedance in the range of 2.5 MΩ to 10 MΩ in order to ensure proper coupling to the amplifier chain, and to exhibit no appreciable 1/f noise above frequencies (~ 30 mHz) that would degrade the sensitivity of the all-sky images. Finally, the efficiency of optical coupling to the detectors, which is a function of the area and impedance of the absorber, must be sufficient to give an overall system optical efficiency (including all losses in the telescope, feedhorns, filters and bolometer) of > 25%.

3. DETECTOR DESIGN

The design of the detector which meets these requirements is based on the "spider-web" architecture pioneered for the BOOMERANG balloon-borne experiment. The detector architecture is illustrated in Fig 2. Radiation is absorbed via a free-standing silicon nitride micromesh that is metalized to tune its surface impedance for maximum absorption efficiency. The grid constant within the absorber is small enough, typically $g < \lambda/5$, that the mesh approximates a solid absorber for the radiation in band. Using a mesh rather than a solid membrane decreases the cross-section of the detector to cosmic rays and high frequency electromagnetic radiation, minimizes the heat capacity of the substrate, and allows the metal film to be thicker, and thus more robust.

Thermal isolation of the absorber from the heat sink is achieved via un-metalized silicon nitride legs that mechanically support the absorber within its silicon frame. These legs are typically ~ 1 micron thick, ~ 3 microns wide and ~ 500 microns long, and contribute, in total, ~ 1 pW/K conductivity between the absorber and the 100 mK heat sink.

The desired thermal conductivity to the detector is achieved by tailoring the length, thickness and width of the Au electrical leads that make contact with the thermistor, which is located either at the center or at the edge of the absorber.

Conductivies in the range of 20 pW/K to 20 nW/K at 100 mK are easily achieved. The thermal efficiency of the bolometer, defined as the fraction of the absorbed power that contributes to a temperature rise of the thermistor, is a function of the geometry of the device, and of the relative thermal conductivities of the absorber, the mechanical support legs, and the electrical leads. A full discussion of the thermal efficiency is given in Turner *et al*. [7]. The thermal efficiency of the Planck detectors is typically 95%, and the internal web thermalization time constants are typically < 1 msec.

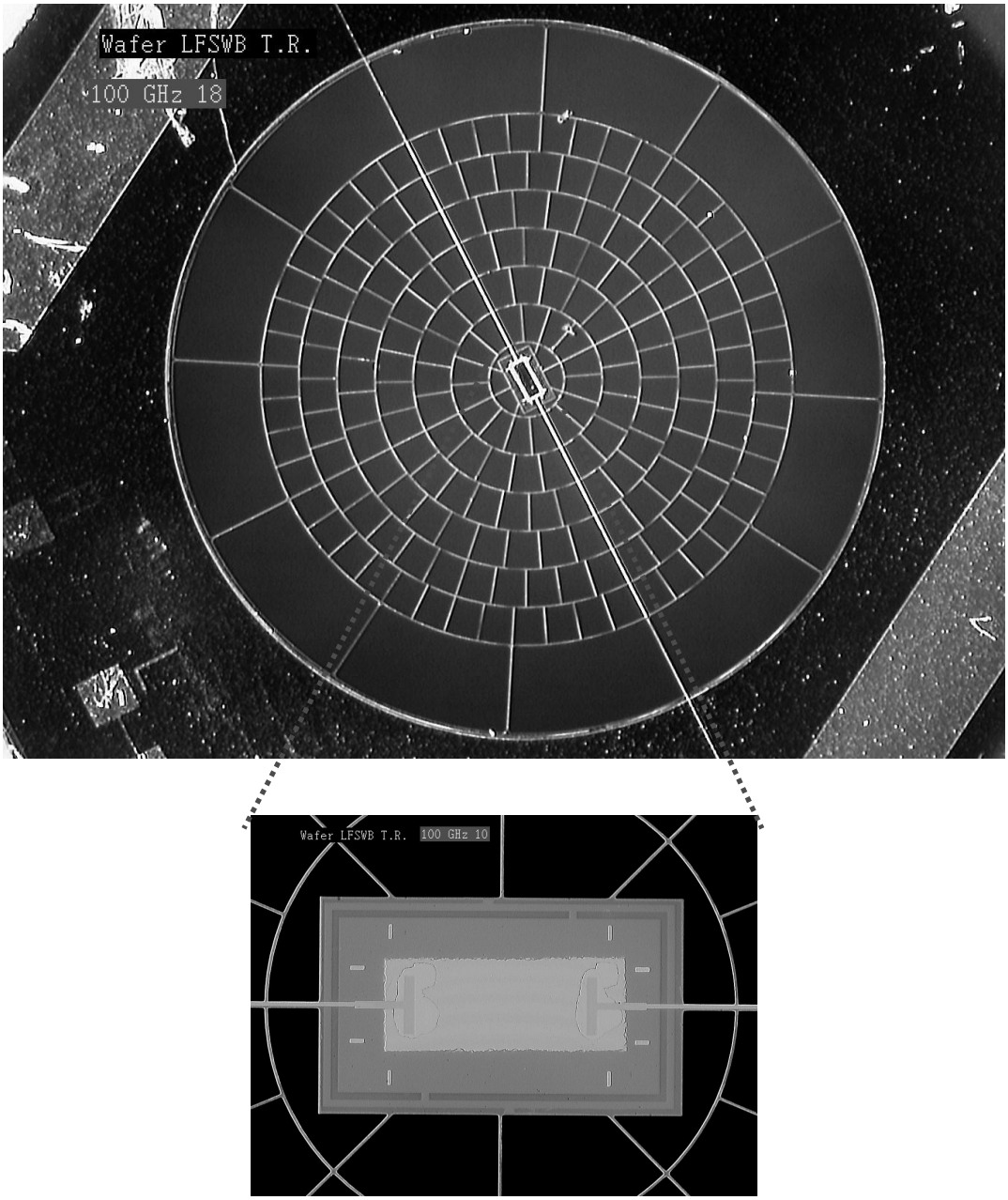

Figure 2. A 100 GHz PFM detector. The absorber is 4500 μm in diameter (see Table 2 for other parameters). The temperature rise of the absorber is measured via an NTD Ge thermistor positioned at the center of the web. The inset shows the In bump bonds that connect the themistor to the absorber.

In order to achieve precise control of the impedance and excellent low-frequency stability, we use Neutron Transmutation Doped (NTD) Ge themistors. These thermistors operate in the hopping conduction regime, and are extremely well understood. Small (20 μm x 100 μm x 300 μm) thermistors with carefully prepared ion-implanted contacts are In bump-bonded to the absorber. The total heat capacity of the thermistor and In bump bonds is < 0.3 pJ/K at 100 mK, well below the maximum allowed heat capacity for each detector type.

Table 2 gives the design parameters for the 6 types of "spider-web" bolometers that are produced for the Planck HFI. The design of the Polarization Sensitive Bolometers (PSB) is similar to that of the spider web detectors, and is described in detail in Jones *et al*. (this volume) [1].

Table 2. Detector Design

Frequency [GHz]	g [μm]	2a [μm]	d [μm]	ff [%]
100	320	4.8	4500	3
143	225	3.4	3160	3
217	160	2.4	2280	3
353	160	2.4	2280	3
545	110	6.4	2200	1.16
857	70	4	2100	11.4

g, grid spacing; 2a, line width in absorber; d, absorber diameter of active area; ff, absorber filling factor

4. DETECTOR FABRICATION

The HFI bolometers are fabricated at JPL's Micro Devices Laboratory (MDL). This laboratory has fabricated similar devices used for a variety of sub-orbital experiments, including BOOMERANG, MAXIMA, ARCHEOPS, and ACBAR. The lessons learned from these sub-orbital applications have proven extremely valuable to the effort to build the Planck detectors.

The fabrication of the Planck detectors poses unique challenges in that a very large number of detectors (~100) must be delivered to the project. Since it is time-consuming and costly to fully characterize each detector, there is a premium on achieving a high yield of detectors that meet all of the goal specifications. We have therefore designed the detectors to have the largest performance margins possible, and have designed the process to provide as low a dispersion in the critical properties – particularly the heat capacity – as possible.

The basic steps in the fabrication are illustrated in Fig. 3. The detectors are fabricated from thermally bonded SOI wafers with a (100) orientation. The use of the SOI wafer facilitates the deep etching that is required to form the free-standing absorber, as described below. The thickness of the top Si, buried SiO_2, and bottom Si layer are 2 μm, 1 μm, and 350 μm, respectively, with ±10% variation. First, the SOI wafers are prepared with a standard RCA cleaning. Then, 1 μm layer of Si_3N_4 [Fig. 3(a)], is deposited on each side of the wafer using low-pressure chemical vapor deposition (LPCVD). Because the Si_3N_4 layer will ultimate form a large (~ 5 mm) free-standing structure, care must be taken in the deposition of the Si_3N_4 to ensure that the material is free of stress and pinholes.

Next, a series of Ti-Au depositions form the absorber for optimal infrared absorption, the electrical leads which define the thermal conductance to the absorber, and the contacts and wiring layer for electrical readout. Ti-Au metal films are deposited using lift-off technique to form the absorber layer [Fig. 3(b)]. The thickness of the Au layer deposited on the absorber is chosen to give optimal infrared absorption, and is typically ~ 12 nm. The thickness of the Au layer forming the electrical leads on the supports is tailored to achieve the desired thermal conductance, and is typically several tens of nm. The thickness of electrical contacts of the array is typically ~500 nm [Fig 3(b)].

The wafer is then patterned to define the mask for the membrane [Fig. 3(c)], and etched first with an Ar reactive ion etch to remove the absorber Ti-Au layer followed by a CF_4 and O_2 reactive ion etch to remove the silicon nitride. The backside is similarly patterned, aligning to the frontside with an infrared camera, and reactive ion etched to remove the backside silicon nitride to define the silicon frame [Fig. 3(d)].

A 15 μm x 40 μm Ni-In bump [Fig. 3(e)] is deposited on each of the two contact pads located at the center of the device using liftoff lithography to deposit 40 nm Ni + ~ 3 μm In. The nickel layer is used as an intermediate layer to prevent reaction of the indium with the gold during and/or after processing. Before attaching the thermistors, the backside is patterned with photoresist and hard baked. Depending on the layout, there are typically 30 to 120 devices on a single 4" wafer. The wafers are diced into individual detectors before further processing.

The thermistors are manufactured from a polished slab of NTD Ge material by p doping with a 4.53 x 10^{16} /cc concentration of Ga and a 1.29 x 10^{16} /cc compensation of As. Two contacts are photolithographically defined on a single face of the chip. The contacts are B-implanted and deposited with 2 nm Ti + 20 nm Au. Two 15 μm x 15 μm In bump bonds are then patterned on each contact of the thermistor with the same Ni-In process used on the wafer. The chips are diced with a diamond saw and etched in a mixture of HF and HNO_3 to remove saw damage. The resulting chips are ~300 μm long, ~50 μm wide, and 25 μm thick with two contacts 100 μm wide and 50 μm long, separated by 200 μm.

The NTD Ge thermistor is located [Fig. 3(e)] over the contacts at the center of the absorber and attached by the In bumps with ~ 10 grams of force by a custom-made manipulator. We have experimented with a large range of bump-bonding force, from ~ 2 to several hundred grams, and found that reliable bonds can be made over the entire range if the bonding fixture is properly designed to balance the pressure on the two ends of the thermistor. The thermistors are subjected to a push test in which a lateral force of several grams is applied to the chip. The pad to pad impedance of the detector is monitored before and after the push test.

The active face of the detector, on which the thermistor is bonded, is now covered with wax in order to protect it during the following etch processes. This is a critical step in the fabrication, as it is essential that the wax seal the thermistor and the In bump bonds against the subsequent wet etch.

The first step in the silicon etch uses a deep trench reactive ion etch (DRIE) from the backside. The DRIE stops at the insulating layer [Fig. 3(f)], leaving only a residual Si membrane that is only a few microns thick. The DRIE is followed by liquid etches to remove the thin oxide and silicon layers [Fig. 3(g)]. We have used ICP (inductive coupling plasma) system for deep trench etching because ICP appears to be the most suitable source for this application [3]. This system allows high etch rates, anisotropic etching with selectivity to conventional photoresist masks [4]. The deep reactive ion etcher (DRIE) is manufactured by Surface Technology Systems (STS) and is a single wafer, load locked system that employs inductively coupled plasma etching with an Advanced Silicon Etch (ASE) process. The plasma is generated by an inductively coupled coil via a 13.56 MHz RF source with a maximum power output of 1000W. Another 13.56 MHz generator is used to apply the electrode, allowing independent control of the bias potential of the wafer with a power up to 300W. The wafer temperature is maintained below 80^{o}C via a temperature controller connected to LN_2 supplier. The system and reaction pressure is controlled by APC (automatic pressure controller). Typical base pressures are 1 x 10^{-7} Torr; operating pressures are from 1 mTorr to > 10 mTorr. During processing, the wafer electrode is lifted using a large bellows from the loading height to a processing height within 10 mm of the bottom coil. This reduces ion density loss by diffusion. The electrostatic chuck and platen assembly are cooled by a de-ionized water chiller system. Wafer cooling is provided by mass flow controlled helium on the backside of the wafer. Ion densities of the order of 10^{12} cm^{-3} are obtained at the center of the chamber. We have used SF_6 and C_4F_8 as the etch and passivation gases respectively. SF_6 is used during etch step to etch Si isotropically; this is followed by a short passivation step using C_4F_8. The SF_6 gas provides fluorine radicals that are isotropic silicon etchants. The C_4F_8 plasma deposits a polymeric passivating layer on the surface as well as on the side wall [4]. The directional ion energy supplied by the capacitive coupled electrode during the etch reaction preferentially removes the paasivation layer from the base of the features hence etching silicon spontaneously. The balance between etch and passivation determines the final process results and this balance can be controlled through a wide variety of process parameter such as etch time RF power, gas flow, and etch pressure.

The etch reaction starts via a standby step which consists of a high purity N_2 purge followed by a system purge. Then, etching gases of 130 sccm of CF_4 and 85 sccm of C_4F_8 are introduced using mass flow controller. The etch rate in this system is 2.2 μm/minute, with some variation depending upon exposed surface area and feature size. In general, to etch through the 350 micron bottom silicon layer takes about 160 minutes. The selectivity to etching relative to silicon is 150 : 1 for the oxide and 75 : 1 for the photoresist. The etch process stops on the buried oxide layer when the silicon has cleared. To complete the deep trench etch, the standby step is repeated and the load lock handler removes the wafer from the reaction chamber.

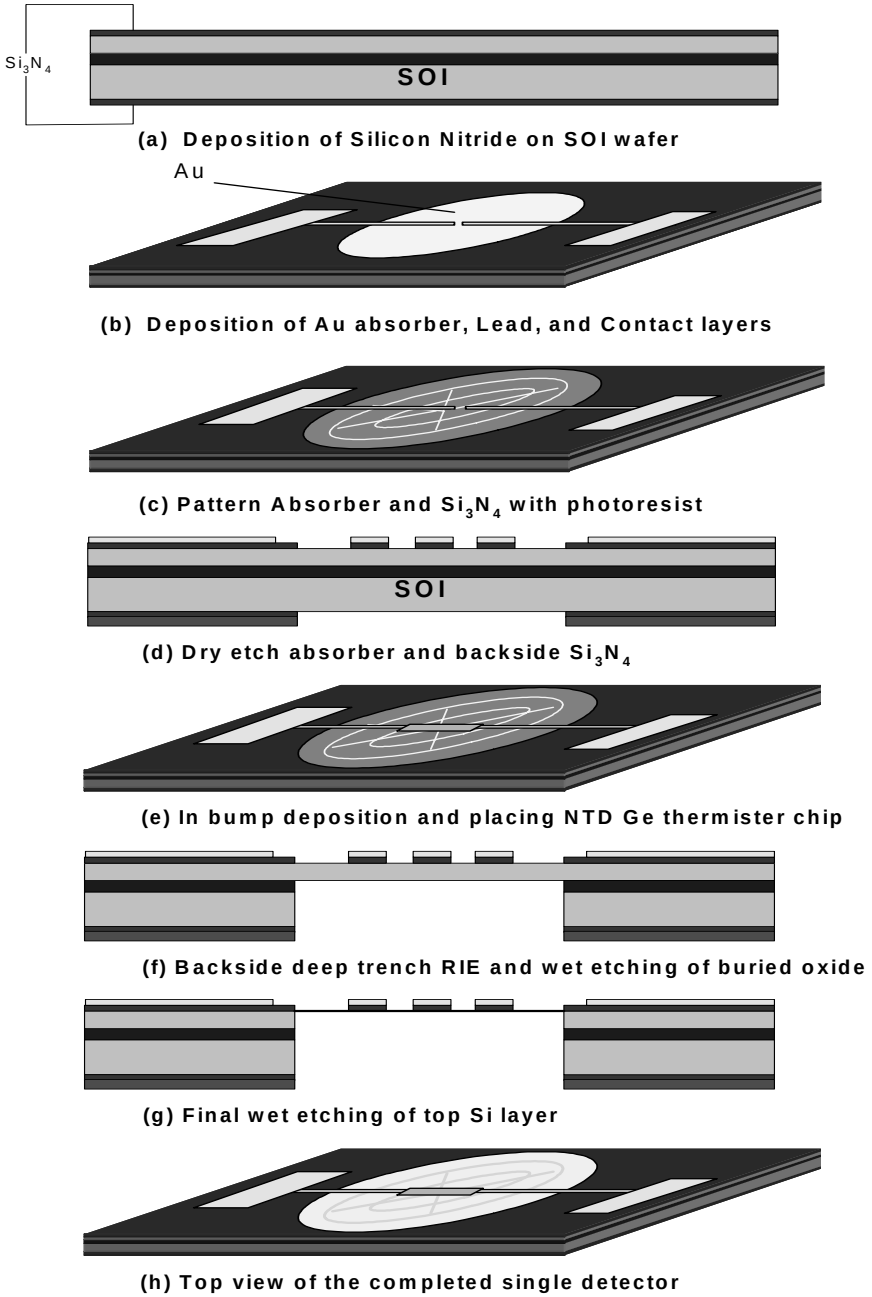

Figure 3. Process Flow Diagram

After the DRIE process, 1 μm of SiO_2 and 2 μm of Si remain under the silicon nitride absorber. The SiO_2 layer is removed with a standard 10:1 buffered oxide etch to expose the 2μm of top Si layer. The bolometer elements are then released from the DRIE mounting wafer by dissolving the mounting wax via a combination of solvents. During this process, each bolometer is separated from all the other corresponding neighbors on the wafer. A thorough cleaning of each bolometer follows this demounting process and each device is recoated with an acid resistant wax on top of the absorbing elements to complete the final wet etch process. An mixture of hydrofluoric acid, nitride acid and deionized water is used to remove the final 2μm of top Si layer while the wax protects the metalizations, nitride web structure and Ge thermistor. After the Si is etched, the device is rinsed thoroughly. To complete the formation of the bolometer, the acid resistant wax is removed via a combination of solvents used to dissolve the wax and clean the surface.

Fig. 3(h) shows the final detector after releasing and cleaning, and prior to packaging. After the microlithographic process is complete, the detector die is mounted in a BeCu housing that provides a thermal, electrical, mechanical and

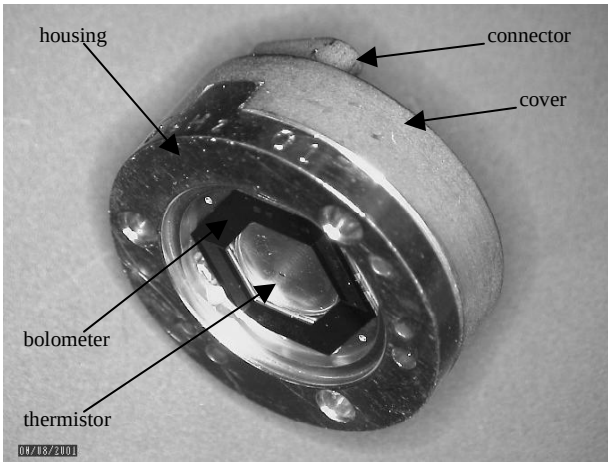

Figure 4 SWB Module

optical interface to the focal plane. The finished detector, shown in Fig. 4. is now ready for evaluation.

5. CHARACTERIZATION

5.1 Qualification

The HFI Bolometer Qualification Testing program is still in progress, but has matured sufficiently for us to know that the detectors are extremely robust. Qualification tests are performed on devices which have completed flight Acceptance Testing but which will not be used as flight deliverables. Twelve (12) detector modules, including, 6 SWB modules (6 bolometers) and 6 PSB modules (12 bolometers), are taken as a representative sampling. Acceptance Performance Tests will ultimately be repeated on all devices and the results will be evaluated for a Qualification report. The simple construction of the detectors allows us to qualify the entire assembly as a hybrid. The number of cryogenic thermal cycles for Qualification, 80, was chosen based on the estimates from various of our collaborators, indicating that the total number of cycles to cryogenic temperatures likely to be experienced by the Flight devices is ~25. The choice of cycling to a low temperature of ~90 K (LN2), rather than to the operating temperature of 100 mK or to 4.2 K (LHe), is based upon experience with similar devices which indicates that most failures occur during transition within this temperature range, and on general experience within the low temperature community that the majority of damage due to differential thermal contraction occurs within this temperature range. Additional detectors will undergo Accelerated Aging Test (1000 hours, 85% RH, 70 C). Resistance will be monitored continuously. We have determined that the elevated temperature is not detrimental, however, we will be able to set limits on exposure to elevated humidity and take steps to control it.

5.2 Vibration and Thermal Testing

Because the full suite of electrical and optical testing must be done at the detector operating temperature of 100 mK, and is thus expensive, each detector is first subjected to several Acceptance Tests to ensure that it will not subsequently fail. The impedance of the detector at room temperature is dominated by the impedance of the electrical leads and is thus a good measure, via the Weidemann-Franz law, of the thermal conductivity in operation. This impedance, as well as the impedance of test strips on the Si frame that give a measure of the leads and absorber metalizations, are all measured to confirm that they fall within specification.

The detectors are vibration tested using special fixturing that holds up to 24 bolometers per test run in a hermetic volume, opened only under controlled conditions. The vibration tests are preformed at JPL, and the detector impedance is monitored before and after, in addition to a visual inspection. The detectors are thermally cycled using a LN2 cryogen

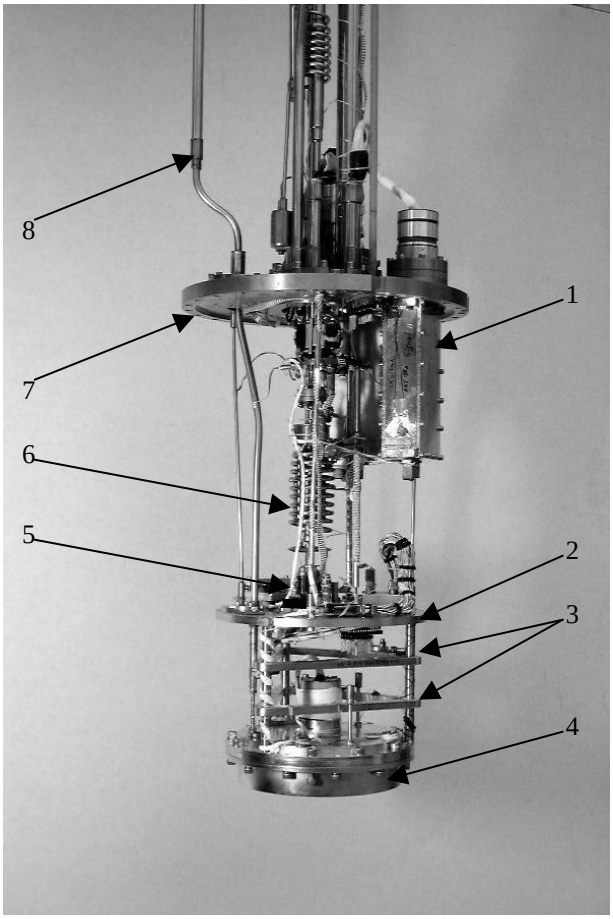

Figure 5 100 mK Test Bed: 1) JFET box; 2) 100 mK cold plate; 3) passive thermal filter stages; 4) evacuated sample can; 5) $^{3}He/^{4}He$ mixing chamber; 6) heat exchanger; 7) indium vacuum to LHe seal; 8) light pipe.

dewar that has been modified with a sample holder that can hold 16 bolometers, a variable flow heat exchanger, and heaters. Automated operation allows unattended thermal cycling between 330 K and 80 K. The resistance of each bolometer is recorded throughout the cycling intervals to a precision of 1%.

5.3 Electrical and Optical Testing

The detectors are characterized at 100 mK in a testbed built into an Oxford Instruments Kelvinox-25 ^{3}He/^{4}He dilution refrigerator. The test facility is capable of testing up to 21 bolometers per run. All channels have demonstrated intrinsic electronic noise <6nV/√Hz over the frequency range 0.010 to 25Hz, and individual bolometers delivered for use in the flight program have been measured to have <12nV/√Hz intrinsic noise under biased conditions in the absence of illumination. The thermal stability required for bolometer intrinsic noise determination is 40 nK/√Hz from 0.016 to 25 Hz. This is implemented via passive thermal design and active feedback using high resolution thermometry. A four stage structure provides passive thermal filtering. Active control of a stage distributes the thermal noise power density over a wider bandwidth and modulation of the isolated stage where the detectors are mounted is reduced. A full description of the testbed is given in Holmes et al. (this volume)[2].

6. DEVICE PERFOMANCE

Many of the CQM (prototype) detectors have already been tested, and testing of PFM (flight) devices will soon begin. An important test of our process is the total measured heat capacity of the device. Because of the relatively large surface areas of the devices and the stringent requirements on the heat capacity, the device performance can easily be degraded by small amounts of residues that are left on the device after processing. These can take the form of unetched Si remnants on the absorber web or, more difficult to see, of residues from the various waxes and ion and wet etching processes that are used in the fabrication.

We have measured heat capacities as a function of the absorber area in a variety of CQM devices, as shown Fig. 6. The heat capacities vary between 0.96pJ/K and 1.92pJ/K for 100GHz bolometers, between 0.24pJ/k and 3.03 for 143GHz, between 0.30pJ/K and 1.90pJ/k for 217GHz, and between 0.23pJ/K and 2.15pJ/K for 353 GHz devices.

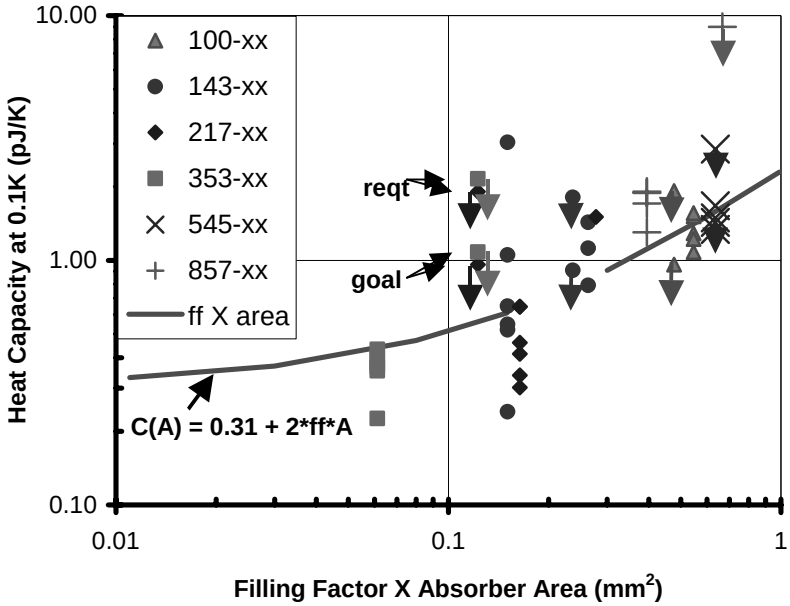

Figure 6. The measured heat capacity at 100 mK as a function of the total surface area (filling factor x absorber area) of the detector. The data come from tests of engineering model prototype. The required heat capacities are positioned to reflect the design of the flight model devices, which have different surface area from the prototype devices in some cases. The goal is to produce detectors with no more than half of the heat capacity allowed by the requirement.

The results to date indicate that there is an anomalous component of heat capacity that is scaling with the detector area, but that it is at an acceptably low level to yield a high fraction of detectors that meet the flight requirements. Since these results were obtained, we have made improvements to the details of the process which result in fewer visible residues on the detectors [5,6].

The thermal conductivity of the electrical leads is related by the Wiedemann-Franz law to their electrical conductivity. The thermal conductivity at 100 mK is correlated with the electrical conductivity at room temperature, as shown in Fig 7. This correlation allows for early screening between room temperature resistance of the electrical leads and the thermal conductivity at ~ 100 mK. This relationship allows for early screening of the detectors based on a simple room temperature measurement. In addition, the data show that the contribution to the thermal conductivity from the Si_3N_4 legs is negligible in comparison with the design values of the thermal conductivities, which are > 100 pW/K

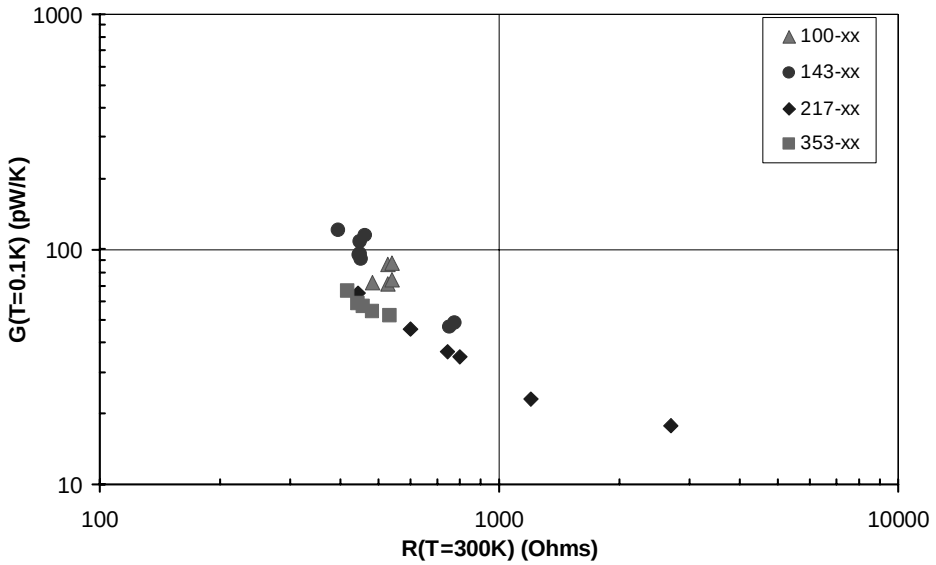

Figure 7. The measured thermal conductivity at 100 mK as a function of the measured room temperature impedance of the bolometer

7. SUMMARY

We have developed and are in the process of fabricating Si_3N_4 micromesh bolometers designed for the High Frequency Instrument on Planck. The process that we have developed reliably produces detectors that meet all of the requirements for Planck. We are near to completing the testing of the CQM model detectors, and are scheduled to complete fabrication of the PFM model detectors in 2002, and to complete testing and delivery of these detectors in 2003.

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REFERENCES

1. W. C. Jones, R. Bhatia, J. J. Bock, and A. E. Lange, “Polarization sensitive bolometers”, these proceedings
2. W. Holmes, J. J. Bock, L. Hustead, T. Koch, J. L. Mulder, C. Paine, A. D. Turner, L. Wild, and M. Yun, “ Performance measurements of bolometers for the Planck high frequency instruments”, these proceedings
3. J. Bhardwaj and H. Ashraf, “Advanced silicon etching using high density plasmas”, Proc. Micromachining and Microfab. Pro. Tech., SPIE, 2639, 224(1995)

4. A. M. Hynes, H. Ashraf, J. K. Bhardwaj, J. Hopkins, I. Johnston, and J. N. Shepherd, “Recent advances in silicon etching for MEMS using ASE process”, Sensors and Actuators, 74, 13(1999)
5. P. D. Mauskopf, J. J. Bock, H. Del Castillo, W. L. Holzapfel, and A. E. Lange, “Composite infrared bolometers with Si_3N_4 micromesh absorbers”, Applied Optics, 36(4). 765(1997)
6. J. J. Bock, J. Glenn, S. M. Grannan, K. D. Irwin, A. E. Lange, H. G. Leduc, and A. D. Turner, “Silicon nitride micromesh bolometer arrays for SPIRE”, Pro. Adv. Tech. MMW, Radio, and Terahertz Telescopes, SPIE, 3357, 297(1998)
7. A. D. Turner, J. J Bock, J. W. Beeman, J. Glenn, P. C. Hargrave, V. V. Hristov, H. T. Nguyen, F. Rahman, S. Sethuraman, and A. L. Woodcraft, “Silicon nitride micromesh bolometer array for submillimeter astrophysics”, Appl. Optics, 40(28), 4921(2001)