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Module Implementation and Modulation Strategy for Sensorless Balancing in Modular Multilevel Converters

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***Abstract*—Modules with series and parallel connectivity add new features and operation modes to modular multilevel converters (MMCs). Compared to full- and half-bridges, the series/parallel modules allow sensorless module balancing and reduce conduction loss with the same semiconductor area. However, in high-voltage applications with limited switching rates, the sensorless operation of the series/parallel modules suffers from large charge-balancing currents. This paper introduces a series/parallel module variant with a small port inductor. The port inductor suppresses the charge-balancing current despite low switching rates. We also propose a carrier-based modulation framework and show the importance of the carrier assignment in terms of efficiency and balancing. The proposed module and the modulation method are verified on a lab setup with module switching rates down to 200 Hz. The module voltages are kept within a narrow band with the charge-balancing currents below 5% of the arm current. The experimental results show practicality and advantages of the new series/parallel modules in high-voltage MMC applications.**

***Index Terms*—Modular multilevel converter; module topology; sensorless balancing; modulation.**

I. Introduction

Modular multilevel converters (MMCs) have a unique position among voltage-source converter topologies for medium- and high-voltage applications due to their modularity, utilization of standard components, and excellent output quality [1]–[4]. During operation, however, it is crucial to keep the modules balanced.

The sort-plus-select method is commonly used for balancing [1], which requires a central controller to activate or deactivate the modules with outlier voltages. The scheduling procedure is usually executed near the switching rate to keep the capacitor voltages within a narrow band [5]. Thus, the complexity of the balancing algorithms and the communication bandwidth grow with the number of modules. The required high-bandwidth communication and galvanically isolated module monitoring increase the cost of MMCs [6], [7], especially for systems with many modules, e.g., in high-voltage direct current (HVDC) systems [8] or where the modules spread geographically, such as many smart grid applications [9]–[11].

In order to reduce the communication and computation complexity of module balancing in MMCs, efforts have been devoted to reducing [12], [13] or completely eliminating [14]–[22] the voltage measurements. The methods of Picas et al. and D'Arco et al. only measure the arm output voltage and estimate the capacitor voltages by strategically activating certain modules [12], [13]. Despite the reduced number of measurements, these methods may demand high-bandwidth arm voltage measurement because of the high effective switching rate. Alternatively, some sensorless balancing methods are based on budgeting the in- and outflowing charge of the modules, which requires perfect knowledge of the load current [14], [18], [19], [22]. Other sensorless methods rotate the module switching states within a load cycle [16], [17], [21], [23]. Due to component manufacturing tolerances, jitter, and current measurement errors, these sensorless balancing methods cannot guarantee stable operation [6], [24].

The difficulty of sensorless balancing widely owes to the MMC's limited connectivity between full-bridge (FB) or half-bridge (HB) modules. These modules are connected via single-port terminals and only allow series and bypass states. As such, module voltage measurements are necessary to clear any accumulated offsets. Several topology modifications were recently proposed to simplify the module balancing. For instance, Ilves et al. proposed a module that can parallel two embedded capacitors [23]. This topology halves the balancing complexity and reduces the capacitor stress. However, the parallel interconnection is only available within small groups of capacitors, and many voltage sensors are still required. Alternatively, the series/parallel module proposed in reference [25] features two-port interconnections (Fig. 1), which can extend the parallel connection through an entire arm. The dynamic alternation between the series and parallel connections introduces features known from switched-capacitor converters, which are common for sensorless energy transfer and balancing in low-voltage applications. In addition to the simplified balancing, the parallel connection distributes the arm current among the module storages and reduces the conduction loss therein. Since the parallel state does not practically change the output voltage of the arm, known modulation methods select it in lieu of the bypass states for the above benefits [26].

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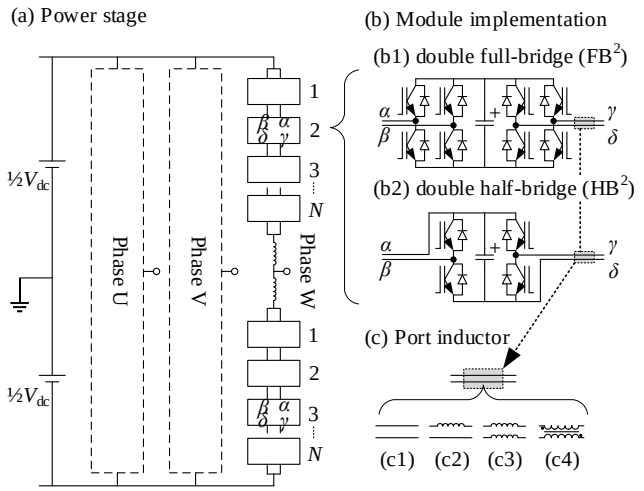

Fig. 1. Schematics of the proposed series/parallel modules. (a) MMC power stage. (b) Proposed modules. (c) Port inductor implementations.

Despite the advantages of the series/parallel modules, there are challenges to their practicality in high-voltage applications. First, at lower switching rates, the accumulated capacitor voltage differences are larger, which cause large equalization currents in the low-impedance charge-balancing loops. In fact, published studies of the series/parallel module concentrated on low- and medium-voltage applications where higher switching rates are possible, and where the high conduction loss in the module storages justifies the parallel interconnection [24], [25], [27]. For high-voltage applications with limited switching rates, a suitable series/parallel module variant is yet to be developed. Second, the canonical series/parallel module is designed for four-quadrant operations, which underutilizes the transistors when replacing the HB modules [28]–[31]. It is desired to have a two-quadrant module variant with fewer components but the same parallel connectivity. Finally, the series/parallel converter family needs an analytical framework for better understanding and optimizing the converter operations. The special parallel connection entails complex dynamics between the modules, which has not been fully exploited at a practical control level—available modulation strategies are either heuristic and potentially suboptimal [25], [26] or computationally expensive [32].

This paper presents two series/parallel module members and derives an equivalent circuit model to address the above problems. Each of the new modules uses the same semiconductor area, ratings, frequency range, and operation quadrants as their HB or FB equivalent. We add inductors to the module ports for suppressing the charge-balancing current. The port inductors have negligible magnetizing current and thus small footprint. The circuit model relates the charge-balancing currents and losses to the module switching rates and, particularly, reveals the importance of the carrier assignments. An optimal modulation scheme is further derived. In a down-scaled MMC setup, the proposed series/parallel module achieves reliable, sensorless balancing with moderate module switching rates (200–500 Hz). Due to the port inductors and the optimal carrier assignment, the charge-balancing currents are below 5% of the arm current, and the capacitor conduction loss is up to 50% lower than that of the conventional module equivalent.

II. Topology

A. Series/Parallel Module Implementation

Fig. 1 shows the double full-bridge (FB^2) and double half-bridge (HB^2) modules as well as their incorporation into the MMC macrotopology.

Double Full-Bridge (FB^2). The FB^2 module allows four-quadrant operations as a functional equivalent of the FB module. Similar to the canonical series/parallel module [25], the FB^2s can be paralleled via the two-terminal inter-connections for sensorless balancing. Different from the canonical series/parallel module, the FB^2 additionally contains a port inductor to suppress the peak charge-balancing current that occurs between the adjacent modules upon parallelization. Fig. 1(c) shows several implementations of the port inductor. This paper focuses on the differential-mode configuration [Fig. 1(c4)] because it does not impede the arm current while suppressing the charge-balancing current. Ideally, the differential-mode inductance L_{diff} and the module capacitance C should satisfy $L_{\text{diff}}C >> (2\pi f_{\text{sw}})^{-2}$, where f_{sw} is the module switching frequency. Note that the requirement on L_{diff} does not compromise the volume of the port inductor, because the port inductor is only magnetized by the charge-balancing current, which can be negligible. In the experiments, a setting of L_{diff} = 1.5 mH, C = 15 mF, f_{sw} = 200 Hz together with the proposed modulation scheme suppresses the charge-balancing currents to less than 5% of the arm current. The leakage inductance of the port inductors can also offset the discrete filter inductors. In this paper, we keep the arm inductors intact. We also do not extend the parallel connection across arms—the two-terminal module ports at the dc bus and the arms' ac output terminal are shorted.

Double Half-Bridge (HB^2). The HB^2 module allows two-quadrant operations as a functional equivalent of the HB module. The HB^2 is identical to the FB except that the former contains additional output terminals for parallel connectivity. The HB^2 is a topological reduction of the FB^2, at the cost of two operating quadrants. Similar to the FB^2, the HB^2's parallel connectivity ensures sensorless balancing and can benefit from the port inductor in the same way. The previous discussions of the port inductor apply equally. In Marquardt's MMC macro-topology, the HB^2 modules are connected equivalently to the FB^2 modules. For applications that do not intend parallel connection across different arms, the module terminals are shorted at the dc bus and the arms' ac output terminal.

B. Switching States and Operation Principle

Fig. 2 introduces the elementary switching states of the FB^2 and HB^2 modules. Since the parallel states are jointly formed by the adjacent modules, we define the switching states per interconnection instead of per module as suggested before [24], [26]:

- ***Series* (+/−)** connects two adjacent modules in positive or negative series, effectively increasing or decreasing the arm output voltage by one step;

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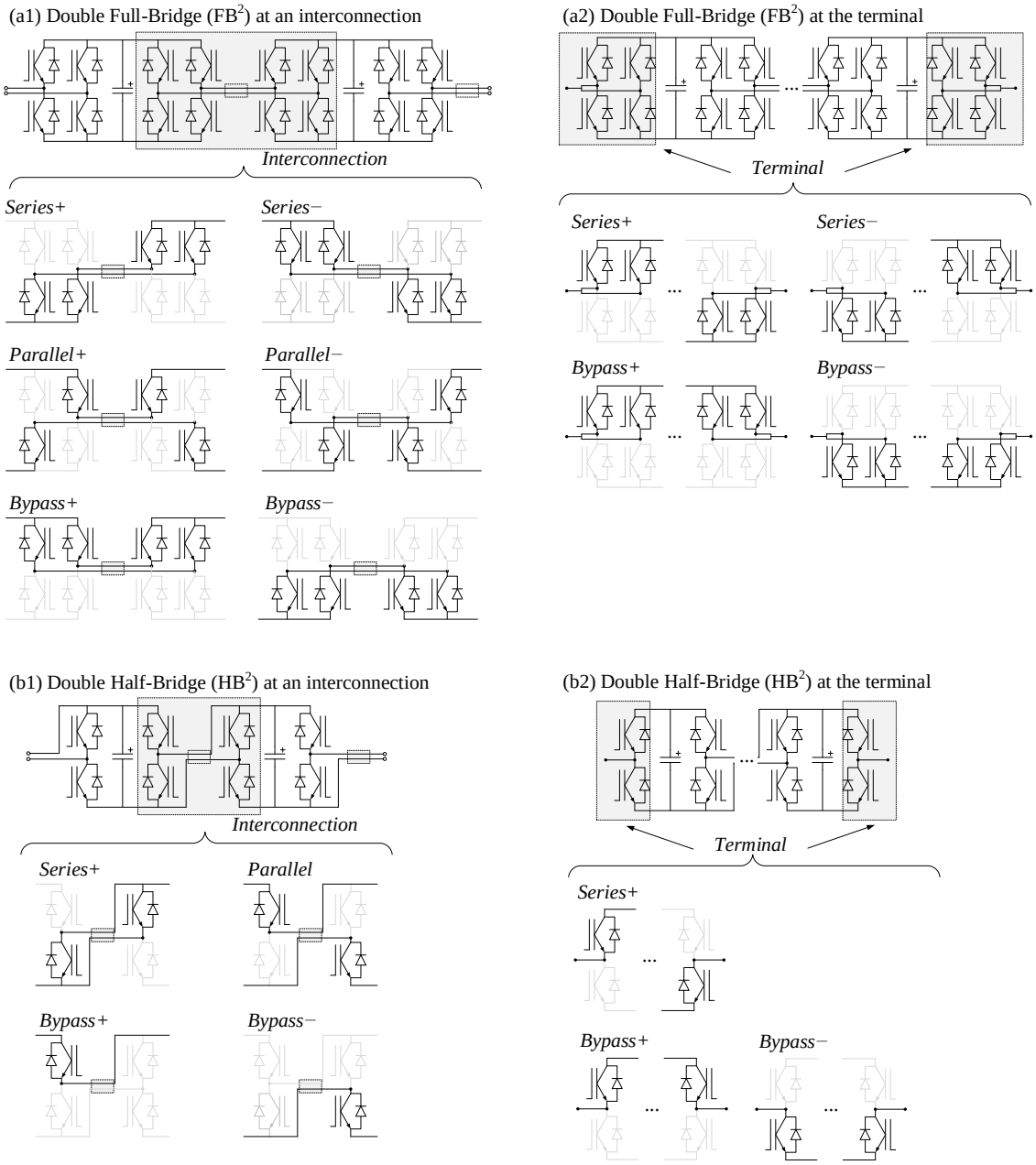

Fig. 2. Basic switching states of (a1–2) FB² module strings and (b1–2) HB² modules strings.

- ***Parallel* (+/−)** connects two adjacent modules in parallel. This state does not modify the arm output voltage. Different variations of the parallel state (for FB²) use complementary transistors but offer the same functionality;
- ***Bypass* (+/−)** connects the positive or negative dc buses of adjacent modules. It does not modify the arm output voltage.

For an arm with N modules, the defined switching states cover all $N-1$ interconnections but ignore the switches at the end of the arm. We combine these terminal switches into one virtual interconnection [26], which can be switched to either *Series*+/− to change the arm output voltage, or *Bypass*+/− (Fig. 2). Compared to the conventional FB/HB arms, the FB²/HB² arms' switching state identifiers are shifted by half a module but the relations to the arm output voltage are similar:

$$\begin{cases} v_{\text{out}} = n_{\text{out}} \cdot V_{\text{m}}, \\ n_{\text{out}} = n_{Series+} - n_{Series-}, \\ -N \le n_{\text{out}} \le N \quad \text{for FB}^2, \\ 0 \le n_{\text{out}} \le N \quad \text{for HB}^2, \end{cases} \tag{1}$$

where n_{out} is the arm output voltage level, $n_{Series+/-}$ is the number of *Series*+/− states, and V_{m} is the voltage of the module capacitors which are assumed balanced.

The dead-time setting of the FB² and HB² modules is not more complex than that of the FB or HB modules. First, the defined switching states always avoid short circuits within or across the modules. Second, dynamic shoot-through due to

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mismatched control timings can be prevented by a proper dead-time. Finally, during the dead time, the residue magnetizing current in the port inductors can always find free-wheeling paths via anti-parallel diodes and charge an adjacent capacitor.

III. Analysis

A. Module-Level Dynamics

Fig. 3 illustrates the circuit dynamics under various switching states. The bypass state is not considered since it can always be replaced by the parallel state with additional balancing and efficiency benefits [26]. The circuits and the equations in Fig. 3 apply equally to both the FB^2 and HB^2, with proper adjustments on the transistors' on-state resistance (to reflect the number of transistors in series) and the polarity of the series states.

Averaged dynamics at the interconnections. Denote $m_{k-1,k}$ as the duty cycle of the series state at the interconnection between the (k–1)th and kth modules ($1 < k < N$). On condition that $L_{\text{diff}}C >> (2\pi f_{\text{sw}})^{-2}$, the four cases in Fig. 3 can be averaged as [33]

$$\begin{cases} L_{\text{diff}}\dfrac{\mathrm{d}i_{k-1,k}}{\mathrm{d}t} = -4r_{\text{on}}i_{k-1,k} + \left(1-\left|m_{k-1,k}\right|\right)\left(v_{k-1}-v_k\right), \\ L_{\text{diff}}\dfrac{\mathrm{d}i_{k,k+1}}{\mathrm{d}t} = -4r_{\text{on}}i_{k,k+1} + \left(1-\left|m_{k,k+1}\right|\right)\left(v_k-v_{k+1}\right), \\ C\dfrac{\mathrm{d}v_k}{\mathrm{d}t} = \dfrac{i_{\text{arm}}}{2}\left(m_{k-1,k}+m_{k,k+1}\right) - \left(1-\left|m_{k,k+1}\right|\right)i_{k,k+1} \\ \qquad\qquad + \left(1-\left|m_{k-1,k}\right|\right)i_{k-1,k}, \end{cases} \tag{2}$$

where the variables are defined in Fig. 3. We ignore the influence of the capacitor equivalent series resistance (ESR) r_{cap} to simplify the current distribution. Defining

$$\begin{cases} L'_{k-1,k} \overset{\text{def}}{=} L_{\text{diff}} \Big/ \left(1-\left|m_{k-1,k}\right|\right)^2, \\ r'_{k-1,k} \overset{\text{def}}{=} 4r_{\text{on}} \Big/ \left(1-\left|m_{k-1,k}\right|\right)^2, \\ i'_{k-1,k} \overset{\text{def}}{=} \frac{1}{2}m_{k-1,k}i_{\text{arm}}, \\ \bar{i}_{k-1,k} \overset{\text{def}}{=} \left(1-\left|m_{k-1,k}\right|\right)i_{k-1,k}, \end{cases} \tag{3}$$

we rewrite Eq. (2) as

$$\begin{cases} L'_{k-1,k}\dfrac{\mathrm{d}\bar{i}_{k-1,k}}{\mathrm{d}t} = -r'_{k-1,k}\bar{i}_{k-1,k} + \left(v_{k-1}-v_k\right), \\ L'_{k,k+1}\dfrac{\mathrm{d}\bar{i}_{k,k+1}}{\mathrm{d}t} = -r'_{k,k+1}\bar{i}_{k,k+1} + \left(v_k-v_{k+1}\right), \\ C\dfrac{\mathrm{d}v_k}{\mathrm{d}t} = i'_{k-1,k} + i'_{k,k+1} + \bar{i}_{k-1,k} - \bar{i}_{k,k+1}. \end{cases} \tag{4}$$

Averaged dynamics at the terminal modules. The switches located at the arm terminals are defined as a joint switching site, which allows the series and bypass states. Defining $m_{N,1}$, $d\cdot(1 - m_{N,1})$ and $(1 - d)\cdot(1 - m_{N,1})$ as the duty cycles for *Series*+/–, *Bypass*+ and *Bypass*–, respectively, we obtain

$$\begin{cases} C\dfrac{\mathrm{d}v_1}{\mathrm{d}t} = i'_1 + i'_{1,2} - \bar{i}_{1,2}, \\ C\dfrac{\mathrm{d}v_N}{\mathrm{d}t} = i'_N + i'_{N-1,N} + \bar{i}_{N-1,N}, \\ i'_1 = \frac{1}{2}m_{N,1}i_{\text{arm}} + \frac{1}{2}\left(2d-1\right)\left(1-m_{N,1}\right)i_{\text{arm}}, \\ i'_N = \frac{1}{2}m_{N,1}i_{\text{arm}} + \frac{1}{2}\left(1-2d\right)\left(1-m_{N,1}\right)i_{\text{arm}}. \end{cases} \tag{5}$$

The equivalent circuit in Fig. 4 summarizes Eq. (4) and (5). The equivalent circuit does not model the arm output voltage but describes the relations among the load current, modulation indices, capacitor discharging rates, and the charge-balancing currents.

B. Module Balancing

Sensorless balancing. In the equivalent circuit, the load is distributed and modeled as the controlled current sources i'_1, i'_N, and $i'_{k-1,k}$ ($1 < k < N$) in parallel to the capacitors. Unequal modulation indices cause unevenly shared load and thus mismatched capacitor discharging rates. However, the time-averaged charge-balancing currents $\overline{i}_{k-1,k}$ ($1 < k < N$) can spontaneously occur to restore balance; no sensor is required. To avoid unnecessary charge-balancing currents, we assign the same modulation index for all switching sites and equally alternate between *Bypass*+ and *Bypass*– at the terminal switching site, i.e.,

$$d = \frac{1}{2}, m_{N,1} = m_{k-1,k} = n_{\text{out}}/N = m_{\text{ref}}\ \left(1<k<N\right). \tag{6}$$

As such, the capacitors are loaded equally: $i'_1 + i'_{1,2} = i'_{k-1,k} + i'_{k,k+1} = i'_{N-1,N} + i'_N = m_{\text{ref}}i_{\text{arm}}$. The charge-balancing currents are only driven by component tolerances and parameter drifts and, therefore, can be small.

Active balancing. One can also assign different modulation indices to actively adjust the discharging currents. Define $\overline{m}_k = (m_{k-1,k} + m_{k,k+1})/2$ ($1 < k < N$), $\overline{m}_1 = (m_{N,1} + m_{1,2})/2$ and $\overline{m}_N = (m_{N-1,N} + m_{N,1})/2$, and the capacitor current control equation follows from Eq. (3)–(4):

$$\begin{cases} C\dfrac{\mathrm{d}v_k}{\mathrm{d}t} = \overline{m}_k i_{\text{arm}} + \bar{i}_{k-1,k} - \bar{i}_{k,k+1}, \left(1<k<N\right), \\ C\dfrac{\mathrm{d}v_1}{\mathrm{d}t} = \overline{m}_1 i_{\text{arm}} - \bar{i}_{1,2}, C\dfrac{\mathrm{d}v_N}{\mathrm{d}t} = \overline{m}_N i_{\text{arm}} + \bar{i}_{N-1,1}. \end{cases} \tag{7}$$

The modulation indices can be solved from the desired list of $\overline{m}_k$'s in a closed form. This control mode is equivalent to the conventional closed-loop module balancing in HB or FB converters. The active balancing is not further discussed in this paper.

C. Conduction Losses

Transistors. The transistors in the proposed modules share the arm current in all switching conditions (Fig. 3). The transistor currents are not strictly equal since they differ by the charge-balancing currents $i_{k,k+1}$ ($1 \le k \le N - 1$). However, the port inductors and a properly designed modulation strategy (Section IV) can suppress the charge-balancing currents to levels far below the arm current as is shown in the measurements (< 5% i_{arm}, see Fig. 9 and Fig. 10). As a result, the individual transistor currents are close to ½i_{arm} and the conduction loss of a module is approximately

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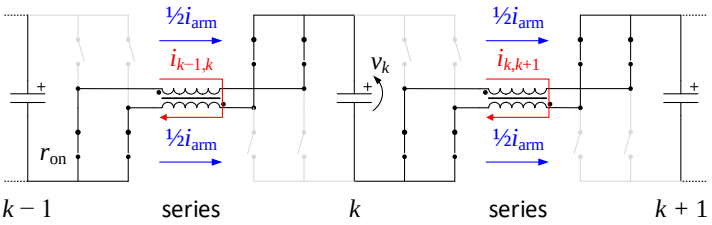
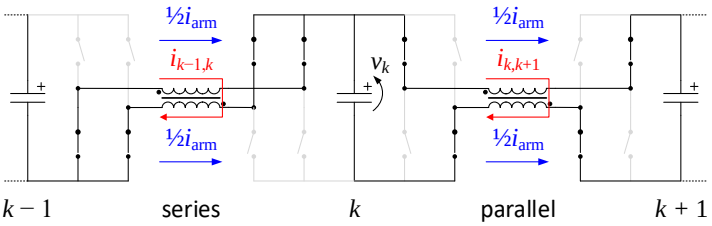
(a) case 1



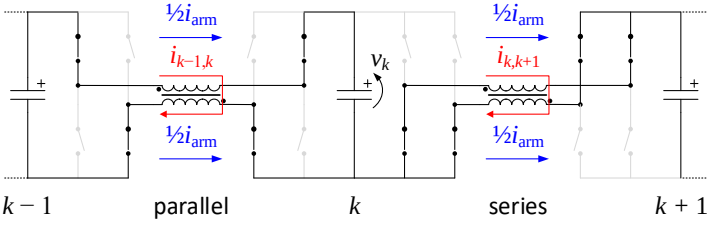
$$\begin{cases} L_{diff}\dfrac{di_{k-1,k}}{dt} = -4r_{on}i_{k-1,k}, \\ L_{diff}\dfrac{di_{k,k+1}}{dt} = -4r_{on}i_{k,k+1}, \\ C\dfrac{dv_k}{dt} = i_{arm}. \end{cases}$$

(b) case 2



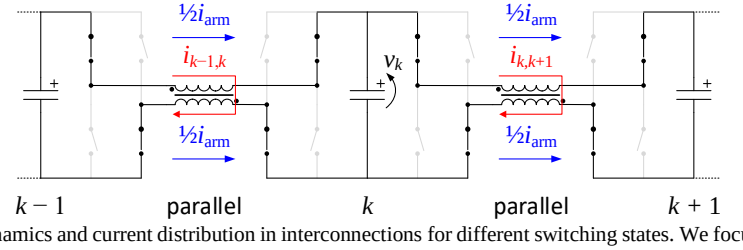
$$\begin{cases} L_{diff}\dfrac{di_{k-1,k}}{dt} = -4r_{on}i_{k-1,k}, \\ L_{diff}\dfrac{di_{k,k+1}}{dt} = -4r_{on}i_{k,k+1} + v_k - v_{k+1}, \\ C\dfrac{dv_k}{dt} = \dfrac{i_{arm}}{2} - i_{k,k+1}. \end{cases}$$

(c) case 3



$$\begin{cases} L_{diff}\dfrac{di_{k-1,k}}{dt} = -4r_{on}i_{k-1,k} + v_{k-1} - v_k, \\ L_{diff}\dfrac{di_{k,k+1}}{dt} = -4r_{on}i_{k,k+1}, \\ C\dfrac{dv_k}{dt} = \dfrac{i_{arm}}{2} + i_{k-1,k}. \end{cases}$$

(d) case 4



$$\begin{cases} L_{diff}\dfrac{di_{k-1,k}}{dt} = -4r_{on}i_{k-1,k} + v_{k-1} - v_k, \\ L_{diff}\dfrac{di_{k,k+1}}{dt} = -4r_{on}i_{k,k+1} + v_k - v_{k+1}, \\ C\dfrac{dv_k}{dt} = i_{k-1,k} - i_{k,k+1}. \end{cases}$$

Fig. 3. Dynamics and current distribution in interconnections for different switching states. We focus on the *k*th capacitor and the two differential-mode chokes aside.

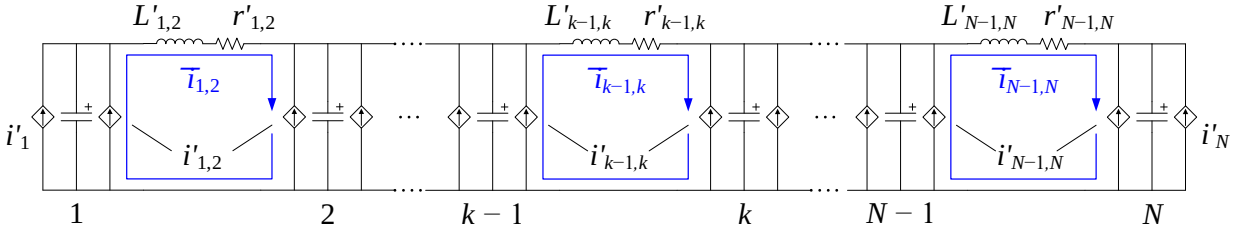


Fig. 4. Equivalent circuit of a series/parallel module string focusing on the charge-balancing currents. The circuit elements are defined in Eq.**Error! Reference source not found.**.

$$\begin{aligned} P_{\text{transistors},k} &= 4\left(\tfrac{1}{2}i_{arm}r_{on} + V_F\right)\tfrac{1}{2}i_{arm} \quad \left(\text{for FB}^2\right), \\ P_{\text{transistors},k} &= 2\left(\tfrac{1}{2}i_{arm}r_{on} + V_F\right)\tfrac{1}{2}i_{arm} \quad \left(\text{for HB}^2\right). \end{aligned} \tag{8}$$

Eq. (8) uses the piece-wise linear loss prediction model for insulated-gate bipolar transistors (IGBTs) [34], [35], where V_F is the forward voltage drop during conduction. If the FB^2 and the HB^2 modules are implemented with the same total semiconductor area as their conventional counterparts, i.e., r_{on}(FB^2/HB^2) = 2r_{on}(FB/HB) and V_F(FB^2/HB^2) = V_F(FB/HB) (assuming similar semiconductor technologies), their semiconductor conduction losses match those of the FB and HB modules, respectively.

Capacitors. The capacitor loss is averaged from the four switching cases in Fig. 3,

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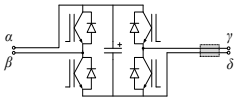
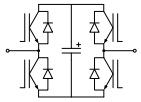
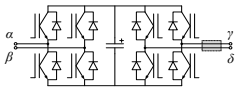
TABLE I
Comparison of the modules

	HB	HB^2	FB	FB^2
Topology				
Modulation range	$0 \le m \le 1$		$-1 \le m \le 1$	
Self-balancing	No	Yes	No	Yes
Switch count	2	4	4	8
Switch current rating	i_{arm}	$\approx \frac{1}{2} i_{\text{arm}}$	i_{arm}	$\approx \frac{1}{2} i_{\text{arm}}$
Switch on-state resistance†	$\frac{1}{2} r_{\text{on}}$	r_{on}	$\frac{1}{2} r_{\text{on}}$	r_{on}
Switch conduction loss	$\frac{1}{2} i^2_{\text{arm}} r_{\text{on}} + V_{\text{F}} i_{\text{arm}}$		$i^2_{\text{arm}} r_{\text{on}} + 2 V_{\text{F}} i_{\text{arm}}$	
Capacitor conduction loss	$i^2_{\text{arm}} r_{\text{cap}} m$	$\frac{1}{2} i^2_{\text{arm}} r_{\text{cap}} m \sim i^2_{\text{arm}} r_{\text{cap}} m$	$i^2_{\text{arm}} r_{\text{cap}} m$	$\frac{1}{2} i^2_{\text{arm}} r_{\text{cap}} m \sim i^2_{\text{arm}} r_{\text{cap}} m$
Port inductor magnetizing current	/	$\ll i_{\text{arm}}$	/	$\ll i_{\text{arm}}$
Component voltage rating	Module capacitor voltage (including the port inductors)			

† matching the total semiconductor amount between the equivalent pairs, i.e., HB vs. HB^2 and FB vs. FB^2.

$$P_{\text{capacitor},k} = i^2_{\text{arm}} r_{\text{cap}} \left(\frac{m_{\text{ref}}}{2} + \frac{t_{\text{case1}}}{2T_{\text{sw}}} \right), \tag{9}$$

where t_{case1} is the dwell time of Case 1 (Fig. 3) during a module-switching period T_{sw}. Variable t_{case1} contributes to the loss because in Case 1 the capacitor is conducting the entire arm current instead of sharing it with the adjacent modules. In the control, minimizing the capacitor loss amounts to avoiding concurred series states, or interleaving the switching patterns, of the adjacent interconnections. Depending on the modulation index, we have $0 \le t_{\text{case1}} \le m_{\text{ref}} T_{\text{sw}}$ and thus,

$$\tfrac{1}{2} i^2_{\text{arm}} r_{\text{cap}} m_{\text{ref}} \le P_{\text{capacitor},k} \le i^2_{\text{arm}} r_{\text{cap}} m_{\text{ref}} . \tag{10}$$

The upper limit $i^2_{\text{arm}} r_{\text{cap}} m_{\text{ref}}$ is exactly the capacitor loss of the FB or HB modules at the same modulation index. With an appropriate modulation strategy, the lower limit (i.e., 50% loss reduction) can be achieved [Fig. 9(b)]. TABLE I summarizes the key features of the mentioned modules.

IV. Modulation Design

A. Phase-Shifted Carrier Modulation

Both the FB^2 and HB^2 have the following features: *1)* the interconnections modify the arm output voltage in an independent, additive manner [Eq. (1)]; *2)* the modulation indices determine the capacitor discharging rates and should be equalized to minimize the charge-balancing current [Eq. (6)]; and *3)* the switching patterns of the adjacent interconnections should be interleaved to minimize the capacitor loss [Eq. (9)].

The phase-shift carrier (PSC) modulation framework [36] satisfies the first two features, and its redundancy in the carrier phase permutation allows various interleaving in the switching patterns. For an arm with N modules, the PSC framework contains N identical unipolar triangle carriers. Their phases differ by multiples of $\Delta\theta = 2\pi / N$. The carriers are assigned to the $N-1$ interconnections (denoted as $L_1, \ldots, L_{N-1}$) and the pair of arm terminals (denoted as L_N). The switching states are determined by the comparison between the carriers and the arm modulation reference m_{ref}. For FB^2 arms, $-1 \le m_{\text{ref}} \le 1$, and for HB^2 arms $0 \le m_{\text{ref}} \le 1$. Denote $0 \le C_k(t) \le 1$ as the carrier for interconnection L_k. The modulation rules for both the HB^2 and FB^2 can be unified as

$$\underset{k=1,\ldots,N-1}{\text{state}}\left(L_k\right) = \begin{cases} \textit{Series}+, & \text{if } m_{\text{ref}} \ge C_k , \\ \textit{Series}-, & \text{if } m_{\text{ref}} \le -C_k , \\ \textit{Parallel}+/-, & \text{if } -C_k < m_{\text{ref}} < C_k ; \end{cases} \tag{11}$$

and

$$\text{state}\left(L_N\right) = \begin{cases} \textit{Series}+, & \text{if } m_{\text{ref}} \ge C_N , \\ \textit{Series}-, & \text{if } m_{\text{ref}} \le -C_N , \\ \textit{Bypass}+/-, & \text{if } -C_N < m_{\text{ref}} < C_N . \end{cases} \tag{12}$$

In summary, the parallel switching state applies whenever the interconnection is not needed to increase or decrease the arm output voltage. *Bypass*+ and *Bypass*− must be alternatively activated to balance the discharging rates of the modules at the arm's terminals (i.e., $d = 1/2$ in Eq. (6)). Fig. 5 visualizes the proposed modulation scheme.

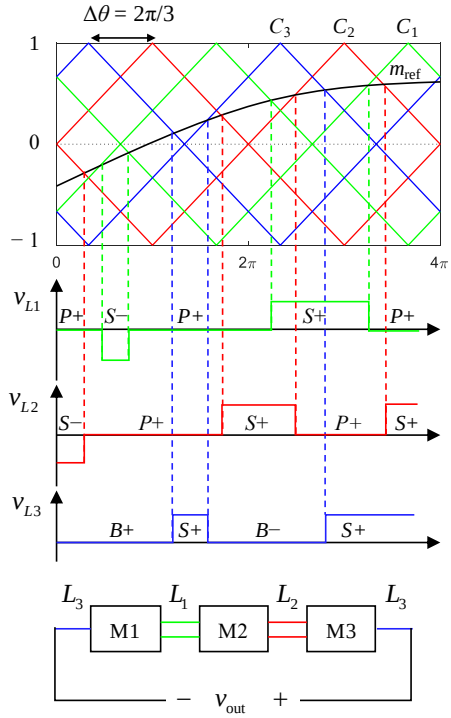


Fig. 5. A PSC-modulation process for a three-module FB^2 arm. Symbols "*B*", "*S*", and "*P*" represent *Bypass*, *Series*, and *Parallel* switching states, respectively. Here, $N = 3$ and L_3 refers to the terminal interconnection. The unipolar carriers are paired by their negative counterparts to visualize Eq. (11)–(12). The same diagram also applies to HB^2 arms if $m_{\text{ref}} \ge 0$.

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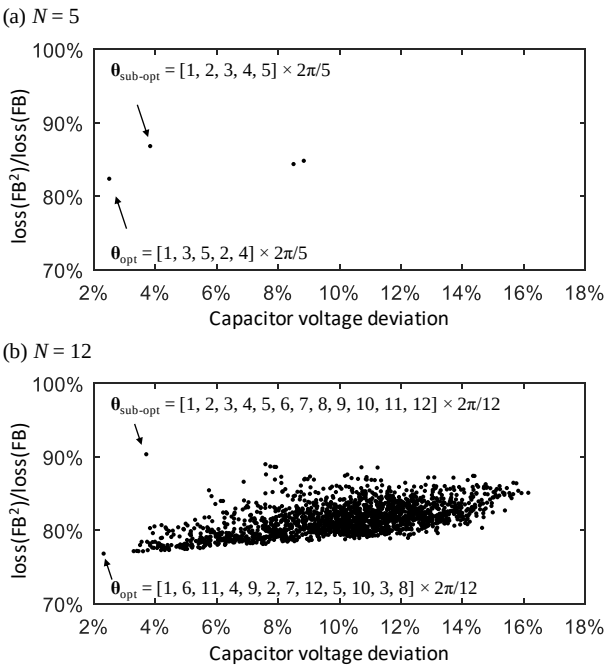

Fig. 6. Simulated performance of different carrier settings with (a) 5 FB^2 modules per arm and (b) 12 FB^2 modules per arm. The result of each carrier setting is represented by a dot. The capacitor losses are normalized against those of the equivalent FB arms (which is invariant to carrier permutations). For the case of $N = 5$, there are only 4 distinct results out of the 5! = 120 possible carrier permutations due to redundancy.

B. Carrier Sequence Optimization

Various carrier sequences in a series/parallel module arm produce different concurrences of series states in the adjacent interconnections and hence different capacitor loss per Eq. (9). Consider two configurations: *1)* modules 1–3 are paralleled and are connected to the 4th module by a series state; and *2)* modules 1–2 and 3–4 are respectively paralleled, and the two pairs are connected in a series state. Despite the same output voltage, configuration 2 produces less capacitor loss, better equalized discharging rates, and less subsequent charge-balancing currents. In general, switching configurations that have evenly paralleled groups are preferred [24]. In the PSC modulation scheme, the trivial carrier setting of $\boldsymbol{\theta}_{\text{sub-opt}} = [1, 2, 3, 4, \ldots] \times 2\pi/N$ more frequently results in situations such as configuration 1 because the carriers of adjacent inter-connections are often simultaneously larger or smaller than the modulation reference, creating concurrent series connections and uneven parallel groups. In comparison, the optimal setting of $N = 5$, $\boldsymbol{\theta}_{\text{opt}} = [1, 3, 5, 2, 4] \times 2\pi/5$ often creates similar parallel groups such as those of configuration 2. A general optimization rule is to separate the carriers of the adjacent interconnections, or

$$\boldsymbol{\theta}_{\text{opt}} = \arg\max_{\forall \theta_k} \left[\min_{1 \le k \le N-1} d\left(\theta_k, \theta_{k+1}\right) \right],$$

s.t.

$$\text{(1)}\ \ d\left(\theta_k, \theta_{k+1}\right) = \min\left\{ \left|\theta_k - \theta_{k+1}\right|, 2\pi - \left|\theta_k - \theta_{k+1}\right| \right\}, \quad (13)$$

$$\text{(2)}\ \ \theta_i \neq \theta_j \qquad \left(\forall i, j\right),$$

$$\text{(3)}\ \ \theta_k \in \left\{ \tfrac{2\pi}{N} \times 0, \tfrac{2\pi}{N} \times 1, \ldots, \tfrac{2\pi}{N} \times \left(N-1\right) \right\},$$

where θ_k denotes the initial phase of the kth carrier, constraints (2) and (3) evenly shift the carriers and guarantee the best output quality. This optimization problem can be solved offline. Exhaustive search is appropriate for small numbers of modules (e.g., $N < 15$). For larger N, examining $O(N!)$ possible carrier permutations can be intractable. For the latter cases, the following formula shows fairly good performance:

$$\theta_k = \begin{cases} \frac{2\pi}{N} \times \left[\left(k \times (2n-1) + 1 \right) \bmod N \right], & \text{if } N = 4n \text{ or } 4n+2; \\ \frac{2\pi}{N} \times \left[\left(k \times (2n) + 1 \right) \bmod N \right], & \text{if } N = 4n+1; \\ \frac{2\pi}{N} \times \left[\left(k \times (2n+1) + 1 \right) \bmod N \right], & \text{if } N = 4n+3. \end{cases} \quad (14)$$

The key idea of Eq. (14) is to generate the carrier sequence by cycling a list of numbers [1, 2, 3, … N] with an integer pitch. Take $N = 5$ for example, a pitch of "1" leads to the trivial suboptimal solution $\boldsymbol{\theta}_{\text{sub-opt}} = [1, 2, 3, 4, 5] \times 2\pi/5$, and a pitch of "2" leads to the optimal solution $\boldsymbol{\theta}_{\text{opt}} = [1, 3, 5, 2, 4] \times 2\pi/5$. For an arm with N modules, the best pitch choice is near $N/2$, corresponding to the goal of separating the carriers of the adjacent interconnections. However, the pitch of $N/2$ might be invalid either because N is odd or because $N/2$ and N share a non-trivial common divisor, which leads to skipped numbers and thus incomplete permutation (e.g., using a pitch of "4" at $N = 8$). For these special cases, we find the valid pitch that is closest to $N/2$ as in Eq. (14). Finally, it is worth noting that the carrier sequences produced by fixed pitches account for only a subset of all permutations; however, this subset contains all carrier settings that creates matched switching patterns and load profiles on modules. Consequently, the proposed carrier settings optimally balance component stresses—it is under this context that Eq. (14) gives the best solutions.

Fig. 6 studies the simulated performance of all carrier permutations for $N = 5$ and $N = 12$. We apply a staircase modulation reference to traverse all switching patterns of any given carrier permutation. The capacitor losses and voltage deviations are compared, and both criterions are concurrently minimized by the carrier settings $\boldsymbol{\theta}_{\text{opt}}$ from Eq. (14). The trivial carrier settings $\boldsymbol{\theta}_{\text{sub-opt}}$ produce the largest capacitor losses in the studied cases. Experimental validations can be found in Fig. 9. We use the capacitor voltage deviation as one of the criterions because it reflects the amplitude of the charge-balancing currents.

Compared with the conventional PSC modulation in FB and HB converters, the proposed modulation method achieves equally good output quality at comparable switching rates since *1)* the carriers are uniformly phase-shifted and *2)* only one switching site is toggled per step change in the output voltage [25], [26], [36].

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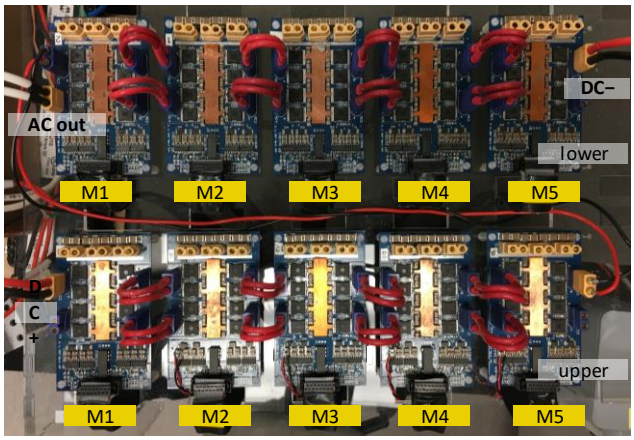

Fig. 7. The lab setup. The same setup can be reconfigured into either FB^2 or FB during operation.

V. Experimental Results

A. Setup

We implemented three module topologies, namely FB, FB^2 without port inductors, and FB^2 with differential-mode port inductors, in a single-phase, down-scaled MMC setup with five modules per arm. Each module contains a 15-mF electrolytic capacitor for main energy storage and some ceramic capacitors (1 mF in total) to assist the switching transients. As such, each module has a unit capacitance constant of $\tau_c = ½\ 2N\ CV_{mdl}^2/S =$ 115 ms, defined as the ratio between the total stored capacitor energy and the rated power [37]. The module contains eight identical transistors, each with $r_{on} = 0.4$ mΩ (IPT004N03L, Infineon Technologies). Each port inductor is implemented with a differential-mode choke (1.5 mH, B82727E6403A40, EPCOS / TDK). The chokes have a high common-mode current rating (>30 A) for conducting the arm current but a small magnetic core since the differential-mode current (i.e., the charge-balancing current) is small. TABLE II lists the implementation details. The HB^2 is not separately evaluated because its experimental behaviors coincide with the FB^2 under unipolar modulations.

The setup is controlled and modulated by an FPGA (40 MHz, sbRIO 9627, National Instruments, USA). As the same setup can represent all studied module topologies, the controller can swap the switching-state codebook to transit between the FB and the FB^2 configurations during operations. For the FB configuration, the controller operates the extra transistors in parallel. The modulation index is 0.9 to represent typical operating conditions.

B. Results

We use the standard deviation of the capacitor voltages to quantify the balancing performance. We use rms capacitor current and the port inductor's differential-mode current to quantify the capacitor loss and the additional conduction loss due to the charge-balancing process.

Operation at 500 Hz and sensorless balancing. Fig. 8 compares the MMC with FB modules and the two FB^2 configurations. All configurations are operated with the module switching rate of 500 Hz and the output quality are practically identical. In both Fig. 8(a) and (b), the setup was operated in the open-loop FB configuration before transited to the open-loop FB^2 configurations at $t = 0$. After the transition, both FB^2 configurations rapidly re-balance the capacitor voltages [Fig. 8(a2) and Fig. 8(b2)] and henceforth keep them within a narrow band. Because of the port inductors, the balancing process in Fig. 8(a2) is comparably slower and smoother. Both FB^2 module types reduce the peak and rms values of the capacitor currents compared to the FB configuration [Fig. 8(a3) and Fig. 8(b3)]. The charge-balancing current measured from the module interconnection is shown in Fig. 8(a3) and Fig. 8(b3), which is zero for the FB case and negligible for the FB^2 with port inductors. For the FB^2 without port inductors, the charge-balancing current presents large peak values and therefore additional loss on the semiconductors. Such charge-balancing current can be reduced at a higher switching rate, as is shown below.

Switching rates. Fig. 9 shows the influence of the switching rate on the rms charge-balancing currents and the rms capacitor currents as they respectively determine the additional transistor loss (compared to the conventional modules) and the capacitor loss. For FB^2 modules without port inductors, higher module switching rates suppress the charge-balancing current because the voltage spread of the modules is cleared more frequently by parallelization and does not reach high levels [25]. At a module switching rate of 5 kHz, for example, the rms charge-balancing current is less than 20% of the arm current, indicating less than 4% of the additional conduction loss.[1]

TABLE II
Circuit parameters of the experimental setup

Module		**FB**	**FB^2 + port inductor**	**FB^2**
Nominal power	S	100 VA		
Load frequency	f	50 Hz		
No. of modules per arm	N	5		
Module voltage	V_{mdl}	12 V		
Module capacitance	C	15 mF (main) + 1 mF (snubber)		
Unit capacitance constant [37]	τ_c	115 ms (115 kJ/MVA)		
No. of switches per module	N_{sw}	4	8	8
Switch on-state resistance	r_{on}	0.2 mΩ	0.4 mΩ	0.4 mΩ
Module switching frequency	f_{sw}	500 Hz		
Port inductor (differential-mode)	L_{diff}	–	1.5 mH	–

[1] The arm current and the charge-balancing current contribute independently to the ohmic loss, as can be derived from Fig. 3.

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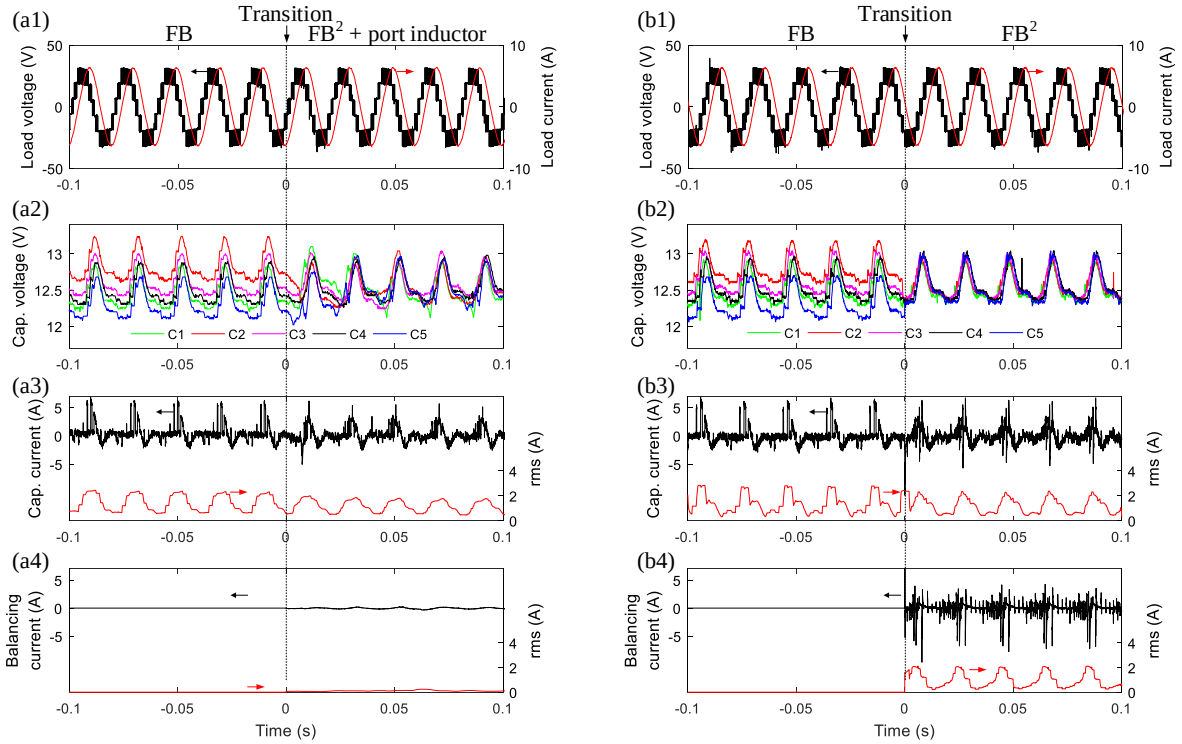

Fig. 8. Waveforms of (a) transition from the FB-mode into the FB^2-mode with port inductors, and (b) transition from the FB-mode into the FB^2-mode without port inductors. From top to bottom: the MMC output voltage and current, module capacitor voltages, module capacitor current, and charge-balancing current measured between modules 1 and 2. The rms value of the latter two measurements are shown. The "voltage spikes" in (b2) are noises due to measurement interferences.

For FB^2 modules with port inductors, the charge-balancing current slightly grows at higher switching rates, possibly because of the interaction between the module capacitor and the stray inductance of the differential-mode chokes or of magnetic loss. Nevertheless, the charge-balancing current is negligible compared to the arm current, and the variation is relatively minor.

Fig. 10 compares the charge-balancing currents in details, where the FB^2 configuration with port inductors [Fig. 10(a)] produces smaller charge-balancing currents that appear to change randomly and slowly, whereas the currents produced without port inductors [Fig. 10(b)] usually peaked when both the momentary modulation index and the arm current are large. In summary, under high switching frequencies or with port inductors, the charge-balancing currents can be small, indicating negligible additional loss and even current distribution among the transistors.

The current of the main capacitor is lower at higher switching rates for all studied cases because of the filtering effect of the snubber capacitors [Fig. 9(b)]. Compared to the conventional FB modules, both FB^2 configurations reduce the capacitor current by 20–30% or the conduction loss by 30–50% due to the load-sharing in parallel connections.

Carrier sequence. Two carrier sequences are compared in Fig. 9: the suboptimal one with $\boldsymbol{\theta}_{\text{sub-opt}} = [1, 2, 3, 4, 5] \times 2\pi/5$ (dashed lines in Fig. 9) and the optimal one with $\boldsymbol{\theta}_{\text{opt}} = [1, 3, 5, 2, 4] \times 2\pi/5$ obtained from Eq. (14) (solid lines in Fig. 9). At most switching rates, the optimized carrier setting reduces the

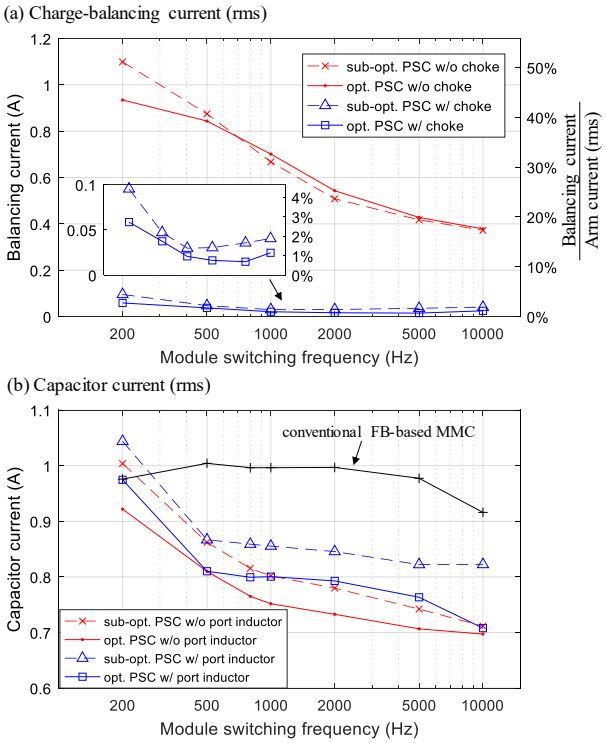

Fig. 9. (a) Charge-balancing currents under different switching frequencies. (b) Capacitor currents under different switching frequencies. All quantities are rms. The load is lowered to 65% of the nominal value by changing the load resistor.

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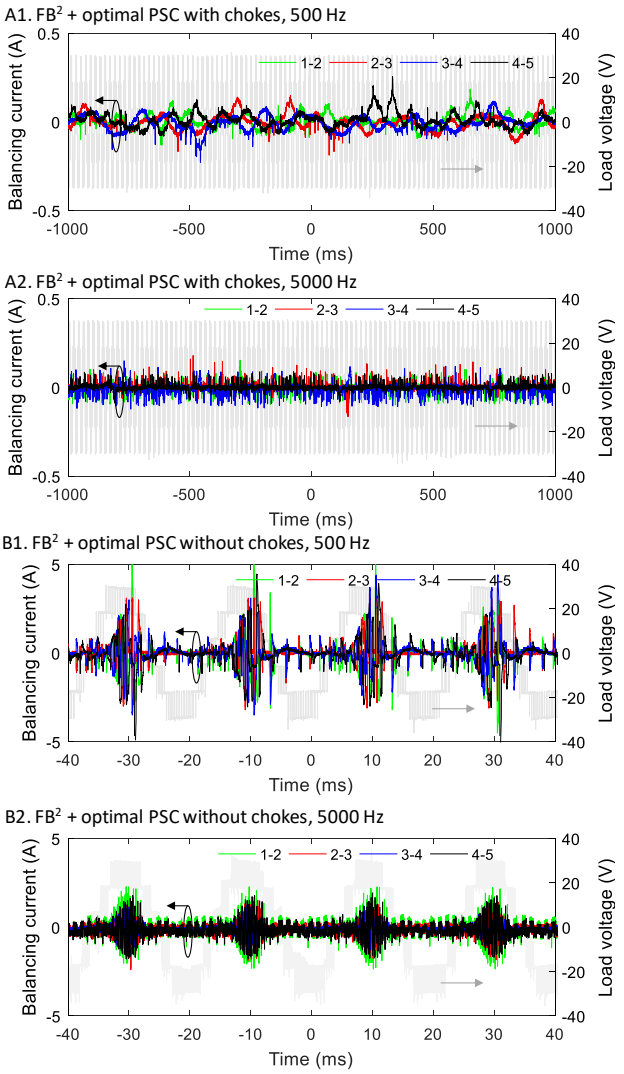

Fig. 10. Charge-balancing currents of all interconnections in the FB² configurations. The rms arm current of the studied arm is 2.15 A for all cases.

capacitor currents as predicted by Section IV. The optimized carrier does not significantly reduce the charge-balancing current but may help reduce the magnetic material if port inductors are used [Fig. 9(a)].

VI. Conclusion

We presented two module topologies for the series/parallel family as replacements of half-bridge (HB) and full-bridge (FB) modules in MMCs. Both modules use the same amount of semiconductor as the HB or FB equivalents but can reliably balance the modules in a sensorless manner. At low module switching rates (e.g., 200 Hz), small port inductors are recommended for suppressing the charge-balancing currents; at higher module switching rates (e.g., 10 kHz), port inductors become optional. We further present an optimal phase-shifted carrier modulation scheme to fully exploit the parallel interconnection, with which the proposed modules generate 30%–50% less capacitor loss compared to the HB or FB equivalents. The reduced module-balancing complexity, alleviated module storage stress, and capability of operating at low switching frequencies make the proposed series/parallel modules viable alternatives of the HB or FB in high-voltage applications (e.g., HVDC systems).

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