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Monolithically Integrated Multilayer Silicon Nitride-on-Silicon Waveguide Platforms for 3-D Photonic Circuits and Devices

This paper discusses multilayer platforms using silicon nitride and silicon waveguides. This technology allows 3-D photonic circuits to be created.

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ABSTRACT | In this paper, we review and provide additional details about our progress on multilayer silicon nitride (SiN)-on-silicon (Si) integrated photonic platforms. In these platforms, one or more SiN waveguide layers are monolithically integrated onto a Si photonic layer. This paper focuses on the development of three-layer platforms for the O- and SCL-bands for very large-scale photonic integrated circuits requiring hundreds or thousands of waveguide crossings. Low-loss interlayer transitions and ultralow-loss waveguide crossings have been demonstrated, along with bilevel and trilevel grating couplers for fiber-to-chip coupling. The SiN and Si passive devices have been monolithically integrated with high-efficiency optical modulators, photodetectors, and thermal tuners in a single photonic platform.

KEYWORDS | Silicon photonics

I. INTRODUCTION

Silicon (Si) integrated photonics has matured rapidly over the past decade with tremendous advances at the device, circuit, and microsystem levels. Research and development (R&D) and commercial foundries are now providing Si photonic fabrication services on 200- and 300-mm wafers [1]–[3]. In generic Si photonic platforms, the waveguides are formed in the topmost Si (i.e., the device) layer of a silicon-on-insulator (SOI) wafer; and P-and N-type implantations for modulators, and germanium (Ge) growth for photodetectors (PDs) are also available in this Si waveguide layer [4]–[8]. While this type of generic platform is useful and can already address many near-term applications of Si photonics (e.g., for single or few-wavelength transceivers), when considering very large-scale and more complex photonic integrated circuits (PICs), such as those for optical switch fabrics, chip-scale interconnects, transceivers for several dimensions of multiplexing, and computing, generic Si photonic platforms may become insufficient [9]–[13].

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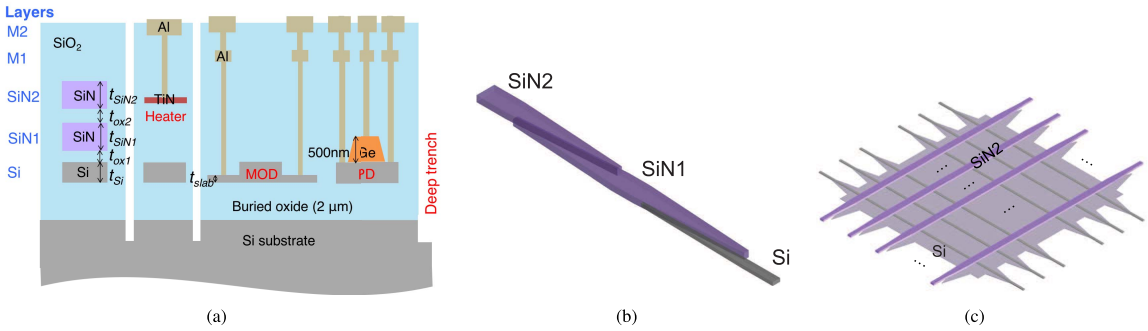


Fig. 1. ***(a) Schematic of the BEOL multilayer platform with full actives integration. (b) Illustration of interlayer transitions for transferring light between the Si, SiN1, and SiN2 layers. (c) Illustration of low-loss under/overpass crossings in the platform. (b) and (c) Reprinted with permission from [20], OSA.***

Very large-scale PICs, containing thousands of photonic devices, require low-loss and densely integrated on-chip optical routing networks that interconnect the devices. They also require energy-efficient optoelectronic devices, such as optical modulators, phase-shift tuners, and photodetectors, as well as passive waveguide devices with low losses, thermal sensitivity, and cross talk. The limitations of strictly 2-D Si integrated photonic platforms with a single Si waveguide layer become evident when we consider the problem of waveguide crossings. Due to the high index contrast of Si waveguides, the in-plane crossing loss of Si strip and rib waveguides is about 15–40 mdB per crossing [14]–[19]. If a PIC contains hundreds to thousands of crossings, the in-plane crossings can contribute of the order of 10 dB of optical loss and possibly untenable levels of crosstalk, prohibiting the implementation of very large-scale PICs. In microelectronics, the problem of on-chip connectivity between the myriad of transistors in the Si substrate is solved by using multiple metal interconnect levels. The metal layers also enable the realization of some passive elements, such as inductors and ground planes, for the electronic circuits.

Using microelectronics as an inspiration, we have been exploring the monolithic integration of additional passive waveguide layers on Si photonic platforms. As illustrated in Fig. 1, in a multilayer photonic platform, closely spaced waveguide layers enable the efficient transfer of light between layers, and the furthest spaced waveguide layers can be used for ultralow-loss waveguide crossings. Although it is possible to use amorphous Si for additional waveguide layers [21], [22], a particularly suitable material is silicon nitride (SiN).

In many ways, SiN is a better complementary metal–oxide–semiconductor (CMOS)-compatible passive optical material than Si. SiN is more suitable for high power handling, as it does not suffer from two-photon or free carrier absorption, and its $\chi^{(3)}$ is about 20 times lower than that of Si in the telecommunication wavelength range [23], [24]. Furthermore, the thermo–optic coefficient of SiN is about five times lower than that of Si [25], [26]. The refractive index of SiN ($n \approx 2$) is lower than Si ($n \approx 3.48$), such that SiN waveguides with SiO_2 cladding have lower sidewall roughness scattering losses and higher tolerance to dimensional variations. Some challenges of using SiN include an absorption peak near 1520 nm due to residual N–H bonds and film stresses if high temperature deposition is used. Nonetheless, the advantages of SiN over Si have led to demonstrations of SiN waveguides integrated on Si photonic platforms [27]–[32] or Si waveguides integrated onto SiN platforms [33], [34] to combine the passive optical routing layers in the SiN with active functionality in the Si. In the past year, several other major foundries, such as ST Microelectronics, CEA-Leti, AIM Photonics, and others, have announced Si photonic platforms that integrate a SiN waveguide layer onto a Si waveguide level [35]–[38]. Previously, we have also demonstrated the integration of a single SiN layer integrated onto Si in a passive photonic platform [32]. In recent years, we have been working on the monolithic integration of two layers of SiN and active photonic devices for 3-D PICs [20], [39], [40].

In this paper, we review our progress on multilayer SiN-on-Si photonic platforms, with a focus on trilayer platforms consisting of two SiN waveguide levels integrated atop a Si waveguide level. The platforms were fabricated on 200-mm diameter SOI wafers using 193- and 248-nm deep ultraviolet (DUV) photolithography. We present SiN-on-Si platforms for the O-band that used low-temperature deposition of SiN for back-end-of-line (BEOL) compatibility, and platforms for the SCL-bands that use high-temperature SiN deposition for front-end-of-line (FEOL) integration. Table 1 summarizes the devices that have been achieved in the trilayer platforms and their performance to date. These new devices complement the bilayer SiN-on-Si devices (such as polarization rotator splitters and grating couplers) that have been reported previously [32]. The paper describes in detail the design of the trilayer platforms and the devices therein. We begin with a brief description of the platform specification and fabrication process in Section II, followed by descriptions of the passive and active components that have been realized in

Table 1 Summary of Devices in Monolithically Integrated Trilayer SiN–SiN–Si Photonic Platforms

Device	Property
FEOL Platform (SCL bands) [20]	
Si-SiN interlayer transition	Insertion loss: < 107 mdB
SiN-SiN interlayer transition	Insertion loss: < 69 mdB
SiN2 overpass crossing	Insertion loss: < 2.6 mdB Crosstalk: < -56 dB
Si underpass crossing	Insertion loss and crosstalk lower than overpass crossing
BEOL Platform (O band) [39], [40]	
Si-SiN interlayer transition	Insertion loss: 0.13 dB
SiN-SiN interlayer transition	Insertion loss: 2.5 dB
SiN2 overpass crossing	Insertion loss: < 3.4 mdB Crosstalk: < -52 dB
Si underpass crossing	Insertion loss: < 3.1 mdB Crosstalk: < -58 dB
SiN-SiN bilevel grating coupler	Single-polarization (TE) Peak coupling efficiency: -3.5 dB 1-dB bandwidth: 53 nm
SiN-SiN-Si trilevel grating coupler	Polarization independent Peak coupling efficiency: -5.6 dB (TE), -5.5 dB (TM) 1-dB PDL bandwidth: 80 nm
TiN thermo-optic phase tuner	P_π = 14 mW
Optical modulator	Carrier depletion, U-shaped PN junctions DC $V_\pi L$: 0.26 - 0.46 V $\cdot$ cm Propagation loss: 12.5 dB/cm Electro-optic 3-dB bandwidth: > 10 GHz Microring and Mach-Zehnder modulators
Germanium photodetector	Responsivity: 0.85 A/W Dark current: 2 μA Opto-electronic 3-dB bandwidth: 29 GHz

TE: Transverse electric
TM: Transverse magnetic
PDL: Polarization dependent loss

Sections III and IV. Overall, the development of multilayer SiN-on-Si platforms is enabling a new generation of foundry-compatible, monolithically integrated 3-D PICs.

II. PLATFORM DESIGN AND FABRICATION

SiN waveguide layers can be formed on SOI using either low-pressure chemical vapor deposition (LPCVD) or plasma-enhanced chemical vapor deposition (PECVD). LPCVD is a FEOL high-temperature process requiring temperatures of about 800 °C, but it results in stoichiometric silicon nitride (Si_3N_4). PECVD can be carried out at temperatures < 400°C, and is thus BEOL compatible, but does not necessarily result in stoichiometric silicon nitride. Multilayer SiN-on-Si photonic platforms that incorporate one or two SiN layers on SOI have been demonstrated using both LPCVD and PECVD SiN [27]–[34], [39]. LPCVD SiN has fewer residual N–H bonds, which leads to lower optical absorption losses than PECVD SiN waveguides around a wavelength of 1520 nm [31], [32], [41]. As reported in [32], PECVD SiN waveguides with a height of 600 nm and width of 1 μm have propagation losses $>$8 dB/cm near 1520 nm, but decrease to 0.8 dB/cm at 1580 nm. Meanwhile, LPCVD SiN waveguides with a height of 400 nm and a width of 900 nm have losses $<$3 dB/cm near 1520 nm and 0.4 dB/cm at 1580 nm. In the O-band (between wavelengths of 1260 and 1360 nm), the waveguide loss of PECVD and LPCVD SiN are similar at around 0.3 dB/cm as presented in the the waveguide loss measurements in [31], [32]. The high-temperature requirements of LPCVD and the resultant thermally induced film stresses make the integration of multiple layers of LPCVD SiN more challenging.

Recently, we demonstrated two photonic platforms that monolithically integrate two SiN layers on SOI [20], [39]. The first is a BEOL platform [39], as illustrated in Fig. 1(a). It used PECVD SiN and was designed for the O-band with nominal thicknesses $t_{\mathrm{Si}} = 150$ nm, $t_{\mathrm{slab}} = 65$ nm, $t_{\mathrm{ox1}} = t_{\mathrm{ox2}} = 200$ nm, and $t_{\mathrm{SiN1}} = t_{\mathrm{SiN2}} = 450$ nm. The platform integrated Si depletion modulators, Ge photodetectors (PDs), and TiN thermo–optic tuners. The second is a FEOL platform [20], which is similar to Fig. 1(a) but with two distinctions. First, the FEOL platform was optimized for the SCL-bands, and therefore, used LPCVD SiN and a different set of nominal waveguide thicknesses: $t_{\mathrm{Si}} = 220$ nm, $t_{\mathrm{slab}} = 90$ nm, $t_{\mathrm{ox1}} = 250$ nm, $t_{\mathrm{ox2}} = 200$ nm, and $t_{\mathrm{SiN1}} = t_{\mathrm{SiN2}} = 400$ nm. Second, the demonstration did not yet include active device integration. High-quality passive device performance was the objective of this first FEOL platform demonstration, and active integration is in progress. As described in Section III, the waveguide thicknesses in both cases were chosen to enable low-loss interlayer transitions as well as low-loss waveguide crossings.

The fabrication process for the BEOL platform begins with Si waveguide formation, along with the Ge growth and implantations for modulators and PDs, as in a generic

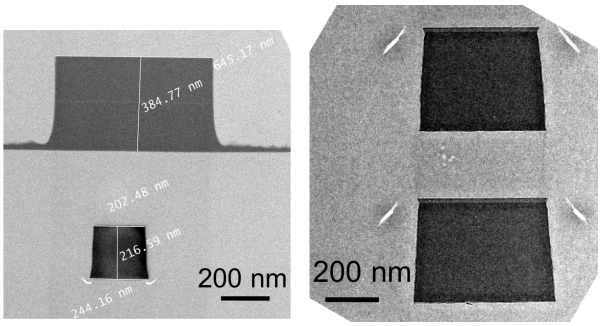


Fig. 2. *Cross-section transmission electron micrographs (XTEMs) from the fabricated FEOL platform showing (a) a SiN1 waveguide above a Si waveguide and (b) a SiN2 waveguide above a SiN1 waveguide. Reprinted with permission from [20], OSA.*

single-layer Si photonic platform. Then, SiN waveguides are formed using a series of deposition, etching, and chemical mechanical polishing (CMP) steps. Then, the metal vias and layers are formed. A layer of high resistivity metal [titanium nitride (TiN)] is also included to realize thin film heaters for thermo–optic tuning of SiN waveguides. A deep trench etch is applied to form the edge couplers and thermal isolation trenches.

The fabrication of a passive FEOL platform involves Si waveguide formation, SiN waveguide formation (LPCVD, lithography, etching, CMP), deep trench etching, and wafer dicing. Active integration of Ge PDs and dopant implantations would be carried out after the SiN waveguides are formed by etching windows in the SiO_2 cladding. The fabrication including active integration is ongoing at present. Fig. 2 shows cross-section transmission electron micrographs (XTEMs) of the waveguides in the FEOL platform. The SiN2 layer was not fully etched in some regions of the wafer, and the thicknesses measured in the XTEMs deviated from the nominal thicknesses, with $t_{\mathrm{Si}} = 217$ nm, $t_{\mathrm{ox1}} = 305$ nm, $t_{\mathrm{ox2}} = 245$ nm, and $t_{\mathrm{SiN1}} = t_{\mathrm{SiN2}} = 385$ nm. Nonetheless, as discussed in Section III, the FEOL platform exhibited low-loss passive devices.

III. WAVEGUIDES AND PASSIVE DEVICES

A. Waveguide Interlayer Transitions and Crossings

In our multilayer platforms, optical power is transferred between the layers using adiabatic tapers as illustrated in Fig. 1(b). Although gratings can also be used [30], adiabatic tapers provide low-loss and broadband interlayer transitions [31], [32], [42]. As shown in Fig. 1(c), the multiple layers also allow for overpass and underpass types of waveguide crossings, wherein the upper (lower) SiN (Si) waveguide can pass over (under) many Si (SiN) waveguides. In adiabatic interlayer transitions, a trade-off exists between the interlayer coupling efficiency and under/overpass crossing loss. A low-loss interlayer transition demands a close spacing between two waveguide layers, while a low-loss crossing demands a large separation between the waveguide layers. A photonic platform with three or more waveguide layers allows the separation between any two successive levels to be kept sufficiently small for low-loss transitions, while creating a large overall interlayer separation between the topmost and bottommost waveguides. Overpass/underpass types of crossings are preferred when the interlayer transition loss is lower than the crossing loss. This situation is most applicable to very large-scale PICs with many (hundreds or thousands) of crossings.

1) Simulated Results: The Si–SiN1 and SiN1–SiN2 transition designs are illustrated in Fig. 3(a) for the BEOL and FEOL platforms. The inputs and outputs of the transitions are single-mode waveguides, and blunt tips terminate the tapers. The transition lengths are chosen to realize low-loss, broadband optical coupling, as shown in Fig. 3(b). For the BEOL platform, over 1260–1360 nm, the simulated Si–SiN1 and SiN1–SiN2 transition losses are < 110 mdB (millidecibels) and < 30 mdB, respectively. For the FEOL platform, over 1480–1600 nm, the simulated Si–SiN1 and SiN1–SiN2 transition losses are < 13 mdB and < 35 mdB, respectively. The Si–SiN1 transition loss is higher in the O-band than the C-band because the Si waveguide mode is more confined, leading to higher scattering losses at the Si tip.

The waveguide crossing designs are shown in Fig. 3(c). A simple crossing design was implemented in the BEOL platform, where single-mode, fully etched waveguides in the SiN2(Si) layer passed over(under) the Si(SiN2) waveguides. Over 1260–1360 nm, the overpass and underpass losses are expected to be < 7 mdB and < 0.06 mdB, respectively [Fig. 3(d)]. The overpass loss is higher than the underpass loss because the Si waveguide mode is more confined than the SiN waveguide mode.

An improved crossing design was implemented in the FEOL platform. Wide SiN2 waveguides passed over Si rib waveguides with a contiguous partially etched Si slab. The Si slab reduced the index perturbation experienced by light in the SiN2 waveguide in an overpass, and the optical mode is more confined in the Si layer in a Si rib waveguide compared to a strip waveguide, which improves the underpass crossing loss. The SiN2 waveguide was chosen to be 1.5 μm wide and multimode to increase the optical confinement in the SiN2 waveguides for overpass crossings. Fig. 3(e) shows that the Si slab reduces the expected maximum overpass loss from 18 to 0.29 mdB, and the maximum underpass loss from 0.26 to < 0.04 mdB. Overall, the improved crossing design leads to submillidecibel overpass and underpass crossings across the SCL-bands. This design may also be applied to the BEOL platform.

2) Measurements: We used the cutback method to measure the waveguide crossing and interlayer transition losses. Due to the low losses, the determination of optical

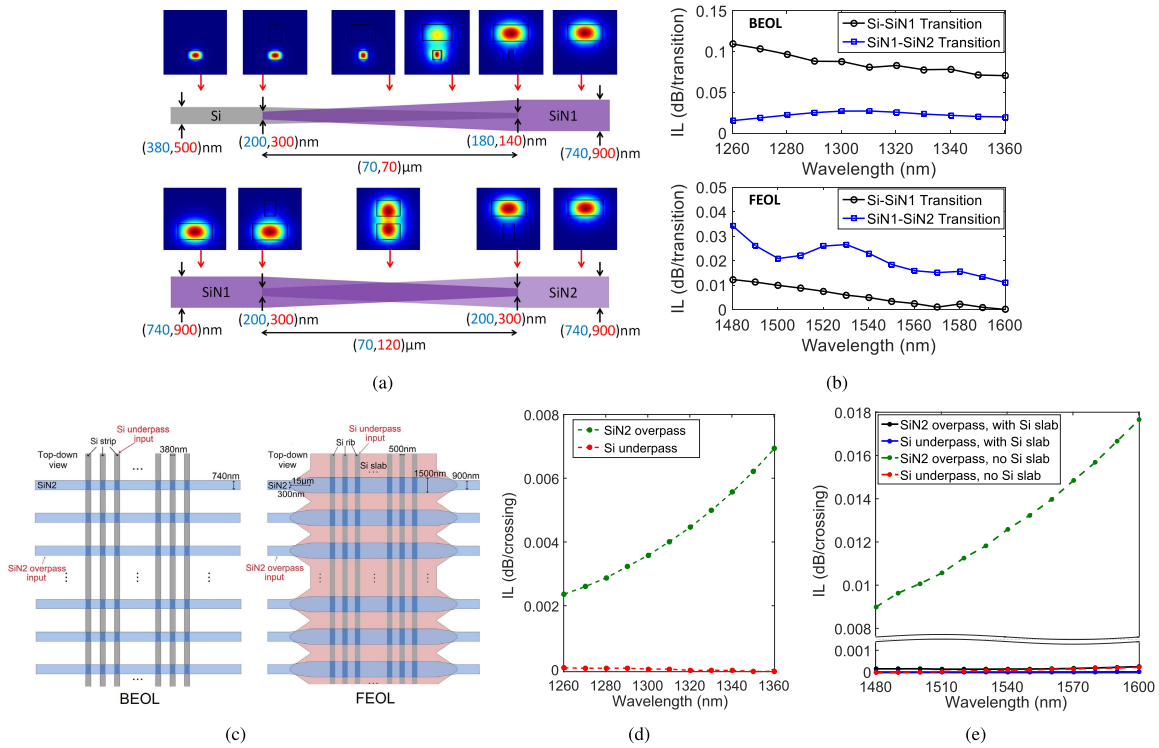


Fig. 3. ***(a) Schematics of the interlayer transitions. Dimensions listed in blue (red) refer to the BEOL (FEOL) platform. TE-polarized mode profiles are shown at several locations along the transitions at a wavelength of 1550 nm for the FEOL design. (b) Simulated interlayer transition losses for the BEOL and FEOL platforms. (c) Schematics of waveguide crossings demonstrated in the BEOL and FEOL platforms. (d) and (e) Simulated crossing losses for the (d) BEOL and (e) FEOL platforms. In (e), the FEOL crossing loss is simulated with and without the partially etched Si slab showing a large reduction in the overpass loss with the Si slab. The transition and crossing loss simulations are for the TE polarization and used the 3-D finite difference time domain (FDTD) method. (a) Adapted from [20]. The FEOL transition simulations in (b), FEOL crossing schematic in (c), and (e) reprinted with permission from [20], OSA.***

losses requires hundreds or in excess of a thousand crossings or transitions. The test structures were edge coupled to ensure broadband input/output coupling. Here, we summarize the transverse electric (TE)-polarization performance, and the transverse magnetic (TM) polarization results were reported in [20] and [39].

Fig. 4 shows the measured crossing loss in the BEOL platform with the waveguide propagation loss removed. Over 1262–1360 nm, the overpass crossing loss was $< 3.4 \pm 0.9$ mdB, the underpass loss was $< 3.1 \pm 1.2$ mdB, and the crosstalk was < -52 dB and < -58 dB, for the overpass and underpass crossings, respectively. Simulations indicate that the discrepancy between the measured [Fig. 4(a)] and simulated [Fig. 3(d)] overpass losses can be explained by a roughly 15% larger than designed spacing between the Si and SiN2 layers. Due to nonoptimal planarization between the waveguide layers [39], the observed SiN1–SiN2 transition loss was high and was about 2.5 dB at 1310 nm. The measured Si–SiN1 transition loss, 0.13 dB at 1310 nm, was closer to the simulations.

The FEOL platform wafer had greatly improved planarization, so very low-loss transitions were demonstrated. Fig. 5(a) shows that the measured Si–SiN1, SiN1–SiN2, and trilayer (Si–SiN1–SiN2) interlayer transition losses were < 107 mdB, < 69 mdB, and < 150 mdB, respectively, across 1480–1620 nm. The SiN1–SiN2 transition loss measurements agreed well with the simulations in Fig. 3(b) with a moderate discrepancy near 1520 nm, due to the extra absorption loss in the SiN waveguides, an effect not modeled by the simulations. The measured Si–SiN1 transition losses were low but substantially larger than simulated, which may be due to waveguide scattering loss and larger than designed Si tip widths.

Fig. 5(b) shows the measured overpass crossing losses in the FEOL platform without de-embedding the waveguide losses. The accuracy of the linear fits for the cutback measurements [Fig. 5(c)] was limited by alignment error and Fabry–Perot oscillations from facet reflections. Accounting for these effects, the overpass loss for a 1.5-μm SiN2 width was < 2.6 mdB with a 90% confidence interval over 1480–1620 nm, and was limited by the loss of the 5–7-μm waveguide length between consecutive crossings, which would explain the difference between the measurements and simulations in Fig. 3(e). Fig. 5(d) shows the extracted crosstalk of the crossing was < -56 dB using the procedure described in [20]. These results show it is possible to

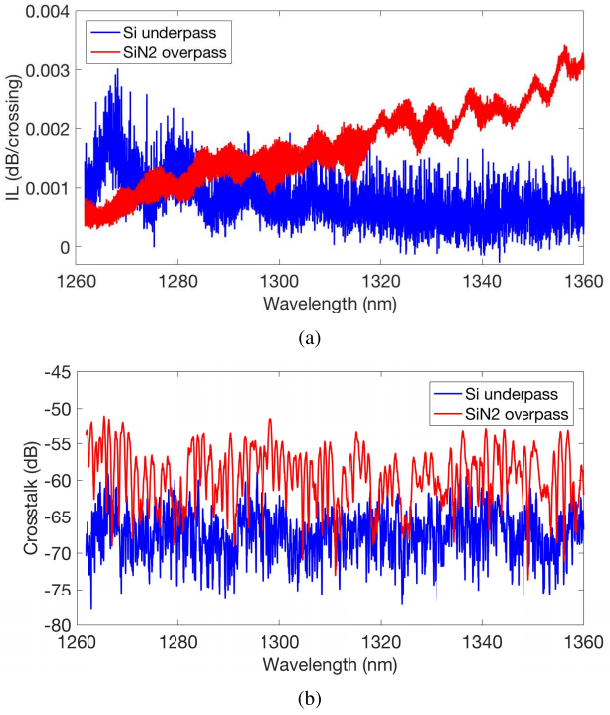


Fig. 4. ***BEOL platform waveguide crossing measurements showing overpass and underpass (a) losses and (b) crosstalk for the TE polarization, as taken from [39].***

achieve ultralow-loss interlayer transitions and crossings in multilayer SiN-on-Si platforms.

The FEOL platform also exhibited reasonable interlayer transition and crossing losses in the O-band, but since the thicknesses and device designs were optimized for the C-band, the transition losses were higher. The measured trilayer transition loss in Fig. 6(a) was < 560 mdB over 1262–1360 nm, about 0.4 dB higher than the SCL-band results. The loss was primarily due to the Si–SiN1 transition, and the measured loss per transition at 1310 nm was 302 and 25 mdB for the Si–SiN1 and SiN1–SiN2 transitions, respectively. In Fig. 6(b) and (c), the measured overpass loss is < 0.6 mdB with a 90% confidence interval and crossing crosstalk is < -53 dB. The crossing loss in the O-band is lower than the C-band due to higher optical confinement for the shorter wavelengths.

B. Multilevel Grating Couplers

Multilevel fiber-to-chip grating couplers (GCs) with composite features that exist in the SiN and Si layers can be realized in the multilayer platforms. SiN-on-Si and Si-on-Si GCs have been reported in [37], [43], and [44]. The main advantage of multilevel GCs compared to conventional GCs defined in one layer of material is that a high peak coupling efficiency η around -1 to -2 dB can be achieved without any back reflectors while maintaining extremely broad bandwidths. For example, Si-on-Si GCs have achieved $\eta = -1.2$ dB with a 1-dB bandwidth of $\Delta\lambda_{1\mathrm{dB}} = 78$ nm in the O-band [44]. Intuitively, the multilayer GCs effectively create a blazed grating profile that efficiently and preferentially radiates in-plane light on the chip upward, rather than downward into the substrate.

Table 2 summarizes University of Toronto's work on multilayer GCs in several SiN-on-Si platforms. The GCs interfaced with standard single-mode fibers, and single-polarization GCs worked for TE-polarized light. Our apodized bilevel SiN-on-Si GC in [43] exhibited $\eta = -1.3$ dB with $\Delta\lambda_{1\mathrm{dB}} = 80$ nm in the C-band. The unapodized version of the GC achieved a broader bandwidth of $\Delta\lambda_{1\mathrm{dB}} = 110$ nm with a slightly higher insertion loss of $\eta = -2.3$ dB in the C-band [32]. More recently, we demonstrated an O-band bilevel SiN-on-Si GC in a platform fabricated at CEA-Leti with $\eta = -2.1$ dB with $\Delta\lambda_{1\mathrm{dB}} = 72$ nm [37]. The design of these multilevel GCs is more computationally intensive than single-level GCs, since a greater number of geometric parameters needs to be optimized. Nonetheless, we have developed an automated design methodology for multilevel GCs based on solving a series of optimization problems that search for the solutions within the fabrication constraints [37], [45]. We have found that a major contributor to the variation in the spectral characteristics of multilevel GCs is the interlayer spacing, rather than the alignment between the layers or feature sizes [45].

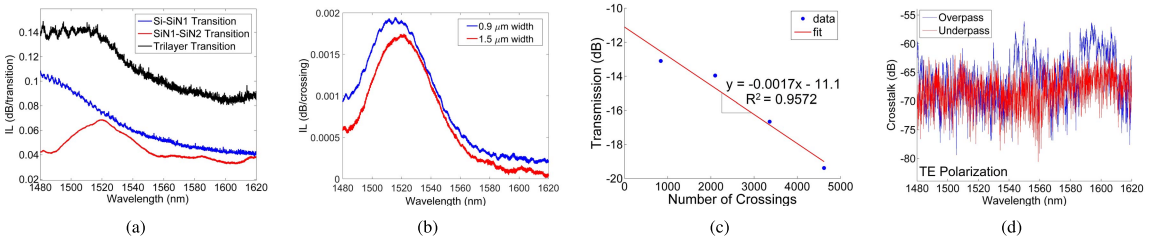


Fig. 5. ***FEOL platform interlayer transition and crossing measurements for the TE polarization across the SCL-bands. (a) Si–SiN1, SiN1–SiN2, and Si–SiN1–SiN2 (trilayer) transition losses. (b) Overpass losses for crossings with 900-nm and 1.5-μm SiN2 widths. (c) Overpass cutback measurement at a wavelength of 1520 nm. (d) Overpass crosstalk. (c) and (d) Crossings with a 1.5-μm SiN2 width. (a), (b), and (d) Reprinted with permission from [20], OSA.***

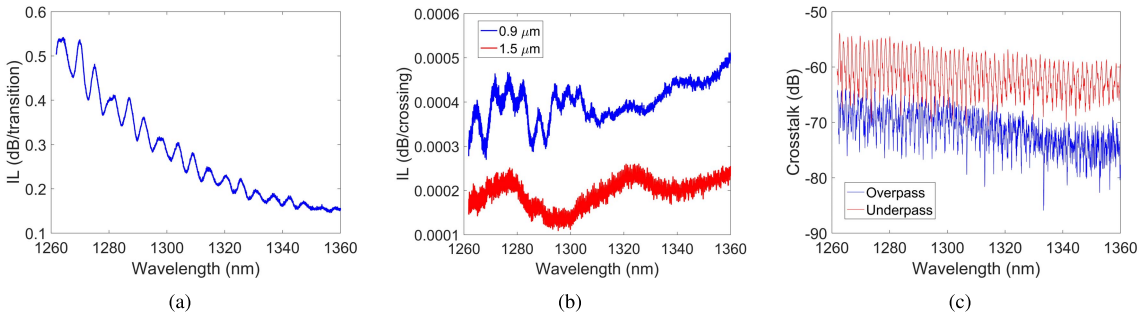


Fig. 6. ***O-band transition and crossing measurements of the FEOL platform for the TE polarization. (a) Trilayer (Si–SiN1–SiN2) transition loss. (b) Overpass crossing losses for crossings using 900-nm and 1.5-μm SiN2 widths. (c) Overpass crosstalk for crossings using a 900-nm SiN2 width.***

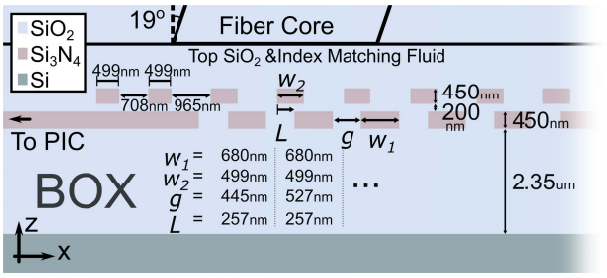
In the trilayer BEOL platform of Fig. 1(a), we have implemented O-band bilevel SiN-on-SiN TE GCs and trilevel polarization-independent SiN–SiN–Si GCs. Fig. 7(a) shows the design of a uniform SiN-on-SiN GC, and Fig. 7(b) shows the measured and simulated transmission spectra of the GC with index matching fluid applied. The measurements show $\eta = -3.5$ dB and $\Delta\lambda_{1\text{dB}} = 53$ nm. The measured insertion loss was about 1.5 dB higher than simulated, suggesting the GC features may not have been accurately fabricated. Nonetheless, the simulations project that with improved fabrication, a bilevel SiN-on-SiN GC can potentially achieve better performance than a single-layer SiN GC (e.g., $\eta = -4.2$ dB with $\Delta\lambda_{1\text{dB}} = 67$ nm in [46]).

To implement polarization diversity on-chip using GCs, polarization-splitting GCs, often having 2-D grating features, are typically used [47]–[53]. In the O-band, polarization splitting GCs with peak efficiencies up to -2.7 dB with a back reflector [54] and -3.3 dB without a back reflector [55] have been reported. Coupling efficiencies as low as -1.95 dB have been demonstrated in the S-band using a double-SOI substrate [48]. A polarization independent GC, where both TE and TM polarizations from the optical fiber are coupled into the same output waveguide, would effectively act like an edge coupler, which would then connect to a polarization rotator-splitter to implement polarization diversity [56], [57]. Thus far, polarization-independent GCs have been based on novelly shaped or nonuniform grating teeth [58]–[60], tailoring of layer and etch thicknesses and geometry to balance TE and TM coupling [61], [62], or relying on subwavelength effective medium structures [63]–[65]. To date, the highest efficiency polarization-independent GC that has been experimentally demonstrated has a peak coupling efficiency of -6.5 dB with a 12-nm 1-dB polarization-dependent loss bandwidth (PDL BW) [65].

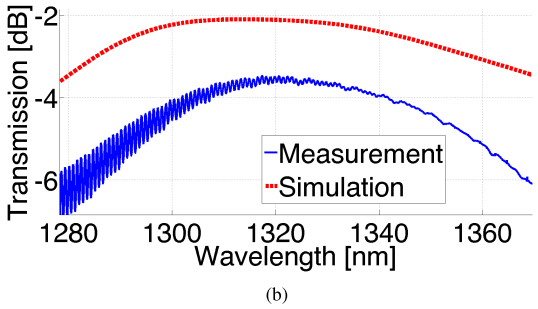
In designing the bilevel SiN-on-SiN GCs, we observed that such GCs had lower polarization dependence than SiN-on-Si and Si-only GCs. By adding grating teeth in the thin, partially etched, Si slab layer under the SiN-on-SiN features, the TE and TM spectra can be aligned, leading to trilevel GCs that are polarization independent. Figure 8 details the design of the trilevel polarization-independent design, which uses the two fully etched 450-nm-thick SiN layers atop the 65-nm-thick partially etched Si layer, for a 34° polished fiber angle. This trilayer SiN–SiN–Si GC, to the best of our knowledge, sets a new record for the highest measured coupling efficiency and 1-dB PDL BW for polarization-independent GCs at this time. Each of the 14 grating periods of the GC and associated layer fill factors has been individually optimized, with the variables labeled in Fig. 8(a) in the ranges of $g \in (554, 941)$ nm, $w_1 \in (776, 1136)$ nm, $L_2 \in (338,621)$ nm, $w_2 \in (498, 939)$ nm, $L_0 \in (482, 762)$ nm, and $w_0 \in (1015, 1484)$ nm.

Table 2 Summary of Performance of SiN–Si Multilevel Grating Couplers

Property	Bilevel SiN-on-Si [43]		Bilevel SiN-on-Si [32]		Bilevel SiN-on-Si [37]		Bilevel SiN-on-SiN (this work)		Trilevel SiN-on-SiN-on-Si (this work)	
	Simulated	Measured	Simulated	Measured	Simulated	Measured	Simulated	Measured	Simulated	Measured
Center wavelength (nm)	1536.0	1536.3	1536.0	1542.2	1311	1303	1313	1320	TE: 1307 TM: 1307	TE: 1305 TM: 1305
Peak coupling efficiency (dB)	-1.0	-1.3	-1.8	-2.3	-1.5	-2.1	-2.1	-3.5	TE: -2.3 TM: -2.0	TE: -5.6 TM: -5.5
1-dB bandwidth (nm)	82	80	114	110	73	72	76	53	TE: 37 TM: 65 PDL: 67	TE: 47 TM: >100 PDL: 80

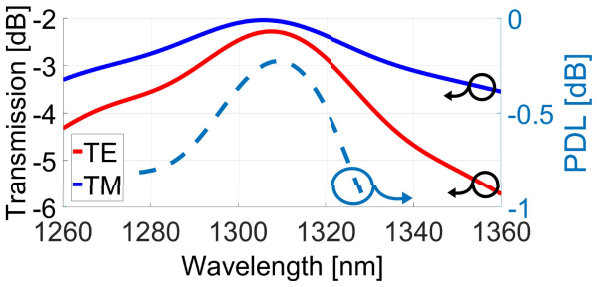


(a)

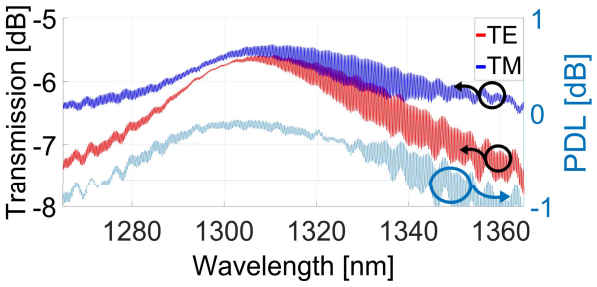


(b)

Fig. 7. *(a) Cross-section schematic of the bilevel SiN-on-SiN GCs. (b) Measured (blue) and simulated (red) transmission for single-polarization (TE) bilevel SiN-on-SiN GCs.*



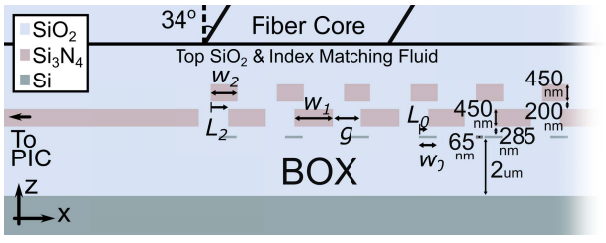
(a)



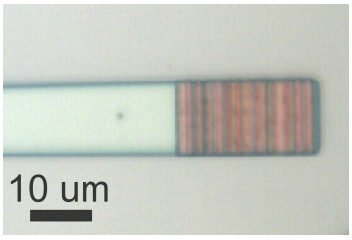
(b)

Fig. 9. *(a) Simulated and (b) measured transmission for the trilevel polarization-independent grating coupler. Transmission spectra for TE (red) and TM (blue) polarized inputs are compared on the left y-axis; polarization-dependent loss (PDL) is plotted on the right y-axis (light blue).*

The simulation in Fig. 9(a) shows the TE and TM spectra are spectrally aligned, with peak coupling efficiencies of −2.3 and −2.0 dB and 1-dB bandwidths of 37 and 65 nm, for the TE and TM polarizations, respectively. The 0.5-dB PDL BW is 25 nm and the 1-dB PDL BW is 67 nm. The measured spectra in Fig. 9(b) show qualitative agreement with the simulation. The peak coupling efficiencies for the TE and TM polarizations are −5.6 and −5.5 dB, respectively; the 1-dB bandwidths are 47 and >100 nm, for the TE and TM polarizations, respectively; and the PDL is less than 0.5 dB over a 44-nm bandwidth and less than 1 dB over a 80-nm bandwidth. Similar to the SiN-on-SiN GCs fabricated in the same wafer (Fig. 7), the measured trilevel GC had an excess insertion loss compared to the simulation, likely due to fabrication errors. Low-loss, polarization-independent GCs would offer an alternative to polarization splitting GCs without the need for in-plane 2-D grating features.



(a)



(b)

Fig. 8. *(a) Cross-section schematic of the trilevel polarization-independent GC design. The GC is nonuniform, and fill factors and period lengths for each of the 14 periods are individually optimized. (b) Micrograph of the fabricated trilevel grating in the BEOL platform.*

C. Thermo–Optic Phase Tuners

Due to the higher thermo–optic coefficient of Si compared to SiN, thermo–optic phase tuners are more power efficient when implemented in Si waveguides. The local temperature of a Si waveguide can be directly changed using doped resistive heaters in the Si level. However, to provide the flexibility of thermo–optic tuning of SiN, the platform in Fig. 1(a) also contains a resistive layer of TiN for thin film heaters. To improve the heater efficiency, deep trenches can be defined near the heater to thermally isolate the heater region from other areas of the die as illustrated in Fig. 1(a). Trenches that are nominally 15 μm wide are defined next to the waveguide region, and the heater is 213 μm in length. The thermo–optic efficiency was quantified using Mach–Zehnder interferometer (MZI) structures

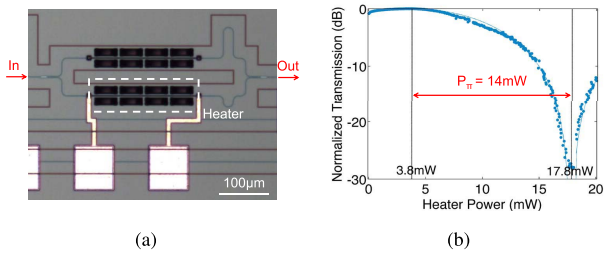


Fig. 10. *(a) Optical micrograph of the MZI heater test structure. (b) Normalized transmission versus heater power.*

implemented using Si strip waveguides. Fig. 10(a) shows the optical micrograph of the test device, and Fig. 10(b) shows the transmitted power as a function of the heater power. The heater exhibits a tuning efficiency metric, represented by the power required for a π phase shift, of $P_\pi =$ 14 mW. This is competitive with certain doped Si heaters that directly heat the waveguides ($P_\pi = 12.7$ mW in [66]). The heater efficiency can be further improved by removing the substrate Si in the heater region and by using serpentine winding waveguides in the tuner region. Combining these two design strategies have led to Si thermo–optic phase tuners with efficiencies as high as $P_\pi = 0.5$ mW as reported in [67].

IV. ACTIVE DEVICES

The BEOL platform also integrates P and N implantations to support carrier injection optical switches, carrier depletion modulators, and Ge PDs in the Si level [39]. These devices can also be implemented in generic Si photonic platforms that do not have any SiN layers. In particular, we implemented U-shaped PN junctions that exhibited high electro–optic efficiencies and the Ge PDs are found to have a near ideal responsivity for the O-band. Efficient electro–optic devices are necessary for large-scale PICs. Here we briefly review the performance of modulators and PDs that were part of the trilayer BEOL platform in Fig. 1(a) [39].

A. Carrier Depletion Modulators With U-Shaped PN Junctions

For high-speed modulation that is not limited by the minority carrier recombination lifetime in Si, carrier depletion modulators are preferred over carrier injection types [68]. For electro–optic modulation, the free carrier plasma dispersion effect is typically used. Since the refractive index change results from a voltage induced charge density change, efficient Si modulators necessitate a high junction capacitance, which often leads to higher optical losses. The most commonly used modulation junction today is a lateral PN junction, which has a relatively high $V_\pi L$ of about 2.5 V·cm, but low propagation losses of 10 dB/cm [4]. Vertical and interdigitated PN junctions have lower $V_\pi L$ of about 0.75–1 V·cm in the C-band, but the waveguide propagation loss is about 25 to 30 dB/cm [69]–[71]. The most efficient MZMs have a SISCAP geometry, which uses carrier accumulation. $V_\pi L$ of 0.2 V·cm has been demonstrated, but the optical loss was about 65 dB/cm [72].

In [40] and [73], we reported U-shaped PN junctions for efficient MZMs and microring modulators. This junction was first proposed theoretically in [74] and [75]. We proposed the implantation steps to be compatible with the BEOL platform and the foundry capabilities. Importantly, the fabrication of this PN junction did not require any extra masks compared to a lateral PN junction, and the implantation steps were kept at normal incidence to be compatible with curved waveguides [40]. Fig. 11(a) shows the designed doping concentrations and depletion regions of the junction at 0- and −1-V bias. The edges of the depletion region are highlighted in red. The junction supports a high modulation efficiency because its per-length capacitance is high (due to the effectively larger surface area of the depletion region afforded by the U-shape) and an excellent overlap exists between the depletion region change and the optical mode. Since a high dopant concentration is not required to achieve the capacitance, the optical loss can be kept low. Therefore, the U-shaped junction breaks

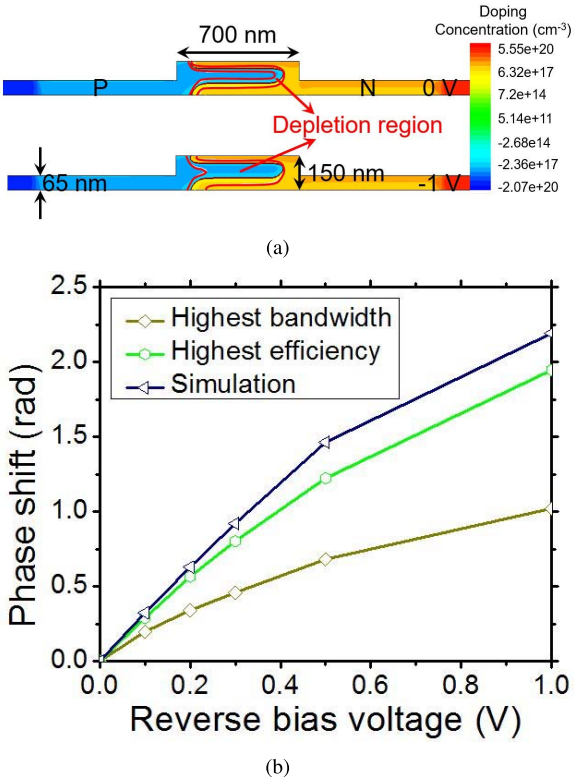


Fig. 11. *(a) Simulated cross sections of the active doping profiles using Sentaurus TCAD of the U-shaped PN junction under bias voltages of 0 and −1 V, as taken from [40]. (b) Simulated and measured phase shift of a 2-mm-long U-shaped PN junction phase shifter at different reverse bias voltages, as taken from [40].*

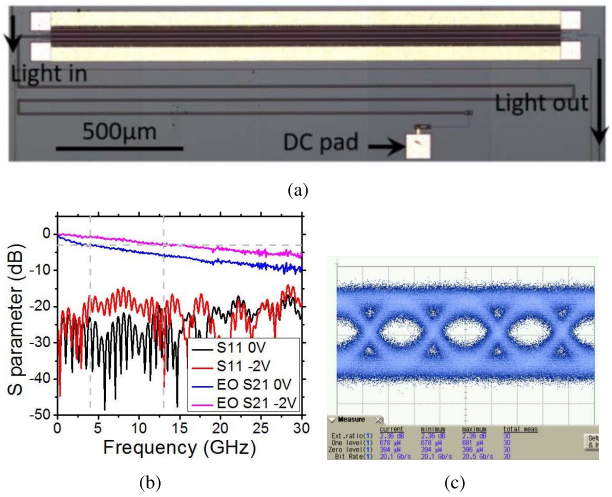


Fig. 12. *(a) Optical micrograph of the MZM incorporating the U-shaped junction. (b) The measured S-parameters of the MZM. (c) The measured eye pattern at 20 Gb/s for a PRBS $2^{31}-1$ pattern at a voltage swing of 2.88 V_{pp} with a −2.4-V bias. (a) and (c) Reprinted with permission from [40], OSA. (b) Adapted from [40].*

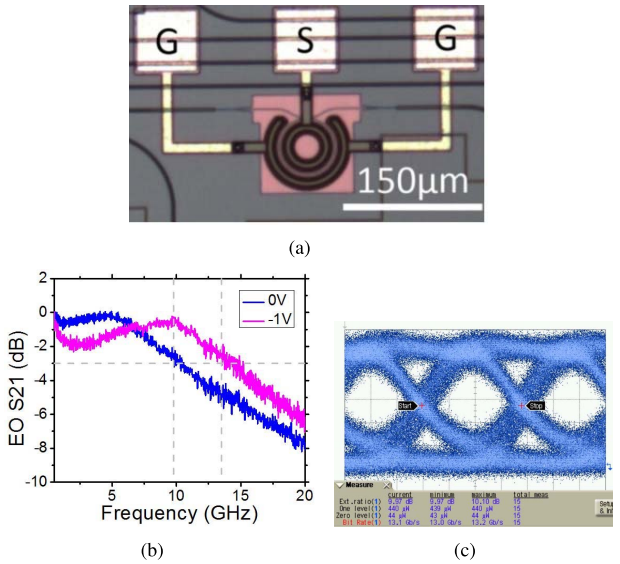


Fig. 13. *(a) Optical micrograph of a microring modulator incorporating the U-shaped junction. (b) The measured EO S21. (c) The measured eye pattern at 13 Gb/s for a PRBS $2^{31}-1$ pattern at a voltage swing of 1.6 V_{pp} with a 0-V bias. Reprinted with permission from [40], OSA.*

the tradeoff between electro–optic efficiency (i.e., high capacitance density) and optical loss.

Fig. 11(b) shows the simulated and measured phase shift of a 2-mm-long U-shaped junction phase shifter at different reverse bias voltages [40]. The measured junction capacitance changed from 2.2 to 0.3 pF/mm between 0- and −2-V bias voltages. We measured several dies across the wafer and found that different devices had slightly different direct current (DC) $V_\pi L$ and bandwidths. The device with the highest efficiency had a $V_\pi L$ of 0.26 V · cm, the device with highest bandwidth had a $V_\pi L$ of 0.46 V · cm at a bias of −0.5 V for the O-band. The $V_\pi L$ value is characterized using the slope efficiency measured at −0.5-V bias. At higher reverse bias voltages, the DC tuning efficiency of the U-shaped junction would reduce. Ideally, the diode should operate at low reverse bias voltages. The optical propagation loss of the phase shifter was about 12.5 dB/cm. The loss-efficiency product (i.e., product of the propagation loss and $V_\pi L$) of the U-shaped junction is about 3.25–5.75 V · dB, which is the lowest among monolithic Si modulators [40].

The U-shaped junctions have been used in MZMs and microring modulators [39], [40]. The MZMs had 2-mm-long phase shifters and were designed in the single-drive push–pull geometry [Fig. 12(a)] [40]. Fig. 12(b) shows the electrical S11 and EO S21 of the MZM with the highest bandwidth at 0- and −2-V bias. The S11 is less than −14 dB over a 30-GHz frequency range, indicating low radio-frequency (RF) reflection. The EO 3-dB bandwidth extended from 4 GHz at 0-V bias to 13 GHz at −2-V bias. Due to a higher than expected capacitance, the bandwidth of the traveling-wave electrodes was compromised and a higher reverse bias was needed to reach >10-GHz EO bandwidths. However, the modulation efficiency of the U-shaped junction is lower at higher reverse bias voltages. So the measured extinction ratio of the MZM is low at high bit rates. bit rates. Fig. 12(c) shows the eye pattern at 20 Gb/s for a pseudorandom bit sequence (PRBS) $2^{31}-1$ pattern and a driving signal swing of 2.88 V_{pp} at a bias of −2.4 V. The input wavelength was set at the MZM quadrature point and an ER of 2.4 dB was achieved. Fig. 13 shows the results for the microring modulator,

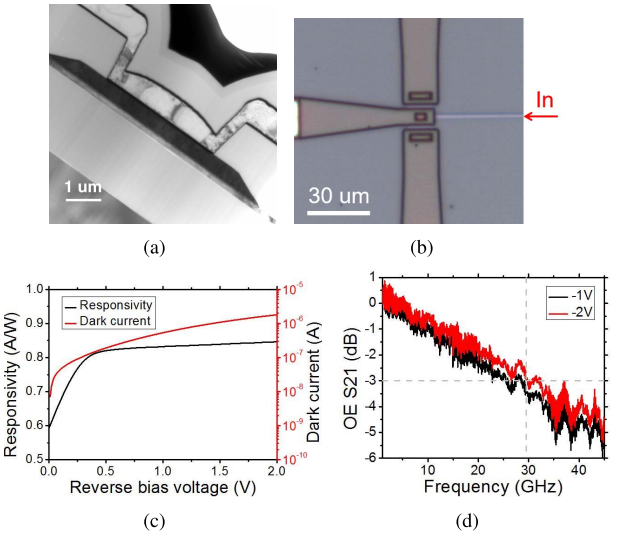


Fig. 14. *(a) XTEM of the Ge PD. (b) Optical micrograph of the Ge PD with a 10-μm-long Ge region. The (c) responsivity, dark current, and (d) OE S21 of the Ge PD in (b).*

which had an effective diameter of 62.5 μm and the waveguide rib width of 500 nm. The 3-dB EO bandwidth was 9.8 GHz at 0-V bias and extended to 13.5 GHz at −1-V bias. Fig. 13(c) shows the 13-Gb/s eye pattern of the ring modulator for a PRBS $2^{31} - 1$ pattern and a driving signal swing of 1.6 V_{pp} at 0-V bias. The achieved ER was 10 dB with an insertion loss of 2.5 dB. The high DC efficiency and the potential for high bandwidths make the U-shaped junction promising for EO modulators in Si.

B. Photodetectors

The photodetector in the fully integrated multilayer platform uses the standard Ge vertical photodetector structure from IME [4]. The Ge was 500 nm thick, and the XTEM is shown in Fig. 14(a). It was fabricated using the standard growth and patterning process in the IME multiproject wafer shuttle service. The optical micrograph of the Ge PD is shown in Fig. 14(b). The DC and RF properties of a PD with a 10-μm-long Ge section are shown in Fig. 14(c) and (d). The responsivity varies from 0.6 to 0.85 A/W at 1310 nm for a reverse bias voltage between 0 and 2 V. The dark current was 2 μA at 2-V reverse bias. The optoelectronic (OE) S21 3-dB bandwidth is about 29 GHz at a −2-V bias.

V. CONCLUSION

In summary, we have reviewed the progress on monolithically integrated SiN-on-Si integrated photonic platforms that have two waveguide layers of SiN atop a Si waveguide layer. A library of passive and active devices that include low-loss interlayer transitions, waveguide crossings, grating couplers, thermo–optic phase tuners, U-shaped modulation junctions, and Ge photodetectors has been developed and demonstrated. Multilayer SiN-on-Si photonic platforms enable certain passive devices, such as optical filters or wavelength multiplexers, in a PIC to be implemented in SiN, a better passive CMOS-compatible optical material than Si. Novel hybrid 3-D SiN-on-Si devices that take advantage of the coupling of optical waves between the levels can also be implemented. On a circuit level, the multilayer platforms make possible complex 3-D on-chip optical interconnect networks. Overall, the monolithic multilayer SiN-on-Si platforms open an avenue toward densely integrated 3-D photonic circuit architectures. ■

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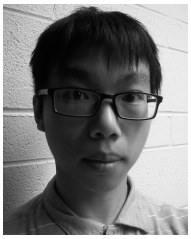

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