TEST STAND FOR THE SILICON VERTEX DETECTOR OF THE COLLIDER DETECTOR FACILITY

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Abstract

A test stand for the next generation of the Silicon Vertex Detector (SVX-II) of the Collider Detector Facility (CDF) at Fermilab has been developed. It is capable of performing cosmic ray, beam, and laser pulsing tests on silicon strip detectors using the new generation of SVX chips. The test stand is composed of a SGI workstation, a VME CPU, the Silicon Test Acquisition and Readout (STAR) board, the Test Fiber Interface Board (TFIB), and the Test Port Card (TPC). The STAR mediates between external stimuli for the different tests and produces appropriate high level commands which are sent to the TFIB. The TFIB, in conjunction with the TPC, translates these commands into the correct logic levels to control the SVX chips. The four modes of operation of the SVX chips are configuration, data acquisition, digitization, and data readout. The data read out from the SVX chips is transferred to the STAR. The STAR can then be accessed by the VME CPU and the SGI workstation for future analyses. The detailed description of this test stand will be given.

I. Introduction

We have developed a test stand for the next generation of the Silicon Vertex Detector (SVX-II) for CDF. The objective of this development is to allow the testing of the new generation of SVX chips [1] and the characterization of the SVX-II prototype detectors, and as a proof of principle of many of the conceptual ideas regarding the future data acquisition system (DAQ) for the SVX-II detector [2].

Figure 1 shows the block diagram of the test stand. The STAR [3] and the TFIB [4] are 9U x 400 mm VME boards which implement the VME J1 interface and a customized J3 backplane interface while the TPC [5] is a 10"x10" board. The TPC sits close to the SVX detector and associated SVX chips in order to deliver the proper single ended TTL levels and the regulated power supply voltages through the High Density Interconnect (HDI) cable. The SGI workstation controls the test stand through the Ethernet interconnection and the VME CPU. The STAR mediates between external stimuli and triggers for the different tests and produces appropriate high level commands which are sent through the J3 backplane (or optionally through a front panel connector) to the TFIB. The TFIB receives these commands and produces different types of SVX chip clocks and low level commands which are differentially sent to the TPC. The TPC then produces the correct sequence of logic levels to control the SVX chips and to readout the data. The parallel readout data travels from the TPC to the TFIB and STAR. The STAR then saves the data into data buffers. Later on, the workstation retrieves, analyzes, and stores the data.

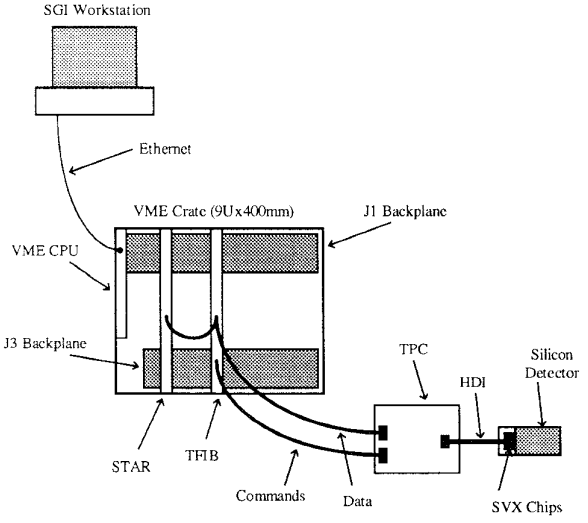

Figure 1: SVX-II Test Stand Block Diagram

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II. Test Stand Modules

A. The SVX Chip

The SVX chip implements a pipeline of 32 rows of analog storage cells per channel and a total of 128 channels per chip. The four distinct modes of operation of the SVX chips are configuration, acquire, digitize, and readout. The configuration mode is used to serially download internal control registers and a hit test pattern for diagnostic purposes. In the acquire mode, two separate operations take place. The preamplifier first integrates charge from the detector, and the pipeline samples and stores the integrator output at the predetermined interaction rate (minimum of 132 ns). Then, sampling of the input signals stop, and the sample with the proper delay is selected and presented at the pipeline output. In the digitize mode, the analog information of all 128 channels is simultaneously digitized to programmable resolution of up to 8 bits. In the readout mode, the digitized date is read out on an eight bit parallel bus. When readout of the chip begins, the chip ID number appears first on the high part of the clock cycle and then an 8 bit status word appears on the following lower half of the clock cycle. After the first complete clock, address and data appear on alternate halves of the cycle until the chip is completely read out. The primary reason for changing modes is to change the function of some or all of the multifunctional chip pads.

B. The STAR

The main functions of the STAR module are to respond to a trigger source (e.g. laser pulsing, particle beam) by means of producing and sending high level commands to the TFIB, to provide a fully programmable Master Clock which emulates the Fermilab accelerator beam structure, and to serve as a data buffer accepting digitized data from the SVX chips via the TPC. The overall block diagram of the STAR is shown in Figure 2.

The Master Clock replicates the accelerator radio frequency (RF) structure by generating an RF clock, a SYNC pulse which marks potential beam crossings every seven RF clocks, and a beam crossing level which, when qualified by SYNC, indicates the presence of a bunch. The Master Clock structure is fully programmable and can emulate 132 ns or 396 ns operation modes of the accelerator. The internal timebase is a 53 MHz crystal which corresponds to the actual accelerator RF. An external clock input is also provided to run the system at any desired frequency within its operating range. Data from the SVX data bus arrives at 53 MBytes per second along with a 26.5 MHz readout clock. The data inputs of the STAR demultiplexes the data stream and loads it into a 64k x 16 bit memory for later VME readout. The STAR employs three data buffers.

A Memory Test facility is provided to test the STAR data buffers as well as similar buffers on other boards. This consists of a 32k x 16 bit memory and a Data Multiplexer to emulate the SVX data stream and put it out onto a cable. The 32k x 2 bytes is time multiplexed at 26.5 MHz to form a 1 byte wide by 53 MBytes per second data stream. When used to test one of the data buffers of the STAR, the test memory output cable is connected to the data buffer input. Blocks of data up to 32k in size along with header (Chip ID) and trailer (end of readout) codes can be sent to the data buffers for diagnostic purposes.

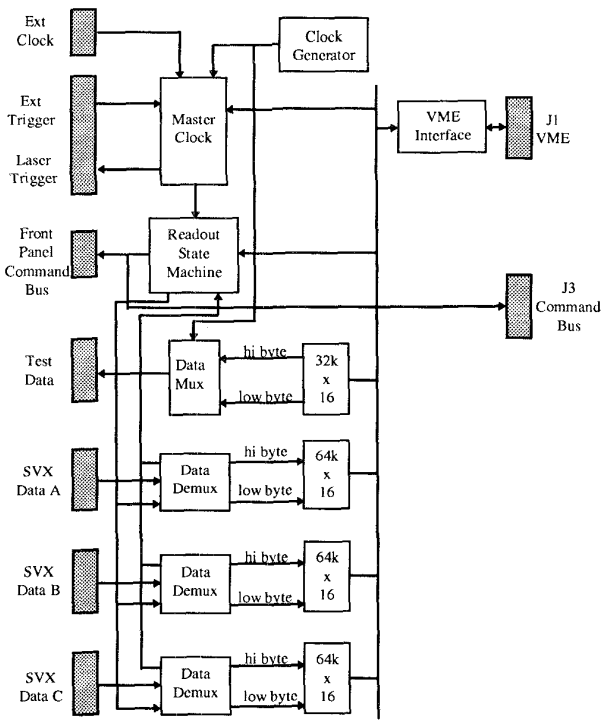

Figure 2: STAR Block Diagram

Command sequences are generated in the STAR by a finite state machine referred to as the Readout State Machine. The exact sequences depend on the mode of operation. A list of commands has been established for STAR/TFIB communication. The state machine operation modes are controlled by means of a state machine Control register. It should be pointed out that the interface with the triggers is handled by the Master Clock. Triggers are generated either internally or externally and then passed on to the Readout State Machine to trigger the appropriate action. Several different trigger types have been provided for and are referred to as external (beam testing, cosmic ray) or internal (charge injection, laser testing) triggers.

C. The TFIB

The main function of the TFIB is to control the SVX chips in conjunction with the TPC. The control functions have been divided between these two modules in such a way

that the TFIB has been selected to execute the high level commands sent by the STAR and to translate these commands into low level commands executable by the TPC. Other functions of the TFIB includes the configuration of the SVX chips and the TPC Controller, the configuration of the DACs on the TPC, and the emulation of the high level commands sent by the STAR. Figure 3 shows the block diagram of the TFIB.

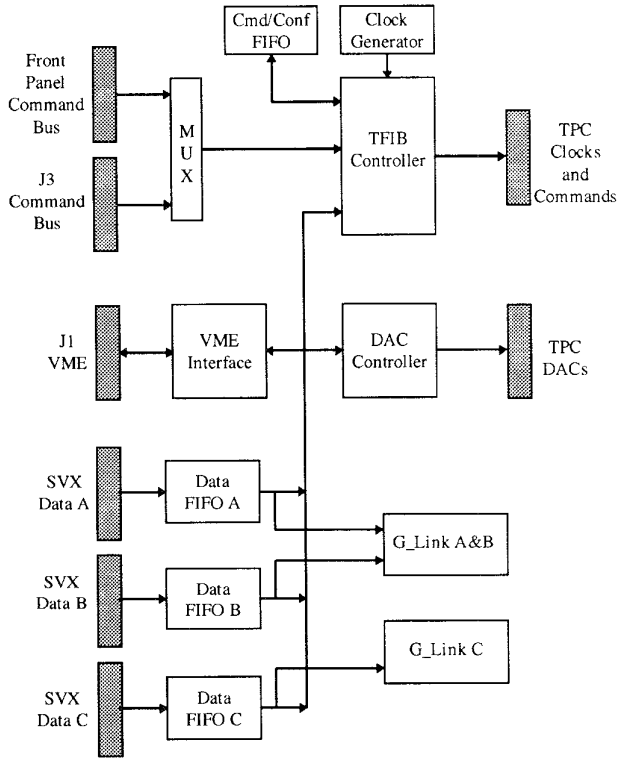

Figure 3: TFIB Block Diagram

All units of the TFIB operate synchronously with the clock which can be supplied by the STAR or by its own internal Clock Generator. The TFIB Controller controls all the functions of the TFIB. It receives high level commands from the STAR (through the Front Panel or through the J3 backplane), emulation commands from the Command Configuration FIFO, or immediate commands when the VME interface sets the appropriate bits of the TFIB Control Register.

The high level commands are used for the control of the data acquisition, digitization, and readout of the SVX chips. Other high level commands include provision for calibration of the SVX chips, for resetting of the TFIB, TPC, and SVX chips, and for diagnostic testing. The emulation commands are the same as the high level commands allowing the TFIB and TPC to be tested independently of the STAR. This has been shown to be a powerful tool for diagnostic testing as well as for the development of the TFIB and TPC. The immediate commands are used for configuration of the SVX chips and the FPGA of the TPC, different resets, and for diagnostic testing.

The emulation commands operate in the following way. The VME CPU writes to the Configuration Command FIFO the list of commands to be executed. The VME CPU then uses one specific immediate command of the Control Register to trigger the emulation operation. The TFIB then reads from the Configuration Command FIFO the list of commands and executes them in the same fashion it executes the commands coming from the STAR.

The TFIB receives commands, interprets these commands, and when necessary sends low level serial commands to the TPC. After the low level command is delivered, the TFIB and the TPC work synchronously. The TFIB Controller sends clocks to the TPC to advance the state machine of the TPC Controller (see Figure 4) with the appropriate timing required by the SVX chips. It also delivers clocks directly to the SVX chip if the operation requires.

Another important function executed by the TFIB is the shaping and frequency control of the SVX chip clock. In the final data acquisition system, the maximum and minimum delay of the SVX chip clock has to be controlled within strict boundaries in order to guarantee that all SVX chips controlled by different TFIBs and TPCs will be acquiring data synchronously.

The bottom portion of the TFIB block diagram has a set of components to receive the data read out from the TPC independently of the STAR. These FIFOs are smaller than the data buffers of the STAR, but they can be used to save events from a few SVX chips. Connected to the Data FIFOs are two G-Links [6] which were added to the TFIB for testing purposes. When the Data FIFOs are delivering data to the G-Links, they are used to synchronize the data from different HDIs.

For configuration of the SVX chips and the TPC Controller, the TFIB Controller also uses the Configuration Command FIFO and specific low level commands. When the VME CPU requests the download of the configuration of the SVX chips, the TFIB requests to the TPC Controller to set the SVX chips into configuration mode. The TFIB Controller then reads the configuration bytes from the Configuration Command FIFO, serializes, and sends them to the TPC. A similar operation occurs when the TFIB Controller configures the TPC Controller or when the Digital-to-Analog Converter (DAC) Controller configures the DACs of the TPC.

D. The TPC

The TPC interfaces with the TFIB, the STAR, and the SVX chips. A Xilinx FPGA [7] has been selected to implement the TPC Controller. The initialization and programming of the TPC Controller on the TPC is done by the TFIB under VME control. A block diagram of the TPC is shown in Figure 4.

The main function of the TPC is the control, initialization, and readout of up to three sets of SVX chips connected to HDI cables. Other important features include the buffering of the SVX chip clock, the transmission of the SVX data to the TFIB and STAR, the recognition and insertion of the end of readout (EOR) byte into the SVX data stream, the implementation of serially downloaded DACs for generation of the voltage references of the SVX chips, and the regulation and filtering of the power supplies of the SVX chips.

The control of the TPC and associated SVX chips is implemented by a serial interface which includes a serial command signal, a serial command clock, and the SVX chip clock. The functions supported by the current implementations of the TPC Controller are initialization, readout, enter acquisition mode, preamplifier reset, calibration inject, perform digitization-readout, and readback of the TPC Controller FPGA configuration. The TPC Controller implements a control sequence for each of these commands. Once the command has been transmitted, the TFIB sequences the TPC Controller through the different states with the serial command clock line. Each state is associated with a specific configuration of the control lines of the SVX chip. The TPC Controller requires a fixed number of rising edges of the clock to complete the command execution before it can be ready to execute a new command. In addition, the TFIB controls the state timing sequencing by controlling the time between the serial command clock edges.

As we have already stated, the control of the SVX chips is split into the TFIB and the TPC. In this application, the TPC is an extension of the TFIB which provides local control to the SVX chips. Clearly, the control of the SVX chips could be implemented in some other way. However, with the design of the test stand we are also interested in proving the principle of conceptual ideas regarding the future DAQ. The approach that we are presenting meets several requirements of the final DAQ. For example, it is necessary to reduce the number of control lines going to the final Port Card in order to reduce the cable mass. The solution presented here uses just one serial command line and two clock lines. Another example: the electronic components of the final Port Card need to resist radiation. To accomplish this the final Port Card Controller can be implemented using a small

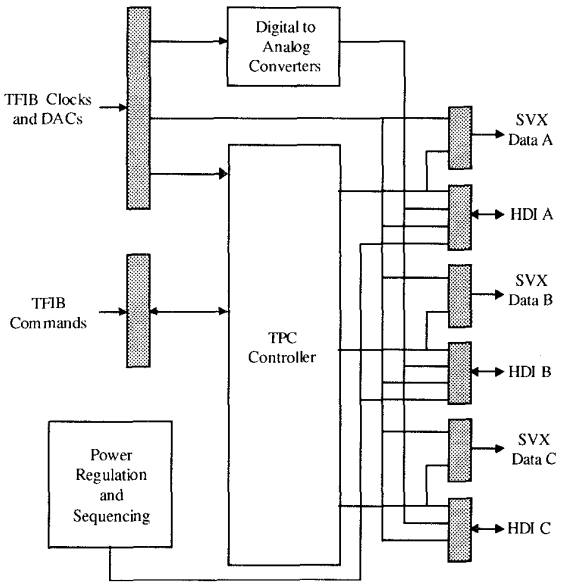

Figure 4: TPC Block Diagram

commecially available rad-hard FPGA. The separation of functions between the TFIB and the TPC accounts for allowing the implementation of the commands inside a small FPGA, which can be replaced in the future by the rad-hard version.

As an example of one procedure to control the SVX chips, the following is the sequence of steps used to perform an event readout.

- The STAR sends to the TFIB the high level digitize-readout command.
- The TFIB interprets the command and sends to the TPC Controller the serial low level digitize-readout command. It then delivers serial command clocks and SVX chip clocks as required by the SVX chips.
- The TPC Controller sets the appropriate lines of the SVX chips to change their operation mode to digitization.
- The TFIB then sends SVX clocks to perform the analog to digital conversion of the storage cells.
- After digitization, the TPC Controller sets the SVX chips to readout.
- The TFIB now delivers SVX chip clocks and reads out the data from the chips. The TPC monitors the SVX chips until it recognizes that all data was read out and then it asserts the EOR byte into the data stream.
- The STAR saves the data. In parallel, the TFIB monitors the readout data until it recognizes the EOR byte, when it then stops the SVX clock.
- Finally, the TFIB automatically sends one more low level command to the TPC to set the SVX chips into acquisition mode.

There are other commands initiated at the STAR that are destined for the SVX chips. The control flow for other operations are similar to the operation described above.

III. Results of the KEK Beam Test of SVX-II Prototype Detectors with the Test Stand

In June 1995, the test stand operated at the KEK 3 GeV pion beam to study SVX-II prototype detectors. The data taken was used to measure the pedestals in a first pass and then reused to search for clusters in a second pass. During the pedestal measurement, the noise on each channel was also determined. The noise is usually taken to be the RMS of the non-zero-suppressed signal on any one strip. The noise and differential noise (D-noise) profile for an detector as taken online are given in Figure 5 and Figure 6.

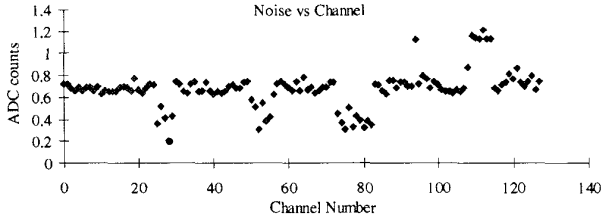

Figure 5: Detector Noise Profile

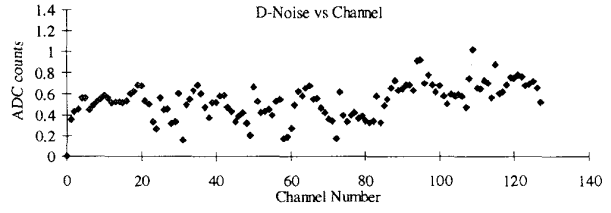

Figure 6: Detector D-Noise Profile

The D-noise is useful because it represents the irreducible detector noise not due to pickup, poor grounding etc., and is also used to determine the Signal-to-Noise ratio for the detector. The noise is used for noisy strip suppression because it depends on only an individual strip rather than on the neighboring strip like D-noise.

IV. Conclusion

The test stand performed as expected and is being extensively used to test prototype detectors and SVX chips. With the test stand development and operation, we have proven the principle of many ideas regarding the final data acquisition system for the SVX-II detector. Presently, another generation of SVX chips which incorporates the death timeless feature where it continues to acquire data from the SVX detector at the same time that it is digitizing or transferring the data of a previous event to the TFIB and STAR, is being developed and tested. We are in process of studying the modifications on the firmware of the STAR and TFIB in order to control and read out these dead timeless SVX chips. We are also developing the new version of the TPC that will be compatible with the death timeless SVX chips.

V. References

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