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Development of 200 GHz to 2.7 THz Multiplier Chains for Submillimeter-wave Heterodyne Receivers

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ABSTRACT

Several astrophysics and Earth observation space missions planned for the near future will require submillimeter-wave heterodyne radiometers for spectral line observations. One of these, the Far InfraRed and Submillimeter Telescope (FIRST) will perform high-sensitivity, high-resolution spectroscopy in the 400 to 2700 GHz range with a seven channel superconducting heterodyne receiver complement. The local oscillators for all these channels will be constructed around state-of-the-art GaAs power amplifiers in the 71 to 115 GHz range, followed by planar Schottky diode multiplier chains. The Jet Propulsion Laboratory is responsible for developing the multiplier chains for the 1.2, 1.7, and 2.7 THz bands. This paper will focus on the designs and technologies being developed to enhance the current state-of-the-art, which is based on discrete planar or whisker contacted GaAs Schottky diode chips mounted in waveguide blocks. We are proposing a number of new planar integrated circuit and device topologies to implement multipliers at these high frequencies. Approaches include substrateless, framed and frameless GaAs membrane circuitry with single, and multiple planar integrated Schottky diodes. Circuits discussed include 200 and 400 GHz doublers, a 1.2 THz tripler and a 2.4 THz doubler. Progress to date, with the implications of this technology development for future Earth and space science instruments, is presented.

Keywords: Submillimeter, Schottky, Multipliers, FIRST, HIFI, Doubler, Tripler, Membrane, GaAs, Diode

1 INTRODUCTION

High resolution millimeter and submillimeter heterodyne observations will improve our understanding of physical phenomena present in the universe [1]. The Far InfraRed and Submillimeter Telescope (FIRST) is a European mission with an American contribution, whose objective is to study the formation and evolution of galaxies in the early universe as well as stellar formation, the physics of the interstellar medium and the interaction between the two [2]. Such observations are severely limited by the absorption of the atmosphere and can only be done via airborne or space borne platforms. FIRST will be launched in 2007 and will be positioned in the L2 orbit. A recent overview of the mission is given in [3].

The Heterodyne Instrument for FIRST (HIFI) includes seven distinct receiver channels. Five pairs of fixed tuned double side-band Superconductor-Insulator-Superconductor (SIS) mixers in dual polarization cover the 480-1250 GHz (625-240 μm) region with a specified system noise temperature of 70-500 K. Two Hot Electron Bolometer (HEB) mixers are expected to cover 1410-1910 GHz (213-157 μm) and 2400-2700 GHz (125-111 μm) with a noise temperature of 650-800 K. The near quantum limited temperatures expected from these receivers will allow for very weak signal detection.

The required local oscillator (LO) sources to pump these mixers are critical to the successful implementation of the mission. The goal of the technology development program for the LO system for FIRST is to enable construction of solid-state sources into the THz range with enough output power and bandwidth to pump the SIS and HEB mixers. Table 1 depicts the seven frequency bands proposed for FIRST along with the required LO power necessary for successful mixing at the three highest bands as suggested by the FIRST Mixer Working group [4]. Frequency stability of 1 part in 10^8 is required. The LO system must also provide for frequency switching to enable side band de-convolution. Due to the large number of required multiplier components, a modular design which reduces cost and simplifies implementation is essential. The US contribution

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is to supply the three highest frequency receivers, while the remaining receivers will be developed and built by a European consortium.

There has been considerable development and improvement of planar Schottky diode multipliers in the last few years. However, the required power and bandwidth performance specifications for the FIRST LO sources remain rather challenging. The highest frequency multiplier circuit reported to date is a tripler to 1395 GHz, which produces about 17 μW of power with an input power of 7 mW from a carcinotron source [5]. The diode used in this multiplier is a whisker contacted Schottky and the circuit is a traditional crossed waveguide block. The highest frequency all solid-state multiplier chains reported to date are around 1000 GHz. These use an InP Gunn diode oscillator at 111.2 GHz followed by two whisker-contacted triplers in series, and have measured output powers of 60-120 μW [6].

At lower frequencies, balanced planar Schottky diode multipliers (2 series doublers pumped with Gunn oscillators) have been reported in the 350 GHz range with about 5 mW of output power [7]. It is now possible to design and build very high power multipliers in the 150-320 GHz range that can be used to drive follow on stages. 80 mW at 140 GHz, 76 mW at 180 GHz, and 15 mW at 270 GHz have already been demonstrated and a number of variations of the balanced doubler concept [8] have yielded very impressive results [7-10].

In order to realize multiplier chains to 2700 GHz it is essential to pump the lower frequency stages with a significant amount of power and to have primary pump sources that are electronically tunable. The recent success of HEMT-based MMIC power amplifiers [11], satisfy the primary source requirement for FIRST. The amplifiers are driven by low-power YIG- or DRO-based oscillators followed by active multipliers to W-band, where the MMIC power amplifiers supply up to 20 dB of gain. The power amplifier technology development effort is described in a companion paper [11].

The multiplier follow-on stages consist of two components – the nonlinear solid state device (Schottky diode) and the surrounding input, output and impedance matching circuitry. To meet the challenges of FIRST successfully it is important to further refine and advance both of these critical elements. As the frequency increases and all relevant dimensions shrink, it often becomes difficult to separate the device from the circuit. This makes it important to optimize processing in combination with the circuit realization, assembly, and testing procedure. The present paper will focus on the ongoing work at the Jet Propulsion Laboratory to develop and demonstrate multiplier technology that will enable local oscillators at frequencies up to 2700 GHz.

LOCAL OSCILLATOR BANDS FOR FIRST

Initial bands	71-79 GHz	80-92 GHz	88-99 GHz	92-106 GHz	106-112.5 GHz
x2	142-158	160-184	176-198	184-212	212-225
x2 x2	284-316	320-368	352-396	368-424	424-450
x2 x3		480-552 Band 1a		552-636 Band 1b	
x2 x2 x2		640-736 Band 2a	704-792 Band 2b	736-848 Band 3a	848-900
x2 x2 x3	852-948 Band 3b	960-1104 Band 4a	1056-1188 Band 4b	**1104-1272 Band 5 (36 μW)**	1272-1350
x2 x2 x2 x2			**1408-1584 Band 6a (1.2 μW)**		
x2 x2 x3 x2	**1704-1896 Band 6b (1.2 μW)**			**2400-2544 Band 7a (1.2 μW)**	**2544-2700 Band 7b (1.2 μW)**

Table 1 Proposed local oscillator bands for FIRST. The required output power levels assume a 27% diplexer coupling efficiency and a 50% margin on the power levels required at the focal plane unit input port[4]. For Bands 6 and 7 single polarization is assumed. Bold type refers to bands being delivered by JPL.

2 MULTIPLIER TECHNOLOGY

Submillimeter-wave multiplier technology is undergoing a major revolution in implementation and realizable performance, for two main reasons. First, the processing of high frequency planar GaAs diode circuits has undergone tremendous progress, both in the advancement of MMIC style topologies toward higher and higher frequencies, and in the accuracy and reproducibility of the most dimensionally critical elements. This is due to the widespread use of e-beam lithography and the blending of traditional metal machining with GaAs and Silicon micromachining. Second, the availability of high performance CAD tools and models now permits better prediction and optimization of circuit performance.

2.1 GaAs Schottky diode technology

Several issues limit the implementation of GaAs multiplier circuits at very high frequencies. In the most successful lower frequency balanced doubler designs [7-10], a small planar diode chip is mounted into a metallic waveguide block by means of solder or silver epoxy. Bias and RF coupling is introduced using either a ribbon wire or a precision-machined coax structure implemented between the block and the chip [7,8]. A different approach solders the diode chip directly to a quartz based filter which in turn is put into the waveguide block where wire bonds are used to contact the quartz circuit [9,10]. In spite of the success of these designs it is obvious that as the frequency of operation increases, the mounting techniques become excessively difficult. The desired diode chip thickness at 300 GHz is only 38 microns and thickness has a major impact on performance. Moreover, the constraints of reduced waveguide size, increasing substrate loss and higher order mode suppression dictate the use of even thinner substrates when at these frequencies.

In order to circumvent these limitations and implement technologies that can work well into the THz range we have proposed two novel ways of fabricating the multiplier chips [12]. In the first implementation, both the matching circuit and the device are fabricated on the GaAs epitaxial layer. After front side processing is completed a backside procedure is used to remove all of the GaAs under the matching circuit. Only a 50 micron-thick GaAs frame is left, where necessary, to support the matching structure. The Schottky anodes are formed on one edge of this frame. This "substrateless" structure results in an all metallic matching circuit with no underlying dielectric and it incorporates the active device monolithically. The structure is physically much larger than previous diode chips thus allowing easier handling and mounting. Moreover, beam leads placed on the structure improve heat transfer and simplify the assembly procedure when mounting in a separate waveguide block. Some representative passive structures were fabricated to test the mechanical ruggedness of the circuit with great success (Fig.1). Several new multiplier circuits have now been designed using this approach and are described in section 3.1. We plan to employ this "substrateless" technology for all the lower frequency stages of each band on FIRST.

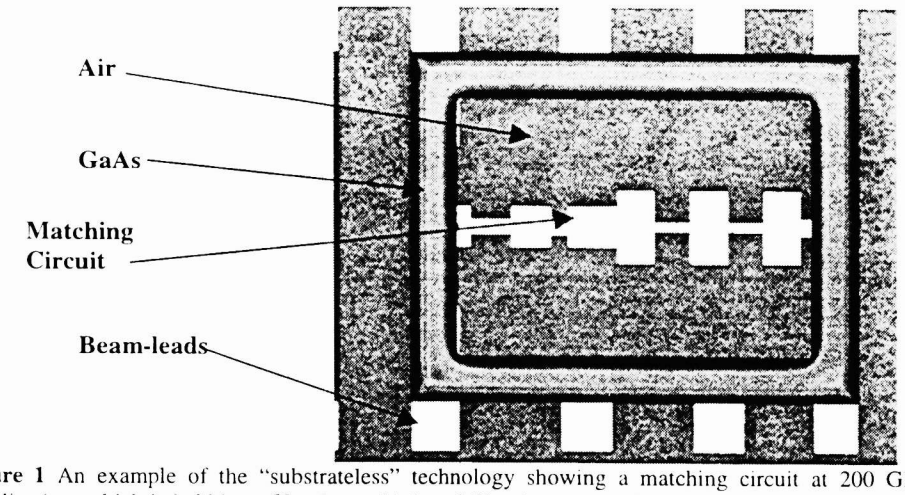


Figure 1 An example of the "substrateless" technology showing a matching circuit at 200 GHz. The white regions are the gold metalization, which is held by a 50-micron thick and 50-micron wide GaAs frame. The devices will be implemented on the other side of the shown structure.

A second approach under consideration for the very high frequency multiplier circuits (1200 to 2700 GHz) is based on a monolithic membrane diode (MOMED) technology first used to fabricate mixers at 2500 GHz [13,14]. In this fabrication approach, a thin (2-3 μm) insulating GaAs membrane bridge is left under the diode and RF filter regions, and the thicker support frame falls outside the active area. The membrane bridge can then be coupled to single-mode coaxial and waveguide circuits fabricated by more traditional machining techniques. A picture of a completed MOMED chip is shown in Figure 2. One planned design improvement in this circuit is the elimination of the frame, leaving a free-standing membrane which allows more flexibility in the substrate shape and circuit implementation. The current efforts are focused on fabricating a 1.2 and a 2.4 THz doubler. Designs will be presented in sections 3.2 and 3.3.

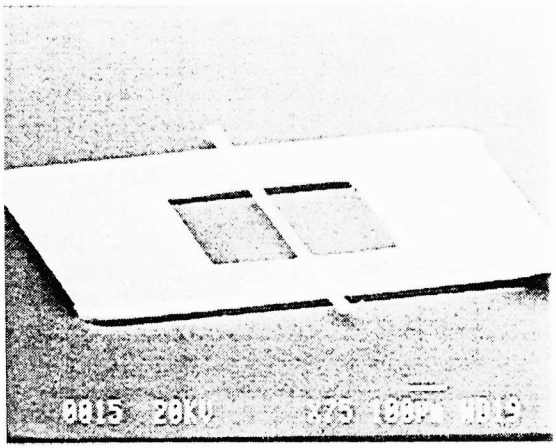


Figure 2 A 2.5 THz mixer [13] on a 3 μm thick GaAs membrane. The central strip is 30 μm wide and is supported by a large 50 μm thick frame which lies outside the active region. Beam leads extend from the membrane and frame for DC contact and IF removal.

2.2 JPL GaAs Schottky diode model

The high frequency GaAs Schottky diode process that has been developed at JPL is based on an anode formation step that is widely used in transistor technology to form the gate structure. An SEM of a JPL fabricated anode is shown in Figure 3. The reason for establishing a process that uses rectangular anode shapes instead of the more traditional circular anodes is to reduce the spreading resistance through the semiconductor [15,18]. This reduces the parasitic resistance associated with the anode, which in turns increases the cutoff frequency while maintaining minimal capacitance. In the traditional Schottky diode process the anode is formed by etching the passivating dielectric and plating the Schottky metalization. However, as the anode sizes shrink to accommodate high frequency operation, uncertainties in the anode dimensions become large. JPL anodes are made by direct write e-beam lithography or a 5X stepper for more precise feature definition and alignment. The anode and the air-bridge are formed in one step thus reducing alignment concerns.

An analytical closed form model has been developed and implemented into a commercial harmonic balance software package to optimize the physical properties of the anode (such as width and length, doping, epilayer thickness) in order to maximize the multiplier efficiency as a function of frequency and input power [15,16,18]. This model has worked well to predict the performance of room temperature diodes up to 300 GHz [17]. However, based on currently available measurements, the discrepancy between theoretical and measured performance increases substantially with frequency. Although part of this behavior can be explained by the tighter tolerances required on fabrication and assembly, it is reasonable to expect that the semiconductor device model is not adequate enough for supra-THz frequencies. To date, the multipliers that have been tested in the THz region seem to exhibit dramatically increased resistance [19]. We have implemented some of the observed effect into our diode model by introducing skin effect inside the buried n+ layer. This effect appears to be important above a few hundred GHz, and has a very strong effect above one THz, doubling the resistance at 1.2 THz and tripling it at 2.4 THz. However, even with this improvement in the model we cannot completely describe the decrease in efficiency observed at high frequency. As a first order compensation, an empirical factor is introduced into the calculation of the series resistance to make it more strongly frequency dependent.

Temperature dependent phenomena also play a role and have been included in our model to allow optimization of the circuit and diode for operation at low temperature. This feature also permits the investigation of the effect of anode heating on efficiency. The very high power levels we use for the first stage multipliers can increase the anode temperature by as much as 100 degrees.

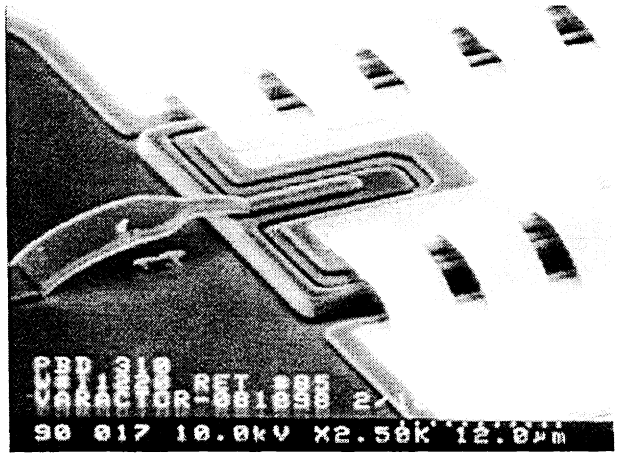


Figure 3 SEM of a rectangular anode Schottky diode and air bridge made at JPL.

2.3 Circuit design methodology

For analyses and design purposes the multipliers are divided into a nonlinear active region, which models the behavior of the diode, and a linear passive region which contains the rest of the circuit. The JPL Schottky diode model is used in conjunction with an harmonic balance simulator to optimize the physical parameters such as anode width and length, and obtain the optimized embedding impedance for the junction. This takes into account only the actual Schottky contact characteristics. The parasitics associated with the diode implementation (mesa, air bridges, etc.), are analyzed using a separate finite element electromagnetic simulator and merged with the diode model.

The larger multiplier input and output matching circuits are then designed using a circuit simulator in an iterative process. The electromagnetic simulator is used to analyze the passive circuit elements, yielding scattering parameter matrices referenced to the diode and waveguide ports. To simplify and speed up the process, the passive circuitry is divided up into small elements at electromagnetically appropriate points, giving several S-parameter matrices. Ports are attached to probes on each anode so that the individual embedding impedances for each diode can be calculated directly. The diodes (with parasitics) are then embedded into the resulting cascaded S-parameter matrix blocks to determine the total efficiency and power performance of the multiplier. If these are unsatisfactory compared to the intrinsic performance of the diodes, the circuit design is iteratively modified to correct for the diode parasitics found with the simulation of the anodes.

More details on the simulation methods used for calculating embedding impedances for the diodes and the passive structure can be found in [8,16-18]. The method just described has been shown to produce multipliers with good agreement between measured and computed results and is the basis for much of the recent improvements in multiplier performance below one THz [7-10,17]. Figure 4 shows this agreement for a 200 GHz doubler (design described in [10], measurements and calculations performed at JPL). We are now confident that this design method can predict accurately multiplier performance up to 300 GHz, and we hope to get reasonably close to reality at even higher frequencies. However, many uncertainties remain above one THz, including assembly alignment, RF losses, fabrication tolerances for the waveguide block and the circuit, and diode physics.

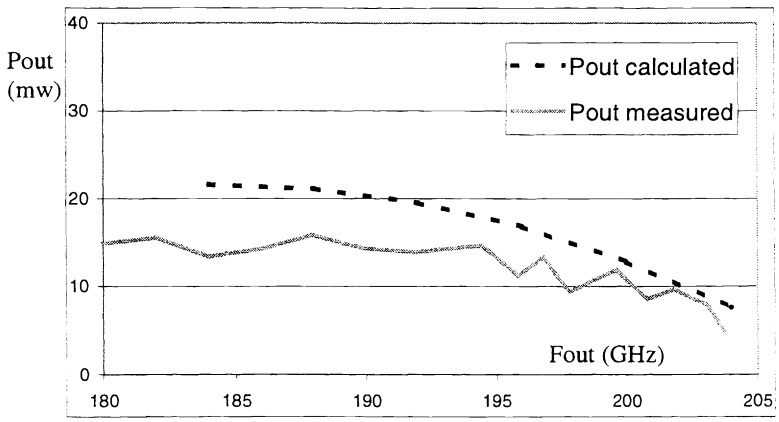


Figure 4 Comparison of measured and calculated performance of a 200 GHz balanced doubler designed by VMI [10].

3 MULTIPLIER DESIGNS AND PERFORMANCE

Multiplier designs which are currently being developed at JPL for four frequency bands are described below. These designs are aimed at the 200, 400, 1200 and 2400 GHz channels on FIRST (Table 1).

3.1 First and Second Stage Multipliers: High Power Doublers to 200 and 400 GHz

The 200 and 400 GHz multipliers have a balanced configuration, which has the advantage of providing natural separation of the input and output signals. Hence, the circuit requires only matching circuits and no extra filters for harmonic separation. The general operating principle is described in [21]. They are somewhat easier to realize because of the higher performance of the diodes at the lower frequencies, and because of the existence of prior experience on which to draw [7-10]. However, these are the stages which must operate at the highest input power. The 200 and 400 GHz doublers are designed to operate with input powers of 200 mW and 40 mW respectively. In order to handle the higher power levels without compromising efficiency, multiple diodes must be utilized. Therefore the 200 GHz stage uses an array of six anodes, and the 400 GHz uses four.

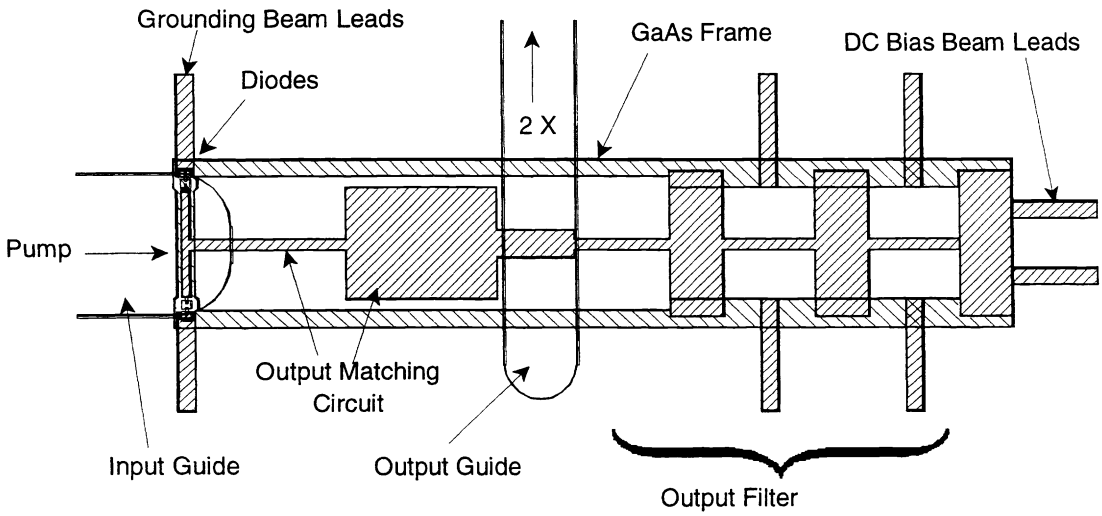


Figure 5 Layout of 200 GHz doubler (top view). The total length is just over 3 mm.

Since the diodes must operate at high input power levels, they have fairly large areas, and by consequence low impedance, which makes a broadband design more difficult because of the relatively large impedance transformation ratio needed between the diodes and the output waveguide. The designs shown here have been based upon the assumption that it is desirable to position the diodes in the input waveguide with most of the output matching circuitry close to the devices, hence the complicated structure between the waveguide probe and the diodes shown in Figure 5. The input impedance matching is accomplished in the input waveguide using the full to reduced height waveguide step, the backshort position and the diode geometry. The line extending across the output waveguide is an E-field probe, terminated on the right with a lowpass filter for DC bias. The diodes are grounded to the waveguide block with the two beam leads shown on the left. The beam leads, extending from the top and bottom of the GaAs frame, are included only to make handling and positioning of the circuit in the waveguide block easier. The filter is a high-low impedance type which, while large, is effective, straightforward to design and does not require any special processing or additional assembly steps. The beam leads at the right (coming off the bias filter metal) are bonded to any convenient insulating standoff, such as a rectangle of metalized quartz or a single-layer chip capacitor. From there a bond ribbon is connected to a DC connector for biasing the diodes.

The predicted performance of the design is shown in Figure 6. It rolls off sharply at the higher end of the band. A second, slightly broader band doubler design, was also implemented and the performance is shown in the figure.

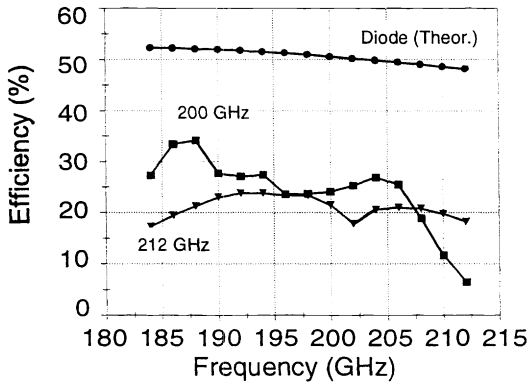


Figure 6 Predicted efficiency of 200 and 212 GHz doublers. Pin=200mW.

The 400 GHz circuit is a scaled version of the 200 GHz design but optimized for the higher frequency and different power levels. The actual fabricated circuit, without the waveguide block, and the simulated efficiency are shown in Figure 7. It is in this frequency range that the advantages of the monolithic fabrication technique become apparent. By integrating the device and the matching circuit together, concerns about the device placement with respect to the surrounding circuit are much reduced. Moreover, since the structure is now relatively large, handling and assembly are greatly simplified. The overall efficiency of the two doublers in series is expected to be better than 5 %. This should provide a 10 mW source at 400 GHz which can be used to drive higher stage multipliers.

Our experience in designing and laying out these circuits pointed to two areas in which the designs could be improved. First, the doubler chips are quite large. The filters take up about half of the circuit area. In the future a simple single layer capacitor mounted to the block on the DC bias side of the output waveguide will be used. This will be included in the simulation to verify that it has no adverse effect on the multiplier performance. It is also possible to integrate the bypass capacitor directly on the monolithic chip further simplifying the assembly process. This will be implemented in the next design iteration. Second, to reduce the complexity of the structure, some of the output matching can be performed using stubs near the diode, with the existing matching elements replaced by a single line going directly to the output guide. Output impedance matching can then be performed in the output waveguide, similar to the input.

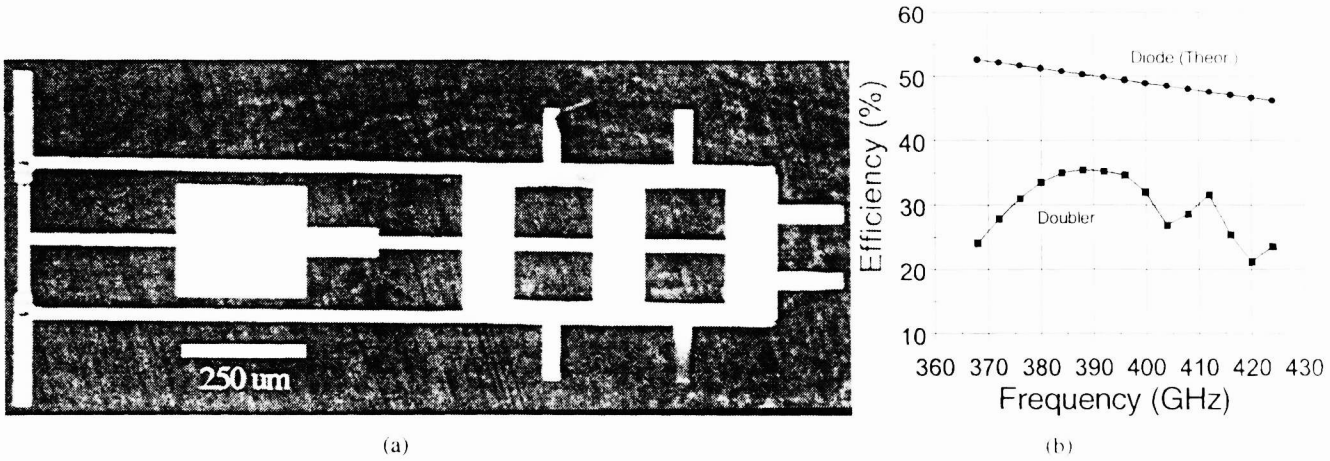


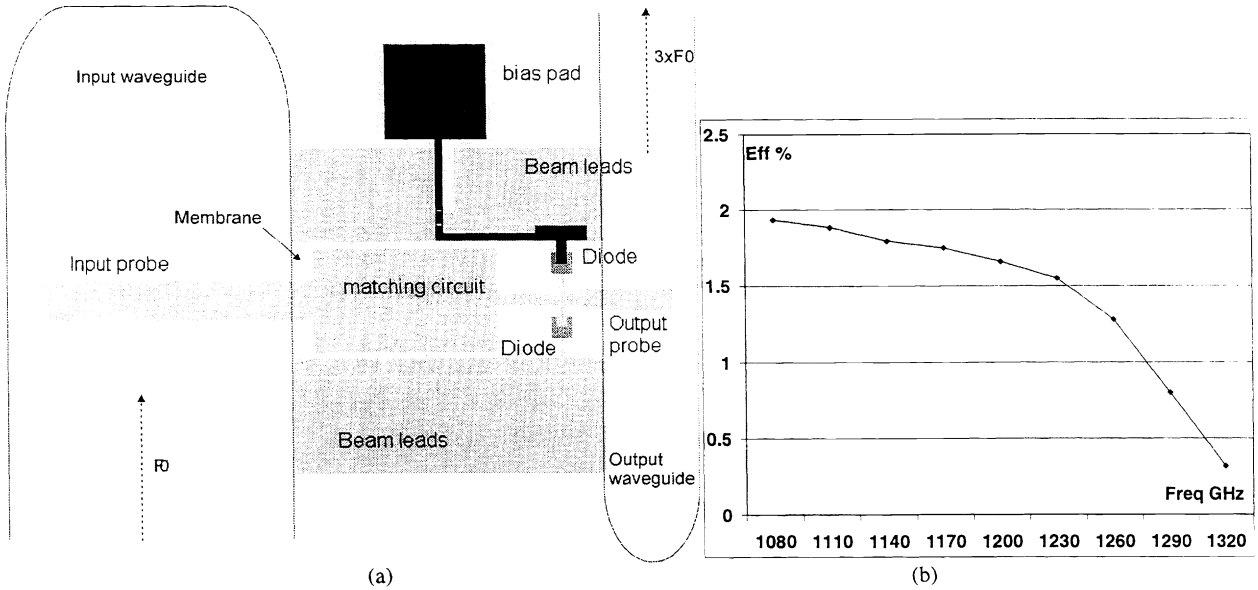
Figure 7 (a) Photo of realized 400 GHz doubler circuit (before assembly into waveguide block). Total length is about 1.5 mm. (b) Predicted efficiency of 400 GHz doubler.

3.2 Third stage multiplier: tripler to 1.2 THz

The tripler design to 1.2 THz uses a balanced configuration, where two diodes appear as anti-parallel for the odd harmonics (including the fundamental), and parallel for the even harmonics (Fig. 8a). This configuration has the advantage of confining the second harmonic idler to the diode loop, reducing the design complexity. The input and output matching circuit need to consider only first and third harmonics, and the required idler tuning can be performed in the diode loop. Such a configuration had been tried previously [20], with limited success. However, the difficult idler tuning optimization is now greatly facilitated by the availability of 3-D electromagnetic simulators.

Our circuit is implemented in coplanar waveguide which facilitates the biasing of the diodes, as they appear in series at DC. The idler tuning is accomplished by optimizing the length of the diode air-bridges. This approach has the advantage of making the circuit very simple, but has the drawback of reduced bandwidth. The extra inductance needed for tuning the second harmonic affects the third harmonic match, providing a highly inductive embedding impedance. The resulting matching circuit becomes fairly high Q, hence reducing the realizable bandwidth. However, in this specific case, we were able to compromise the efficiency slightly to achieve the desired bandwidth for FIRST (Table 1). The input and output signals are coupled to the waveguides by means of E-field probes. The diodes are matched to the probes using a very simple high-low impedance matching circuit. On the output side, this is reduced to the extreme of only one step. This is desirable to reduce loss, and increase the membrane mechanical stability The membrane is held in the inter-waveguide channel with the help of beam leads, clamped between the two halves of the split waveguide block. The bias is provided via a pad and a line running on one of the beam leads, while the other beam lead is shorted, providing the DC ground.

Using a full simulation of the waveguide and circuit structures together with an harmonic balance simulation of the diodes, we find an efficiency better than 1% over the required bandwidth for FIRST, and up to 2% in the lower part of the band (Fig. 8b). This result is for 10 mW input power, yielding an approximate output power of 100 μW over 1104 to 1272 GHz. A very strong roll-off is found at the upper end of the band. It is due to the appearance of higher order evanescent modes in the output waveguide, coming from the interaction with the circuit channel. The next iteration will resolve this problem and a relatively flat response across the design range is expected.



(a) (b)

Figure 8 (a) Sketch of the 1.2 THz tripler layout, and (b) its predicted efficiency with 10 mW input power.

3.3 Fourth stage multiplier: doubler to 2.4 THz

The doubler from 1.2 THz to 2.4 THz is designed to directly follow the tripler described above. In this case also we are using a balanced doubler configuration, which provides isolation between the input and the output of the circuit. The general operating principle is the same as for the two first stage doublers, and is described in [21]. In this design, the input signal is coupled directly to the diodes, whereas the output is coupled to the output waveguide by means of an E-field probe. The input matching is done entirely using the waveguide structure. The output matching is realized using different slot dimensions for the inter-waveguide channel, which changes the impedance of the coaxial line. A small open stub is used on the input side of the diodes to tune out some of the varactor capacitance. As with the tripler, the membrane is held in the block by two metal beam leads formed monolithically with the circuit and diodes. Figure 9 shows the final design and its calculated performance. Both the 1.2 THz tripler and the 2.4 THz doubler are currently in fabrication.

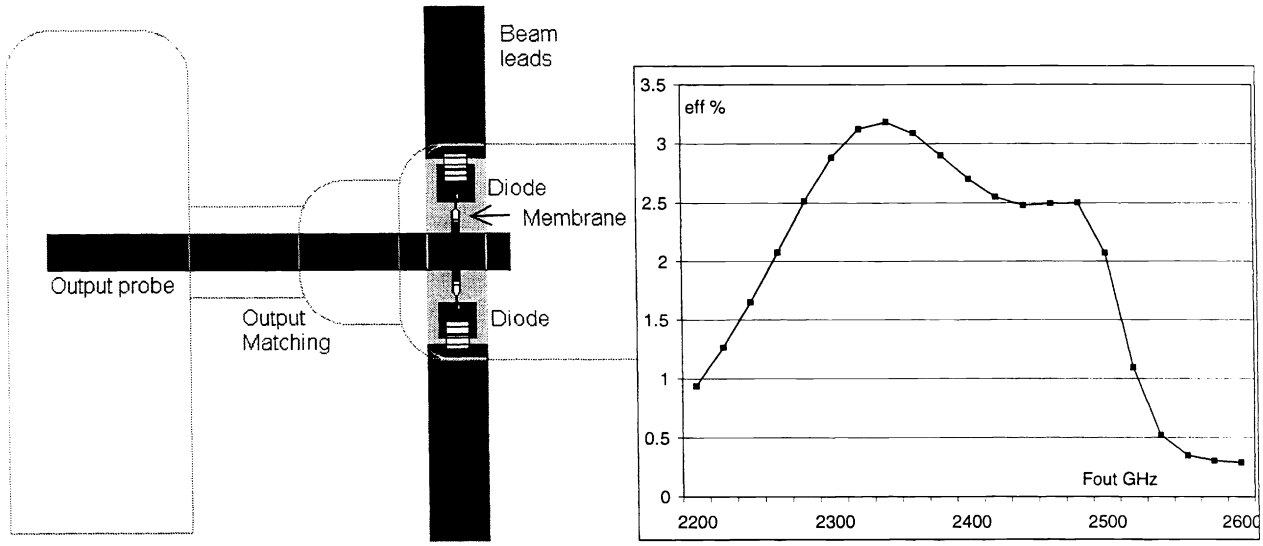


Figure 9 Sketch of the 2.4 THz doubler, and its calculated efficiency with 100μW of input power.

4 CONCLUSIONS

Building on recent advances in planar Schottky diode fabrication techniques, it is now possible to design and build planar multiplier stages at THz frequencies. Goals for the lower stage multipliers are high power handling capacity, large bandwidth and high efficiency. Higher frequency stages are designed using advanced integration techniques that provide more flexible, lower loss implementation. We have finished the design and performance calculations for two complete multiplier chains up to 1.2 and 2.4 THz, covering bands 5 and 7a of FIRST. The calculations show that it is possible to meet the instrument requirements, however many unknowns remain at the higher frequencies. Only measurements of these multipliers will tell us whether we can expect to actually realize the specifications. If successful, the present designs will be applied to the layout of a second iteration wafer for both the low and high frequency circuits. These two new wafers will contain all 16 required designs for realizing bands 5,6 and 7 on FIRST.

We have already learned much about multiplier design and fabrication processes in the course of this development effort. The next iteration of these circuits will see several important improvements including a more simplified layout for the matching structures and improved high frequency device and circuit modelling. In the longer term, other NASA and ESA missions will require very high frequency receivers. The technology and design approach presented here is expected to be the foundation of work on future Earth and planetary heterodyne remote sensing instruments such as NASA's Array Microwave Limb Sounder, VESPER, Cloud Ice and THz Limb Sounder, or ESA's MASTER/SOPRANO. However, we must be able to insure availability and continuity of the recently developed device fabrication technologies. We will also need to improve the circuit and device models so that less iterations are needed to realize desired performance, especially at the highest submillimeter wave frequencies. This requires progress on the high frequency device models, and more precise circuit characterization.

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