10.1149/1.2356305, copyright The Electrochemical Society

Design, Fabrication and Characterization of Parylene-Packaged Thin-Film Transistors

Hsi-wen Lo and Yu-Chong Tai

Micromaching Laboratory, California Institute of Technology, California, 91125, USA

A micro-fabricated parylene-packaged flexible pentacene thin film transistor is presented. Different from preceding devices that have been reported, this thin film transistor employs parylene as the substrate, the gate insulator and also the encapsulation layer. Also, this thin film transistor uses pentacene, an organic semiconductor with high mobility, as the active material. The transistor consists of Au/Cr gates and Au source and drain electrodes and takes a bottom-contact configuration. The freshly made thin film transistor shows a hole mobility of 0.084809 cm^2/V-s with an on-off ratio of 10^4.

Introduction

Vision loss due to retinitis pigmentosa (RP) and age-related macular degeneration (AMD) has troubled millions of people around the world. Recently, a retinal prosthesis has been developed for the treatment of aged-related blindness. This technology is based on the concept of replacing photoreceptor function with an electronic device (1). For this technology, a huge amount of electrodes are needed to achieve reasonable or high resolutions. A biocompatible and scalable high lead count electrode array for retinal prosthesis has been successfully fabricated (2). These electrodes are directly connected to the implanted control electronics through metal interconnects. As the resolution increase, the number of electrodes and interconnects increase, too. So is the volume of the implanted device. One way to reduce the number of metal interconnects and to satisfy the small volume constraint is to introduce a multiplexer into the system. This multiplexer has to overcome such difficulties as the corrosive environment and integration with the metal interconnects and so on.

One revolutionary approach to solve the problem is to explore biocompatible electronics that do not require conventional hermetic packaging and, at the same time, flexible enough for implantation use.

The combination of organic semiconductor and polymer substrate can serve this purpose. Pentacene ($C_{14}H_{22}$) thin film transistors (TFT) have been fabricated and possess a hole mobility up to 2.59 cm^2/V-s (3), which is comparable to the popular a-Si:H TFT technology.

Pentacene, however, is sensitive to oxygen, so unprotected pentacene transistors are vulnerable to even normal environments. It is therefore interesting to use parylene (readily a proven biocompatible material) as a pentacene-protecting polymer. Parylene C, a widely used MEMS (micro-electro-mechanical system) material, shows great flexibility (Young's modulus ~ 4 GPA), chemical inertness and biocompatibility (4). Parylene C has been recognized as a USP Class VI material and its intraocular biocompatibility has been

studied (2). In fact, parylene has been and is being studied for both encapsulation layer and even as a new gate insulator (5) (6). However, this work reports the first flexible parylene-pentacene electronics where parylene is exclusively used as the substrate, gate insulator and encapsulation layer.

Device Design

Our TFTs assume bottom-contact configurations. The schematic structure is shown in Figure 1. Pentacene is intolerant to exposure to solvents and other liquids (7). It has been demonstrated that the bottom contact configuration gives inferior performance to the top contact configuration for a range of deposition conditions and material thickness (8). However, the top contact configuration requires shadow masks, which introduces difficulties when integrating OTFT processes with standard photolithographic CMOS fabrication technology. We chose the bottom contact because of easy process integration. However, this brings up another problem, the contact resistance of source and drain. To reduce Au contact resistance, very thin Au (30nm ~50nm) without any adhesion layers is used (9). To further reduce contact resistance, we use large contact area. They are 4mm*1mm, 4mm*0.5mm, 1mm*1mm, 1mm*4mm, and 0.5mm*1mm (width/length). Mobility results of these transistors with different geometries of source/drain contacts are shown in the Table 1.

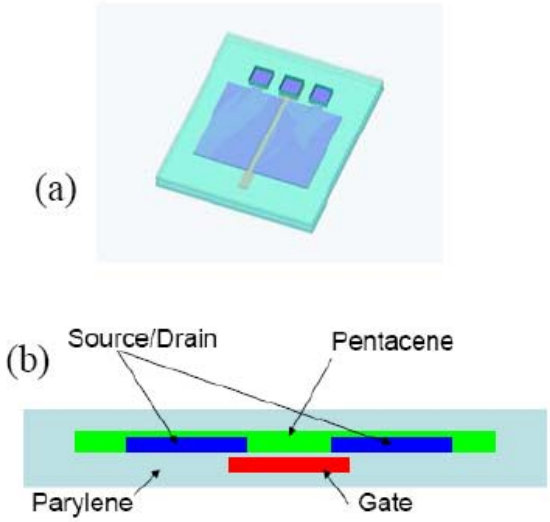


Figure 1. Isometric (a) and cross-section (b) views of bottom-contact configuration of parylene-packaged flexible pentacene TFTs

Device Fabrication

The basic technology involved in parylene-packaged pentacene TFT is the parylene/metal skin technology (10) (11). The simplified fabrication process is illustrated in Figure 2. The fabrication started with photoresist-coated wafers. A 10-μm parylene-C was first deposited as the substrate. A 1,500-angstron Au with 100-angstron Cr was thermally deposited and patterned to be the gate. A 0.1-μm parylene-C was then deposited as the gate dielectrics. Next, a 500-angstron Au was deposited and patterned as

the sources and drain. Then, a 200-nm pentacene (as purchased from Sigma-Aldrich) was thermally-evaporated under high vacuum. A 1-μm parylene-C was deposited as top-protecting layer. Finally, the whole parylene-pentacene TFTs was liftoff from the photoresist in a flexible MEMS form, shown in Figure 3.

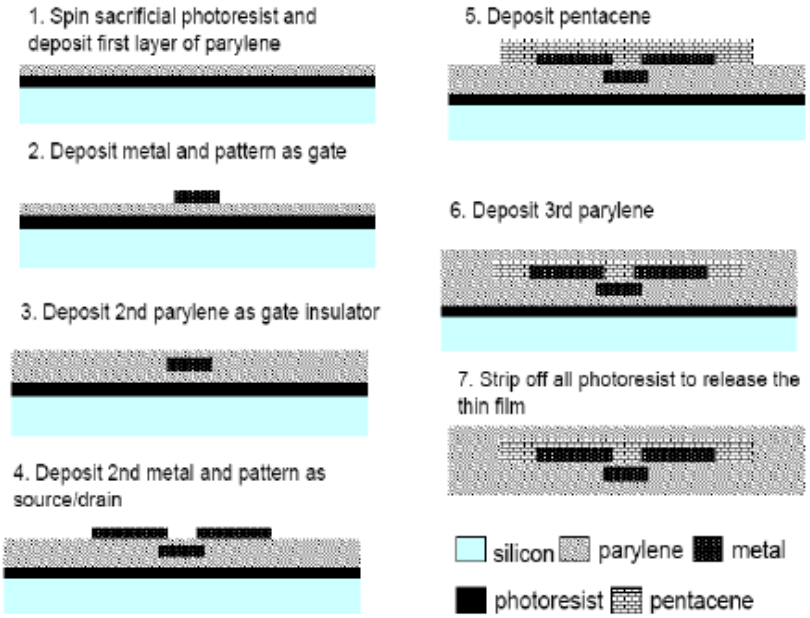
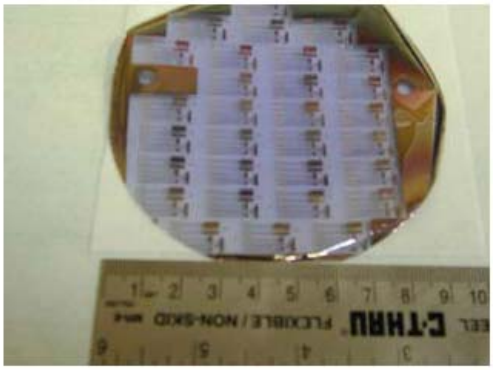
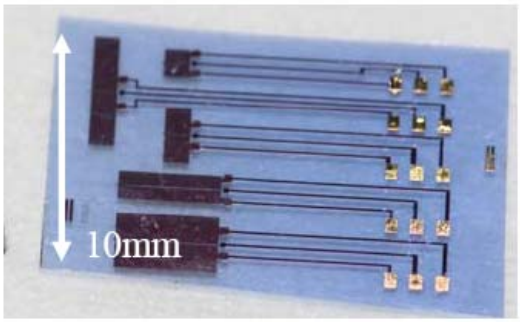


Figure 2. Simplified process flow.



(a)



(b)

Figure 3. Fabricated Parylene film containing pentacene thin-film transistors. (a) Released film (b) Closer view

Device Characterization

We obtained the drain and gate characteristics of the thin-film transistor with a probe station and the HP4145B semiconductor parameter analyzer. The transistor was measured at room temperature. The mobility of charge carrier (μ) in the saturation regime can be calculated from the drain current given by the equation.

$$I_D = \frac{1}{2}\mu C_i \frac{W}{L}(V_{GS} - V_T)^2 \quad [1]$$

Take square root of both sides.

$$\sqrt{I_D} = \sqrt{\frac{C_i W}{2L}}\mu(V_{GS} - V_T) \quad [2]$$

Solving this equation and use a definition of "k" as

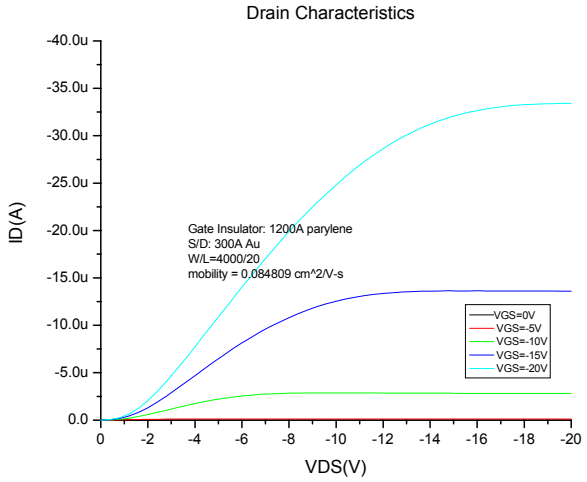
$$k = \sqrt{\frac{C_i W}{2L}}\mu \quad [3]$$

$$\mu = \frac{2L}{WC_i}k^2 \quad [4]$$

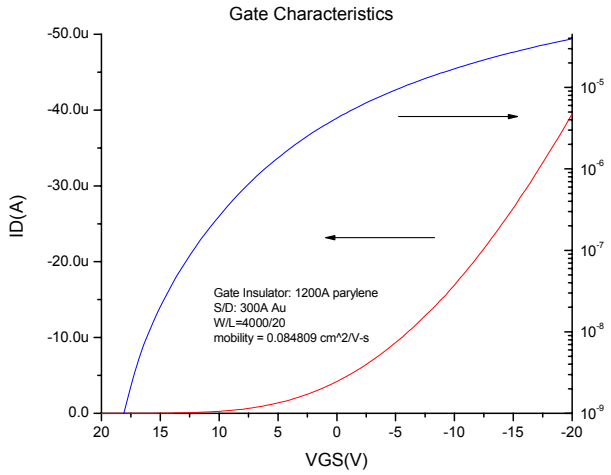
Equating the slope of the plot $\sqrt{I_D}$ versus V_G to "k" determines the μ in the saturation regime.

As mentioned before, we have fabricated OTFTs with source and drain electrodes of different geometries. The mobility results are show in Table 1. From these values, the mobility does not vary a lot for different sizes of source/drain electrodes. However, transistors with too small source/drain electrodes show poor performance, according to our previous observations.

The best transistor we fabricated shows a mobility of 0.084809 cm^2/V-s with an on-off ratio of 10^4. Its drain and gate characteristics are shown in Figure 4.



(a)



(b)

Figure 4. Drain (a) and gate (b) characteristics of the fabricated transistors. W/L=4000um/2000um

TABLE 1. Mobilities of transistors with different source/drain electrode area (cm^2/V-s).

sets\area	4mm*2mm	4mm*0.5mm	1mm*1mm	1mm*4mm	1mm*0.5mm
Set01	0.058707	0.05208	0.046192	0.049484	0.050826
Set02	0.05067	N. A	0.047853	0.050902	0.062866
Set03	0.060771	0.065774	0.062914	0.067255	0.065339
Set04	0.06093	0.061961	0.057696	N. A.	0.051044
Set05	0.047353	0.045827	0.047425	0.050727	N. A.
Set06	0.050896	N. A.	0.050609	0.049328	0.055986
Set07	0.044969	0.042931	0.042062	0.049058	0.047858

Conclusion

We fabricated parylene-packaged pentacene thin-film transistors with fully MEMS-compatible parylene thin-film technology. The pentacene thin-film transistors use parylene as the substrate, the gate dielectric and the encapsulation layer, and take the bottom contact configurations. The fabricated pentacene thin-film transistor has a mobility of 0.084809 cm^2/V-s with an on-off ratio of 10^4. Further bio-implantation tests are underway.

Acknowledgements

The authors would like to thank Mr. Trevor Roper for his assistance with equipment and fabrication. We would also thank Tanya Owen, Christine Matsuki and other members of the Caltech Micromachining Laboratory for their assistance.

References

1. Humayun, M.S., “Intraocular retinal prosthesis”, Tr: Am Ophth Soc, **99**, 2001.
2. D. C. Rodger, J.D.W., M.S. Humayun, and Y.C. Tai, “Scalable Flexible Chip-level Parylene Package for High Lead Count Retinal Prosthesis”, Transducer. 2005.

3. S.C. Lim, S.H.K., J.H. Lee, H.Y. Yu, Y. Park, D. Kim and T. Zyung, "Organic thin-film transistors on plastic substrates", Elsevier Materials Science and Engineering B, **121**, pp211-215, 2005.
4. Wolgemuth, L., "Assessing the performance and suitability of parylene coating", Medical Device & Diagnositic Industry, **22**: p. 42-49. 2000
5. I. Kymissis, C.D.D., and S. Purushothanman, "Patterning pentacene organic thin film transistors", Journal of Vacuum Science & Technology, **B 20-3**: p. 956-959, 2002
6. D. Feili, M.S., T. Doerge, S. Kammer, and T. Stieglitz, "Encapsulation of organic field effect transistors for flexible biomedical microimplants", Elsevier Sensors and Actuators, A, **120**: p. 101-109. 2005
7. D. J. Gundlach, T. N. Jackson, D. G. Schlom, and S. F. Nelson, "Solvent induced phase transistion strain relaxation in thermally evaporated pentacene films", Appl. Phys. Lett, **74**, p3302, 1999
8. F. Garnier, F. Kouli, R. Hajlaoui, and G. Horowitz, "Tunneling at organic/metal interfaces in oligomer-based thin-film transistors", MRS Bull., pp52-56, June, 1997
9. N. Yoneya, M. Noda, N. Hirai, K. Nomoto, M. Wada, and J. Kasahara, "Reduction of contact resistance in pentacene thin-film transistors by direct carrier injection into a-few-molecular-layer channel", Appl. Phys. Lett, **85**, #20, 2004
10. M. Liger, N.P., Y.C. Tai, S. Ho and C.M. Ho. Large-area electrostatically-valved skins for adaptive flow control on ornithopter wings. in Technical Digest, Solid State Sensor and Actuator Workshop. 2002. Hilton Head Island, South Carolina, USA.
11. Y.C. Tai, F.J., Y. Xu, M. Liger, S. Ho and C.M. Ho. Flexible MEMS skins: technologies and applications. in Proceedings, Pacific Rim MEMS Workshop. 2002. Xiamen, China