MMIC Low-Noise Amplifiers and Applications above 100 GHz

R. Lai(1), T. Gaier(2), M. Nishimoto(1), S. Weinreb(2), K. Lee(2), M. Barsky(1), R. Raja(1), M. Sholley(1), G. Barber(1), D. Streit(1)

(1): TRW One Space Park, Redondo Beach, CA, 90278
(email Richard.Lai@trw.com)

(2): JPL Microwave, LIDAR, Pasadena, CA, 91109
(email Todd.C.Gaier@jpl.nasa.gov)

ABSTRACT

In this paper we will present recent work on low noise amplifiers developed for very high frequencies above 100 GHz. These amplifiers were developed with a unique InP-based HEMT MMIC process. The amplifiers have been developed for both cryogenic and room temperature amplifier applications with state-of-art performance demonstrated from 100 GHz to 215 GHz.

INTRODUCTION

The frequency range above 100 GHz is fertile for next generation applications in telecommunications and radars as well as the fields of radio astronomy, Earth remote sensing, planetary exploration and millimeter-wave imagers. Working at these higher frequencies offers the advantages of broad available bandwidth, reduced aperture and instrument size, and a higher density of observable spectral lines. Advanced high frequency MMIC technology is uniquely suited to circuit fabrication above 100 GHz due to reduced parasitics and interconnections. Recent demonstrations in MMIC low noise amplifier and power amplifier technology above 100 GHz have enabled a new generation of instruments. In this paper we will discuss the development and performance of several first of a kind amplifiers for applications including microwave atmospheric sounding and radio astronomy.

DEVICE AND PROCESS DESCRIPTION

The device performance necessary to achieve usable gain and noise figure for low noise amplifiers operating at frequencies between 100 to 200 GHz requires very high device transconductance above 1000 mS/mm, cutoff frequencies above 200 GHz and maximum oscillation frequencies above 400 GHz. To achieve usable gain and sufficient MMIC design margin, the device must exhibit a maximum available gain of 7-8 dB per stage up to 200 GHz. InGaAs/InAlAs/InP HEMTs are the only three terminal devices that have demonstrated performance at these levels[1-4].

In developing a MMIC process for this frequency range, three significant process enhancements were implemented on TRW's baseline 75 nm diameter 0.1 um gate InP HEMT process[5-6]. The first is the growth and design of pseudomorphic high indium composition InGaAs channels. Cutoff frequencies of 300 GHz have been achieved at the highest indium compositions greater than 70%. The 2nd process enhancement was the reduction of the gate length from 100 nm to 70 nm. 15-20% improvement in cutoff frequency and transconductance was observed in the shorter gate length devices compared to the baseline 100 nm devices with similar gate finger yield. The third area is the development of a 50 um thick substrate with very small through substrate grounding via holes. This process prevents substrate waveguide mode propagation and allows for minimal device source inductance to maximize device gain at high frequencies. TRW has established this enhanced MMIC process with an eye towards future production capability. Good MMIC yield and repeatability for this process have already been demonstrated on several wafer lots. The development of a robust InP MMIC process has been a critical key to the first-pass design success of the variety of MMIC amplifier designs shown in this paper.

AMPLIFIER DESCRIPTION AND PERFORMANCE

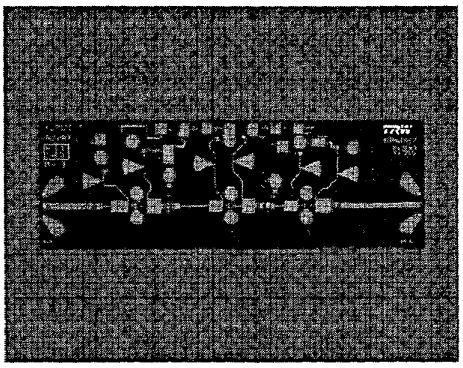

Figure 1. Photograph of a 3-stage single ended 112-118 GHz MMIC LNA

In order to establish amplifier performance and optimize the designs, it is critical to obtain test data at

these high frequencies. A series of waveguide frequency extenders for network analysis covering the range 50-220 GHz has been developed for this effort. In addition, wafer probes operating up to 220 GHz have been employed to obtain s-parameter data. Noise measurement capability has also been developed at frequencies as high as 200 GHz, as well as solid-state noise sources operating 180 GHz, which has enabled the first meaningful on-wafer noise measurements in this band. The data achieved from on-wafer measurements has also been duplicated with fixtured amplifier measurements.

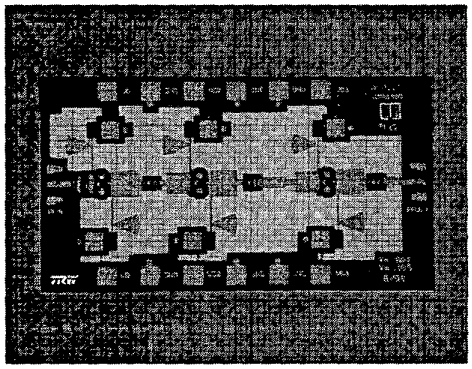

Figure 2. Photograph of 3-stage single ended 165-190 GHz MMIC LNA

A series of amplifiers has been demonstrated in the frequency range of 100 – 215 GHz. In the frequency range 85-110 GHz, a CPW low noise design uses four stages to achieve 20-25 dB gain and a module noise performance of 3-4 dB. Under cryogenic operation these amplifiers perform with 30-40K noise temperature (~0.5 dB NF). A three-stage microstrip amplifier covering the frequency range 112-120 GHz has 15 dB gain with a noise figure of 4-5 dB (Figure 1).

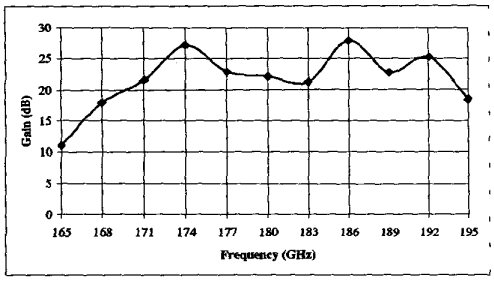

Figure 3. Fixtured 165-195 GHz amplifier including a 3-stage single ended MMIC LNA cascaded with a 4-stage balanced LNA.

A three-stage microstrip amplifier design demonstrated 14 dB gain and a noise figure of 7 dB from 165 GHz to 190 GHz (Figure 2). To demonstrate a usable front-end amplifier, two MMIC amplifiers were cascaded to achieve 20-25 dB gain from 170-190 GHz. The first MMIC was the same as shown in Figure 3 (3-stage single ended amplifier) and this was cascaded with a 4-stage balanced amplifier. 7.5 dB noise figure average was measured across the band for this amplifier. All of these measurements were made flange to flange. Special care was taken to minimize upfront losses associated with the waveguide transition and ribbon bond.

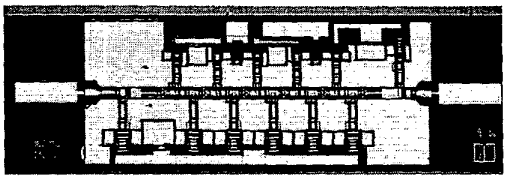

Figure 4. Photograph of 6-stage single-ended 160-215 GHz MMIC LNA

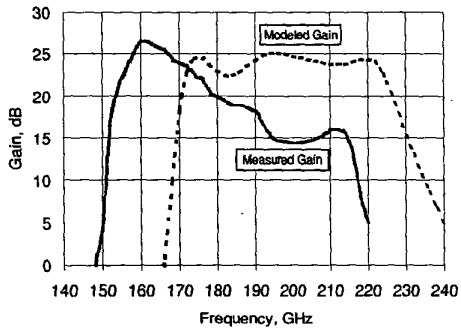

Figure 5. Measured vs. Modeled Gain Plot for the 160-215 GHz MMIC LNA

A 6-stage CPW design covering the frequency range 160-215 GHz has 15-27 dB gain with a measured module noise figure of 8 dB at 170 GHz (Figure 4,5). A measured 15 dB gain at 215 GHz is the highest frequency gain amplifier demonstrated to date. Further state-of-art amplifer demonstrations are shown in Table 1. The presentation will also include more detail on the MMIC design and performance described in this paper, the on-wafer testing techniques for MMIC screening and the challenges in designing 100+ GHz MMICs and modules (EM and modeling issues, techniques). We will also present the latest state-of-art results as they are available for dissemination at the time of the conference.

Freq. (GHz)	LNA Description	Noise Figure	Gain
100-110*	4-stage LNA (cooled to 20K)	0.5 dB	20-22 dB
112-120*	3-stage single ended LNA	3.9 dB	16-18 dB
139-142	2-stage single ended LNA	5.8 dB	8-10dB
150-157	3-stage single ended LNA	5.1 dB	9-12 dB
165-190	3-stage single ended LNA	7.0 dB	13-15 dB
160-215	6-stage single ended LNA	8.0 dB	15-27 dB

Table I. TRW's state-of-art InP HEMT MMIC low noise amplifiers >100 GHz

CONCLUSION

In conclusion, we have described our development of low noise amplifiers above 100 GHz using a 0.07 um InP HEMT MMIC process on 50 um thinned InP substrates. This process has been used to establish a family of first-of-a-kind amplifiers that push the frontier in future remote sensing and communication applications. Much work remains in this area and they include establishing a production worthy process, further device enhancements, stabilization of device models, novel design techniques, packaging challenges and improved testing techniques at these high frequencies.

ACKNOWLEDGMENTS

The authors would like to acknowledge Lorene Samoska and other technical members from JPL, Sam Esparza, Bruce Osgood, for on-wafer and fixture testing of wafers and parts, Liem Tran, Rosie Dia, Rita Rodriguez and members of the fabrication team for InP wafer fabrication. We would like to acknowledge Barry Allen for the advice and guidance for this work. We would like to acknowledge the several key MMIC designers for their contribution including T.W. Huang, Yon-Lin Kok and Huei Wang.

BIBLIOGRAPHY

[1] P. D. Chow et. al, "W-band & D-band Low Noise Amplifiers Using 0.1 μm Pseudomorphic InAlAs/InGaAs/InP HEMTs", Proc. 1992 Int. Microwave Symp., Albuquerque, NM p. 807.

[2] M. Wojtowicz et. al., "305 GHz fT Using 0.1μm Gate-Length Graded Channel Pseudomorphic InxGa1-xAs/In0.52Al0.48As HEMTs", IEEE Electron Device Letters 1994, p. 477

[3] K. H. Duh et. al., "A Super Low-Noise 0.1 μm T-gate InAlAs/InGaAs/ InP HEMT", IEEE Microwave and Guided Letters., 1991 p. 114.

[4] L. D. Nguyen et. al. "650Å self-aligned gate pseudomorphic AlInAs/GaInAs HEMTs", IEEE Electron Device Lett., 1993, p. 143

[5] H. Wang et. al., "Fully passivated W-band InGaAs/InAlAs/InP monolithic low noise amplifiers", IEEE Proc. Microwave, Antenna & Propagation, 1996

[6] R. Lai et. al., "A High Performance and Low DC Power V-band MMIC LNA Using 0.1 μm InGaAs/InAlAs/InP HEMT Technology", IEEE Microwave Guided Letters, Dec. 1993, p 447.