

On the Stability of Millimeter-Wave Power Amplifiers

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Abstract — In this paper, we discuss issues affecting high-frequency power amplifier stability. Two methods for simulating K -factor stability in a monolithic millimeter-wave integrated circuit (MMIC) power amplifier will be discussed. Both methods will be used to predict the occurrence of millimeter-wave oscillations (Ka-band and above) in a W-band power amplifier. We present experimental results confirming the simulation data, and discuss how the methods may be applied to eliminate instabilities in MMIC power amplifiers.

I. INTRODUCTION

Millimeter-wave power amplifiers are increasingly in demand for higher bandwidth communication, local oscillator sources, automotive radar, and fiber optic communication [1,2]. As the need for higher frequency power amplifiers increases, some design issues affecting power amplifier stability become important. In the case of a 100 GHz monolithic millimeter-wave integrated circuit (MMIC) power amplifier, oscillations which occur at low frequencies (lower than a few GHz) may be easily treated off-chip with proper terminations or bypass capacitors, but oscillations occurring at 10-50 GHz must be corrected with a new MMIC design and costly fabrication run.

Often, instabilities in amplifiers can be lived with, and if they are of small-amplitude, may be tolerated. However, with increasing interest in satellite communications or spacecraft flight of MMIC chips, reliability and lifetime are critical performance issues and oscillations must be eliminated. In this paper, we outline stability analysis applied to W-band (75-110 GHz) MMIC power amplifiers, and give some general guidelines for designing for amplifier stability out of band. A 71-84 GHz MMIC power amplifier with an observed oscillation at 33 GHz is used for a case study. The analysis and experimental results matched quite well. Furthermore, based on the design guidelines, the 33 GHz oscillation was successfully removed.

II. DESCRIPTION OF PROBLEM

In Figure 1 we show a two-stage, 71-84 GHz MMIC power amplifier, of similar type as those in [2], fabricated by TRW using a 2 mil thick, 0.1 μm GaAs PHEMT process. The design topology makes use of 4-way and 8-way microstrip power combiners to combine the FETs. The photograph indicates the two stages and the 8-parallel FETs combined in Stage 2. The combiner utilizes odd-mode suppression resistors placed between the FETs. This type of cell is common for combining large devices in parallel to achieve more power.

When we packaged the chip in a waveguide module, we observed some oscillation phenomenon which was difficult to control with off-chip stabilizing networks. The oscillation behavior was transient, and occurred over a range of drain voltages, but disappeared if we biased the amplifier above $V_d = 3$ V. The behavior, while we could work around it, warranted further investigation.

We tested the amplifier chip with a spectrum analyzer, using GGB industries wafer probes at the input and output of the chip, and applied DC bias with DC needle probes. The output RF probe was attached to a 2.4 mm coaxial cable and fed into a DC-40 GHz spectrum analyzer. We observed that a transient oscillation was present between 32-34 GHz, for drain voltages up to 2.9 V. The spectrum with the 34 GHz peak is shown in Figure 2. The peak varied from 32-34 GHz depending on gate voltage. Our investigation into the nature of the oscillation revealed that it was convincingly coming from the second stage of the MMIC chip (it remained whether stage 1 was turned on or

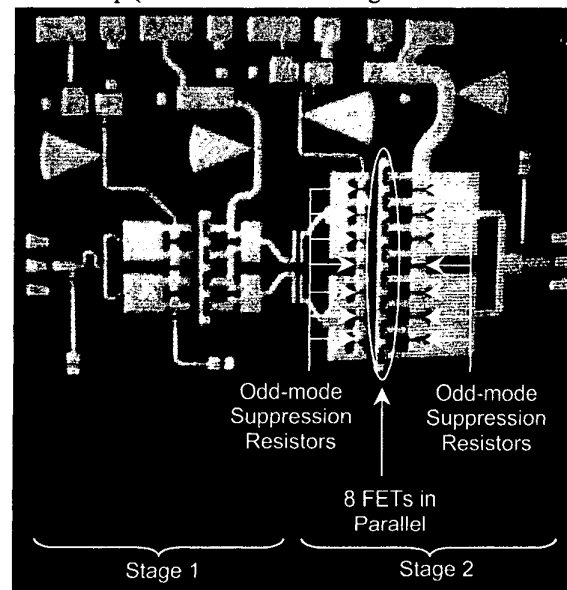


Figure 1. Chip photograph of two-stage amplifier to be analyzed. Side arrows at left and right indicate positions of odd-mode suppression resistors which separate each FET, on both the gate and drain side of stage two. The bottom arrow indicates the column of 8 FETs in parallel.

off), and occurred for no applied RF signal (only DC bias). Also, it was not dependent on whether the input was terminated or left open. This work describes the analysis we have performed on the MMIC design into the nature of the oscillation, and the methods we have used to correct the oscillation. These methods can be applied to all types of high frequency MMIC amplifiers to guarantee stability in a MMIC design.

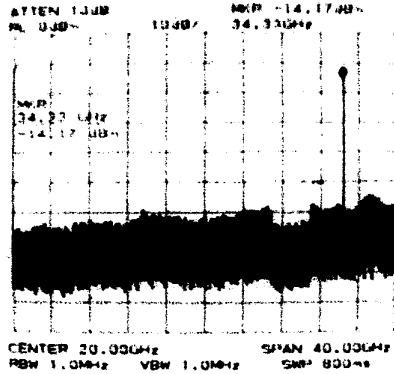


Fig. 2. Spectrum of chip showing 34 GHz oscillation.

III. METHODS OF STABILITY ANALYSIS

Two-port small-signal simulations of the amplifier chip between the RF input and RF output revealed no special anomalies between 0-150 GHz, while the in-band stability factor, K , was greater than 2 between 60-85 GHz. In addition, the stability condition of each stage was carefully investigated to ensure that there was no overlap between the stability circles of one stage with the source mapping circles of the other stage. We therefore investigated two other ways to simulate the circuit, to make the experimentally-verified oscillation at 32-34 GHz appear in the simulations.

We have performed two types of stability analysis in this work. We focused our simulations on the second stage of the chip, since experimentally it appeared responsible for the oscillation. First, we performed a K -factor analysis using the bias lines in each stage of the amplifier chip as ports, as shown in Figure 3, according to reference [3]. The RF input and output of the circuit are terminated in 50 Ohms, while ports are inserted at the bias lines of the

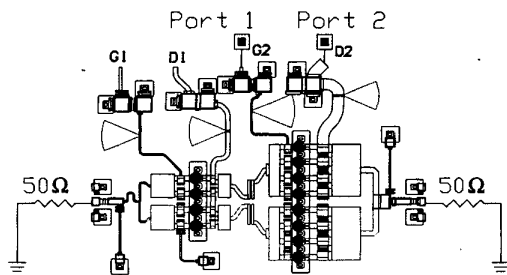


Figure 3. Configuration for simulated K -factor analysis using the second stage bias lines as ports (after Ref 3).

circuit. Port 1 is applied to the gate bias line while Port 2 is applied to the drain bias line. The figure illustrates this for the bias-line analysis of the second stage. This method is usually applied to low frequency oscillations < 2 GHz, but it is equally applicable to higher frequencies as well.

The second method we used to detect the instability in simulations was to apply a push-pull analysis to the second stage of the circuit, shown in Figure 4. In this method, the circuit is broken strategically at a point where the power is to be split into two legs, and an ideal transformer is inserted. The transformer serves to drive the two legs of the power splitter 180 degrees out of phase, thereby forcing an odd-mode condition. The transformer is applied at the input and output of the split circuit. Figure 4 shows the setup of the problem in the linear simulator, and the K -factor is calculated between the input and output of *only* stage 2. The bias circuitry above the radial stubs is not shown in the figure, although it is simulated. The push-pull analysis is another way to simulate odd-mode oscillations, which have been investigated previously using a different procedure [4,5].

In order to make the instability more obvious in the simulations, we enhanced the value of transconductance, G_m , to twice its nominal value for the simulations to follow. Although this is a relatively high value to use, such a theoretical exercise is more likely to make potential instabilities appear, and then correcting the circuit for large variations in G_m will make it more immune to undesired problems. We were also interested in running the circuit at sub-room-temperature operation, and had observed an increase in G_m and circuit gain upon cooling, and wanted to have sufficient margin for stability in our analysis. In addition, one could also vary other device parameters in the model to check for instabilities. One possibility is to vary the C_{gs} and C_{gd} by about 40 %, since these parameters also vary with changing bias conditions considerably.

IV. SIMULATION RESULTS

First, we applied the bias-line analysis (from Figure 3) to calculate the K -factor of the stage 2 bias lines with the enhanced value of G_m . The full spectrum to 150 GHz is not plotted here, however, we observed that the K -factor appeared relatively benign *except* in the region of 30-35 GHz. In this area, a sharp dip in K -factor was observed around 32.8 GHz, indeed, at one of the experimentally measured frequencies. The plot is shown in Figure 5a.

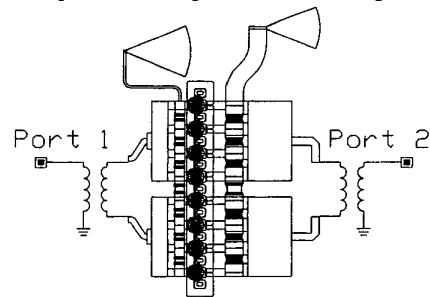


Figure 4. Configuration for simulated push-pull analysis of the second stage of the MMIC power amplifier.

Figure 5b shows the results of a push-pull analysis (from Figure 4) on the second stage of the same chip. A sharp spike in K -factor at 32.5 GHz is also observed. Our analysis has shown that a dip in K -factor appeared at 32-33 GHz in both simulations, in agreement with the experimentally identified oscillation between 32-34 GHz, and despite the fact that $K > 1$ everywhere in the simulation data of the whole chip from RF input to RF output.

V. ELIMINATION OF UNDESIRABLE OSCILLATIONS

With sensitive simulations it is possible to trace the cause of the Ka-Band oscillation and remedy it. We have found that the oscillation was due to an improper value of odd-mode resistors, as well as placement of the odd-mode resistors too far away from the PHEMTs (see Figure 1). By judiciously choosing the odd-mode resistor value to

more closely match the input impedance of the PHEMT (~5 Ohms), we were able to eliminate the oscillation condition in simulation. The optimum value of odd-mode resistor was found to be 10 Ohms, and it had to be placed within 40 μm s of the PHEMTs in order to be effective. With these changes to the second stage of the circuit, we achieved the simulation data in Figures 5c and 5d. Figure 5c shows the bias-line analysis and Figure 5d shows the push-pull analysis, with $R=10$ Ohms instead of 50 Ohms, and with the odd-mode resistors placed 10 μm closer to the PHEMTs. In both cases, the potential region of instability has disappeared, and has not reappeared at any other frequency. We next present experimental data on the redesigned amplifier chip, showing that the instability has indeed been eliminated up to 40 GHz.

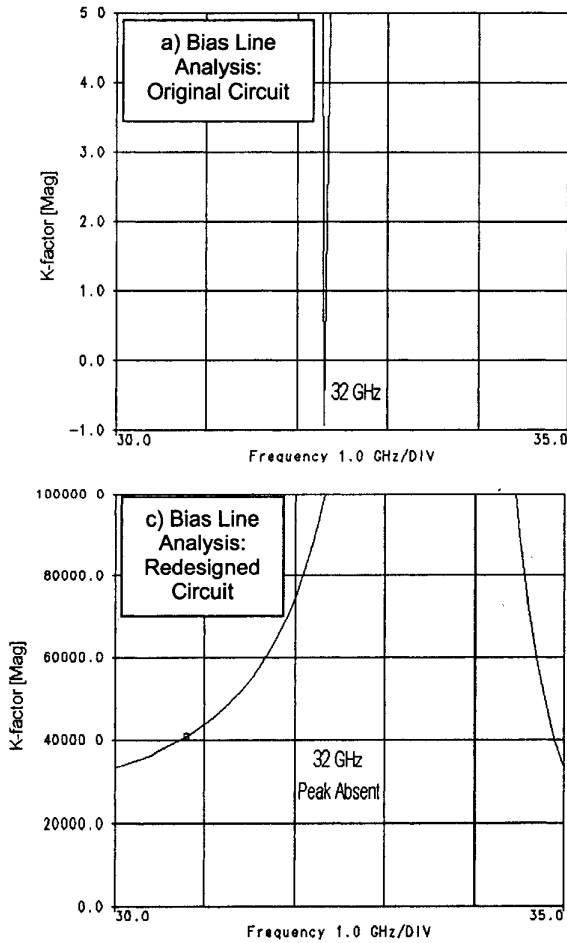


Figure 5a.(Top) Simulation of the K -factor between the gate and drain bias lines of stage 2; 5c (Bottom): Simulation of the K -factor between the gate and drain bias lines after decreasing the value of odd-mode suppression resistors and moving the resistors closer to the FETs. Note the scale of K (0 to 100000).

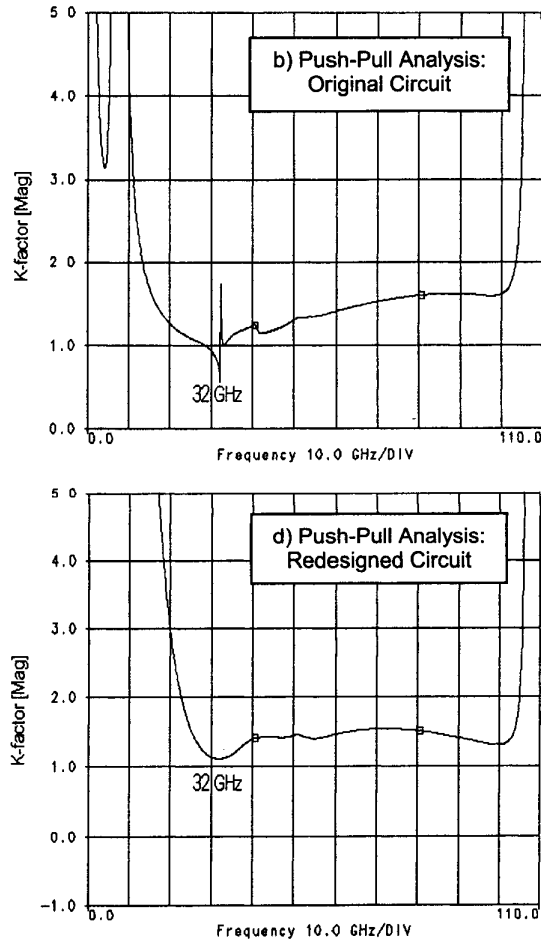


Figure 5b (Top) Simulation of K -factor of pushpull analysis of stage 2; 5d (Bottom): Simulation of K -factor in pushpull analysis of stage 2, after decreasing the value of odd-mode resistors, and moving the resistors closer to the PHEMTs.

VI. EXPERIMENTAL RESULTS

The MMIC chip was redesigned according to the simulations, to have smaller-valued odd-mode resistors, and fabricated alongside the original chip design. Two types of data were obtained for the stability measurements: spectrum analyzer data up to 40 GHz, and small-signal S-parameters were obtained using an HP 8510A vector network analyzer with Oleson Microwave Labs extension modules covering WR15 (50-79 GHz). All of the data were obtained via on-wafer measurements with RF wafer probes.

While Figure 2 showed the 34 GHz oscillation in the original circuit, Figure 6 illustrates the clean spectrum obtained from the redesigned MMIC. No oscillation at 32-34 GHz was observed in the new circuit under any bias condition. As in Figure 2, $V_d=1.5$ V, and $V_g=-3$ V.

Small signal V-band S21 measurements of the original circuit and the redesigned, "fixed" circuit are shown in Figure 7. The original circuit exhibits a spike in the S21 data at 67 GHz, $2 \times (33.5$ GHz). We believe this to be the second harmonic of the 32-34 GHz oscillation. The "fixed" circuit exhibits no such spike, and also has about 2 dB higher gain since the oscillation has been eliminated. Gain and drain current were suppressed in the original circuit due to the oscillation.

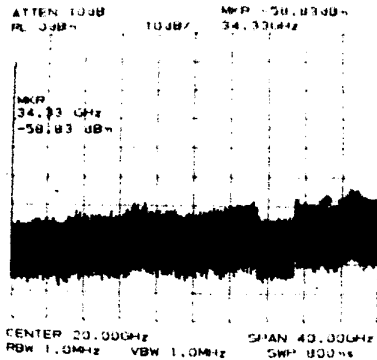


Figure 6. Spectrum of redesigned amplifier chip, showing elimination of the 34 GHz oscillation at all bias conditions.

VII. CONCLUSION

We conclude by stressing that stability analysis in the band of interest is insufficient to guarantee stable operation for very high frequency MMIC amplifiers. Out of band stability must be analyzed, especially in the case of power-combined transistors where odd modes are possible. Even when a two-port, input-output K -factor analysis may look sufficient to guarantee stability, checking the bias-line stability as well as a push-pull analysis is important in power-combined cells, where several modes are possible. We have outlined two methods

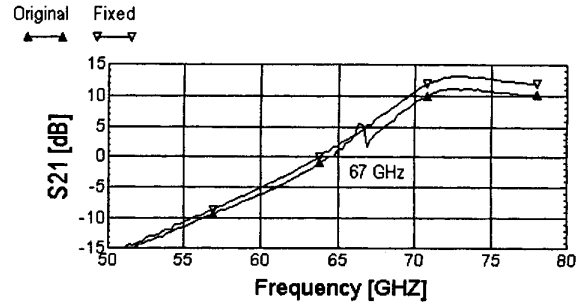


Figure 7. V-band S21 measurements of original chip (dark triangles), showing gain spike at the second harmonic of 33.5 GHz, and the "fixed" chip (light triangles), with no spike. Gain is also enhanced in the fixed chip.

for analyzing circuits for stability, as well as indicated parameters which may be varied to make a potential instability appear in simulations, and used these methods to correct an existing instability in Ka-Band which was difficult to detect in conventional simulations. Future work could involve large signal S-parameter measurements and K -factor analysis for stability.

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