EMPIRICAL LOAD-LINE CAPACITANCE MODELS FOR HEMT

Y.C. Leong[1] and S. Weinreb[2]

[1]U. of Massachusetts, 619 Lederle GRC, Amherst, MA 01003
[2]Jet Propulsion Laboratory, 4800 Oak Grove Drive, Pasadena, CA 91109-8099

ABSTRACT

Models for describing the gate-source and gate-drain capacitances' variation along resistive load line have been proposed. They are charge conservative and consistent with small-signal model at bias points along the load line. Extraction procedure for the models' parameters is fast and intuitive. The *models can be implemented easily in most* circuit simulator programs.

INTRODUCTION

The gate-source and gate-drain capacitances of HEMT have long been determined to have dual voltage dependency. Expressions for these capacitances as functions of two voltages have been published. However, small-signal linearization of the charge functions that are derived from these capacitance functions will introduce transcapacitances [1]. These extra elements cause discrepancy between the large-signal and small-signal models. A recent transistor model proposed in [2] is consistent and charge conservative. However, it requires a new topology for the intrinsic small-signal equivalent circuit model. Very often, the constant capacitance or junction capacitance models are still used. But in these two cases, variation of the capacitances with output voltage swing is not modeled.

MODEL DESCRIPTION

In this paper, empirical models for the gate-source and gate-drain capacitances will be proposed. These models have only single voltage dependency and they track the capacitances' variation along a resistive load line in the IV plane of the HEMT. In this way, the influence of the output voltage on the capacitances can be modeled by using only the local voltages of the capacitors. They are charge conservative and the nonlinear model will be consistent with the common small-signal model at bias points that are along a resistive load line in the IV plane.

The extraction procedure for the models' parameters is straightforward and can be done using commonly available spreadsheet programs. As the capacitance functions are only one dimensional, the time needed to extract the capacitance models is very fast and the fitting is of good accuracy. The models also give an intuitive picture of the behavior of the FET during large-signal excitation since fitting is done directly with the measured capacitances' variations instead of the S-parameters.

These models can be implemented easily in most circuit simulators as simple charge sources across the capacitors' terminals or as single-voltage dependent capacitors. The load-line models had been used to analyze a 47 GHz HEMT frequency tripler and good agreement has been obtained between the measured and modeled results.

0-7803-5687-X/00/$10.00 © 2000 IEEE

These models are not global but they are application specific. They are best used in applications where the loading of the circuit can be approximated by a resistive load line over the frequency range of operation of the circuit. They are not intended to be used as a global model for foundry distribution.

CAPACITANCE MODELS

The expressions that are used to fit the gate-source and gate-drain capacitances along a resistive load line in the intrinsic IV plane are listed as follows:

$$C_{gs} = C_{gso} + C_{gsp}(1+\tanh\rho_1) + C_{gsn}(1-\tanh\rho_2) + C_{gsn}(1+\tanh\rho_3) \quad (1)$$

where

$$\rho_1 = r_{10} + r_{11}V_{gs} \quad (2)$$

$$\rho_2 = r_{20} + r_{21}V_{gs} \quad (3)$$

$$\rho_3 = r_{30} + r_{31}V_{gs} \quad (4)$$

and:

$$C_{gd} = C_{gdo} + C_{gdp}(1+\tanh\rho_4) + C_{gdn}(1-\tanh\rho_5) \quad (5)$$

where

$$\rho_4 = r_{40} + r_{41}V_{gd} \quad (6)$$

$$\rho_5 = r_{50} + r_{51}V_{gd} \quad (7)$$

These expressions are well bounded in either direction of the local voltages, minimizing the possibility of causing convergence problem during nonlinear simulation.

To extract the parameters of the capacitances, cold FET method [3] is first used to obtain the parasitic resistances. Intrinsic IV characteristics of the HEMT can then be obtained from transforming extrinsic values or through automated measurements of the HEMT. From the IV characteristics, target biasing point and specific resistive load line can be identified based on the intended application. Multi-bias S-parameter measurements are performed and conventional small-signal equivalent circuits are extracted using hot/cold FET method [3] for each intrinsic bias point. The target resistive load line is mapped onto the gate-source and gate-drain capacitance planes in the intrinsic voltage space. Equations (1)-(7) can then be fitted against the mapped load line using commonly available spreadsheet programs.

Asymptotic behavior of the capacitances can be used as constraints to help in the fitting of the parameters. Voltages and gradients at the points of inflexion along the mapped load line in the capacitance planes can also be used to estimate the initial values for the r-parameters. Higher order terms could be used in the ρ-expressions for better fitting of the gradients across voltages but it is usually not required. GaAs and InP HEMTs with gate-length of 0.1-0.15 μm and gate-width of 50-200 μm have been fitted easily for class A power amplifier and active frequency multiplier applications using these expressions.

EXPERIMENTAL RESULTS

A 47 GHz MMIC frequency tripler was analyzed in HP MDS using the above expressions to model the device's capacitances. The chip uses a 200 μm wide GaAs 0.15 μm HEMT device that is biased near pinched-off condition. Low impedance is presented at the output of the device at the fundamental and second harmonic frequencies. After accounting for the parasitic resistances, a 5-Ohm load line was first selected to approximate the output loading condition. Foundry-supplied DC model was used for modeling the IV characteristics of the device and the load-line capacitance models were entered as charge functions in the HP MDS circuit simulator.

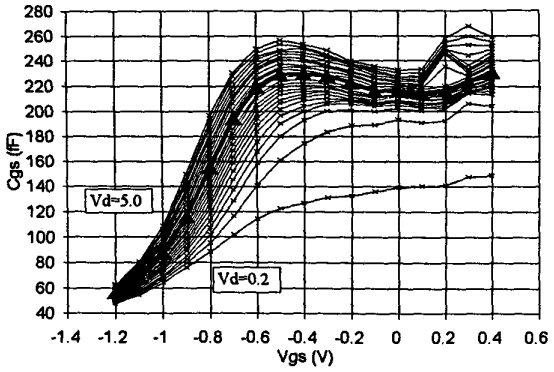

Figure 1. 5-Ohm load line mapped onto Cgs plane.

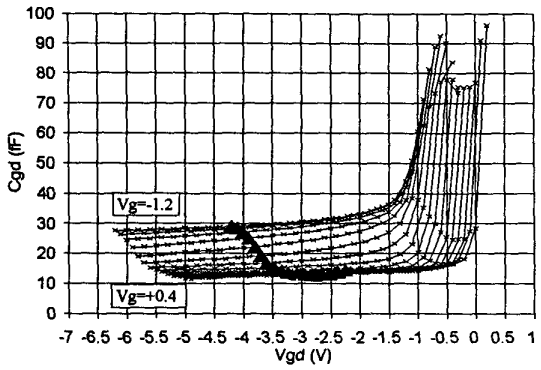

Figure 2. 5-Ohm load line mapped onto Cgd plane.

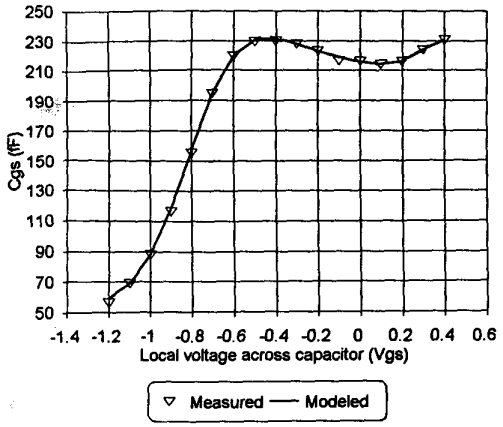

Figure 3. Fitting of Cgs capacitance using the load-line model.

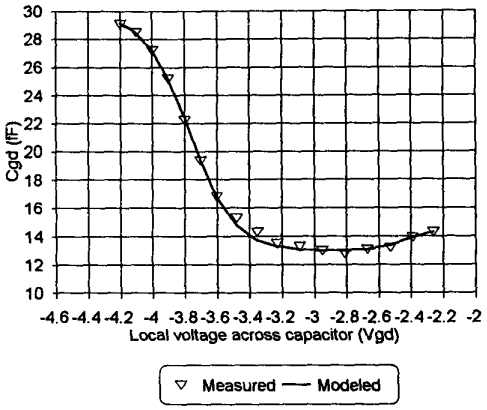

Figure 4. Fitting of Cgd capacitance using the load-line model.

Figure 1 shows the 5-Ohm load line being mapped onto the gate-source capacitance plane while figure 2 shows the mapped load line in the gate-drain capacitance plane. Figure 3 shows the result of the fitted Cgs model against the mapped load line for the gate-source capacitance and figure 4 shows the result of the fitted Cgd model against the mapped load line for the gate-drain capacitance. To illustrate the typical values of the parameters, a set is listed in Table 1. Figure 5 shows the measured output power of the frequency tripler against the modeled performance by incorporating the load-line capacitance models and the constant capacitance model.

From the illustrations, good fit has been achieved by using the proposed models on the measured capacitances' variation along the load line (<5% error in both cases). Good agreement between the measured and modeled performance of the frequency tripler has also been obtained by incorporating the proposed load-line capacitance models in the nonlinear simulation.

The device's dynamic load line of the entire circuit was also evaluated after implementing the device model. It was found that the average

resistive path has a slope of about 10 Ohms. The models were refitted with the 10-Ohms load line and the circuit was re-simulated. It was observed that there is little change in both the simulation result and the final profile of the dynamic load line.

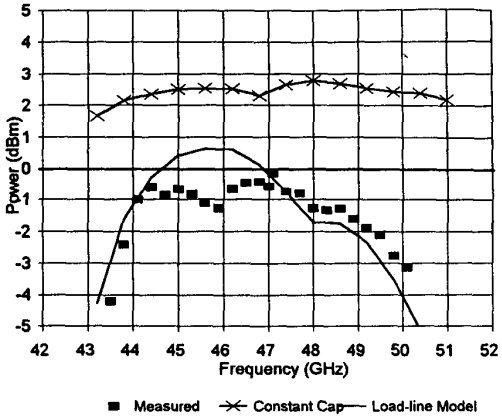

Figure 5. Modeled output power for frequency tripler using the load-line models and constant capacitance model.

CONCLUSION

Expressions for modeling the capacitances' variation along resistive load line in the IV plane of the HEMT have been proposed. The parameter extraction procedure is fast and intuitive. The models showed a good fit in tracking the capacitances' variation along a resistive load line of an actual 0.15 μm GaAs device. Good agreement between the simulated and measured results of a MMIC frequency tripler is also obtained by incorporating the proposed capacitance models in the circuit simulation.

REFERENCES

[1] David E. Root and Brian Hughes, "Principles of Nonlinear Active Device Modeling for Circuit Simulation," 1988, Proc. 32nd IEEE MTT ARFTG Conference, Tempe, AZ, pp. 3-26.

[2] Ph. Jansen *et al.*, "Consistent Small-Signal and Large-Signal Extraction Techniques for Heterojunction FET's," IEEE Trans. Microwave Theory and Tech., Vol. MTT-43, No. 1, pp. 87-93, 1995.

[3] Gilles Dambrine *et al.*, "A New Method for Determining the FET Small-Signal Equivalent Circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, no. 7, pp. 1151-1159, Jul. 1988.

Cgs	Cgso	Cgsp	Cgsn	Cgsa	r_{10}	r_{11}	r_{20}	r_{21}	r_{30}	r_{31}
5-Ohm	-35.1	122.2	42.9	11.8	3.0	3.8	1.2	2.5	-2.4	8.4

Cgd	Cgdo	Cgdp	Cgdn	r_{40}	r_{41}	r_{50}	r_{51}
5-Ohm	12.9	0.8	8.5	11.4	4.7	13.7	3.6

Table 1. Fitted models for Cgs and Cgd along a 5-Ohm resistive load line.