# FULL W-BAND MMIC MEDIUM POWER AMPLIFIER

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## ABSTRACT

**A full W-band, MMIC amplifier has been tested on-wafer. The chip delivers 25-43 mW with 6.2±1.2 dB associated large-signal gain across 75-110 GHz when input power is held constant at 8 mW. This is the widest bandwidth MMIC amplifier ever published that delivers at least 25 mW over the entire W-band.**

## INTRODUCTION

GaAs HEMTs have been demonstrated to possess good power capability in W-band. A MMIC power amplifier with a device periphery of 1.28 mm has been reported [1] to yield 300 mW of RF power at 94 GHz. Using the same device structure and process, similar performance has been repeated in the frequency range of 100-110 GHz [2].

All the results reported were relatively narrow-band and the amplifiers are targeted for very specific applications. On the other hand, a broadband, medium power W-band amplifier would have many applications. It can be used for general instrumentation purposes or it can be used in the development of new mm-wave sub-systems to test out new concepts or ideas. However, a search in the published literatures did not find any such amplifier. This paper describes the construction of a full W-band medium power MMIC amplifier that will deliver 25 to 43 mW of output power across the entire W-band.

The amplifier can be used with frequency multipliers to construct a compact, full W-band, electronically tunable source. Compared to the traditional Gunn diode oscillators in the same frequency range, the new signal source has the capability to set the output frequency quickly and electronically over a wide range of frequencies. This can be used as local oscillator for designing new wide-band transceivers, or it can be used as a general instrumentation source to develop new mm-wave subsystems. An application example will be described in the later section.

## DEVICE CHARACTERIZATION AND MODELING

The circuit uses the proven 0.1 μm AlGaAs/InGaAs/GaAs power HEMT [1] device and MMIC process developed by TRW. A 160 μm wide device on 50 μm thick GaAs substrate has been used as the basic cell for device modeling and characterization. DC and pulsed IV, diode IV and multi-bias S-parameter measurements from 1-40 GHz were performed on the basic device. The small-signal equivalent circuit model parameters were extracted using cold/hot FET method [3] for each biasing point. Angelov's [4] model was used to fit the pulsed IV characteristics and gate-source, gate-drain capacitances' variations across different bias. Calvo's formulation [5] was then used to resolve



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discrepancies between the large-signal and small-signal models at the biasing point.

## CIRCUIT DESCRIPTION

The amplifier consists of four stages of amplification. Each of the first three stages utilizes a 160 μm wide devices while the last stage consists of two 160 μm devices connected in parallel via a Y-junction. The size of the chip is 2300 μm by 1200 μm. Figure 1 shows the photograph of the fabricated chip.

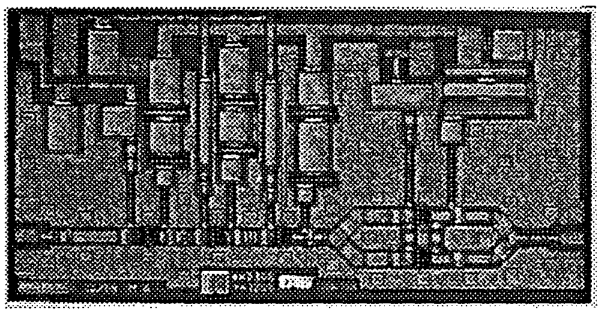

Figure 1. Photograph of the broadband amplifier. Chip size is 2300 μm x 1200 μm x 50 μm.

The extracted large-signal model for the FETs was entered into HP MDS by defining custom equations for the current and charge sources. Load-pull contours were simulated across the entire W-band to determine the optimized loading impedances for the device. For the last two stages, the length of the RF-shorted shunt stubs and the length of series transmission lines between stages were adjusted for good output power across the entire band, by trading off with power efficiency. The matching networks for the front two stages were optimized for flat overall small-signal gain. Clamping resistors were used at the last stage to suppress any possible odd-mode oscillation. Grounded coplanar waveguide transmission lines were used to reduce parasitic elements that will limit high frequency performance. All the discontinuities were simulated using a full 3-D electromagnetic simulator.

## RESULTS

The amplifier was attached to a copper plate with off-chip R-C networks to prevent bias oscillations. The small-signal gain, input and output return loss were measured via on-wafer GGB WR-10 probes using an HP 8510 VNA with 80-120 GHz frequency extender. The plot for the small-signal gain and input return loss from 75-110 GHz is shown in Figure 2. At 75 GHz, the gain and power were measured using a scalar setup, which used a HP 8350B source driving a DBS Microwave active doubler driving a Pacific Millimeter tripler. An HP 8486A power sensor and HP 437B power meter were used to measure the output power and gain.

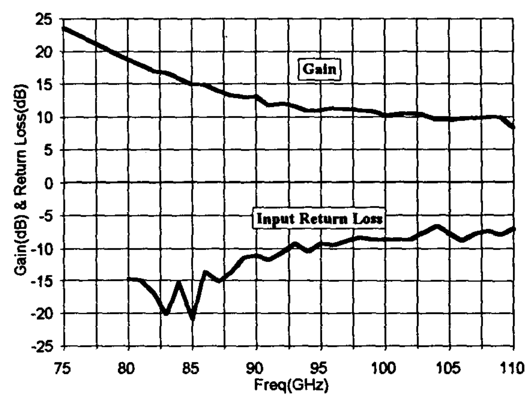


Figure 2. Measured small-signal gain and input return loss over entire W-band.

From 80-110 GHz, a wide-band mechanically tunable (Carlstrom) Gunn oscillator was used to supply the input power to the chip for output power measurements. A Hitachi WR-10 precision variable attenuator was used to control the input power and a Tektronix harmonic mixer is attached to a frequency counter to monitor the actual frequency via a 15-dB Millitech coupler. HP 8486A power sensor and HP 437B power meter were used to measure the output power from the chip. All measurements were referred to the pads of the chip and Figure 3 shows the output power, associated large-signal gain and P.A.E across the W-band frequencies with the input available power being kept constant at 8 mW.

The small-signal gain rolls off quickly from 23 dB at 75 GHz to 15 dB at 85 GHz. From 85-110 GHz, the gain is generally flat with a typical value of about 10 dB. When the input power is held constant at 8 mW, the chip delivers 43 mW at 80 GHz, and generates more than 25 mW across the rest of the band. Under these conditions, the associated large-signal gain is flat with 6.2±1.2 dB across 75-110 GHz.

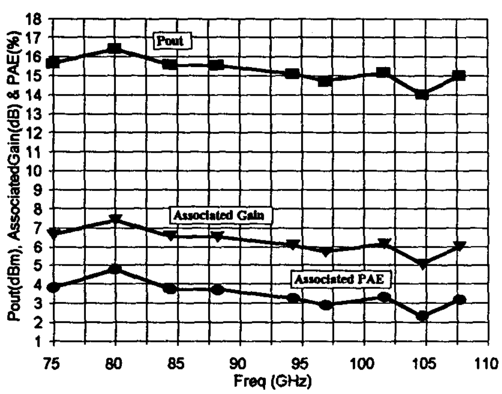


Figure 3. Measured Pout, associated large-signal gain and PAE across W-band. Pin is held constant at 9 dBm.

The originally simulated results predicted a flat small-signal gain of about 12 dB and a higher output power of 50-100 mW across 75-110 GHz. The discrepancy seems to be caused by inaccuracies in the EM-simulation results of the discontinuities and process variation. Re-simulation of the circuit was performed without including effects of the discontinuities and with a new extracted model from the same wafer run. It predicted a small-signal gain of similar roll-off trend as seen from the measured data and it also predicted a flat gain of about 9 dB from 85-110 GHz. The large-signal re-simulation gave an output power of 25-40 mW across W-band, which is also close to the actual result.

The P.A.E. for the entire chip is between 2.3-4.7%. With better models for the discontinuities and by using smaller gate-width devices for the front two stages, it is believed that a P.A.E. of 5-10% can be achieved across the entire W-band. A second iteration of the design has been planned and higher output power, P.A.E and small-signal gain are expected.

## APPLICATION

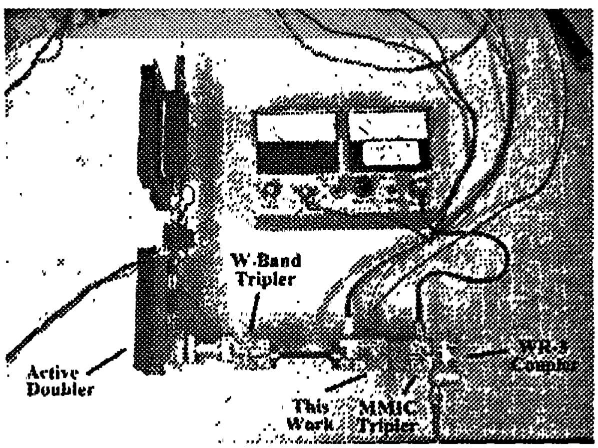


Figure 4. 240-320 GHz single-sweep scalar setup using the amplifier to drive a high frequency tripler.

Two of the amplifiers were mounted in WR-10 waveguide blocks with alumina waveguide-microstrip transitions [6] wire-bonded to the input and output pads. The amplifier module amplifies x6 (Avantek active doubler + in-house built tripler) signals derived from the fundamental HP 8350 source to drive a high efficiency frequency tripler [7] to produce signals in the range of 240-320 GHz. Together with a WR-3 waveguide coupler and Pacific Millimeter WR-3 power detector, transmission/reflection scalar measurement can be made with a single sweep. The photograph of the arrangement is shown in Figure 4. The setup is used to develop frequency multipliers for application in sub-millimeter receiver systems to study radio astronomy phenomena such as the early universe formation.

## ACKNOWLEDGEMENT

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