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Ion etching of ultra-narrow structures.

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ABSTRACT

We describe the use of Polymethylmethacrylate as both electron beam sensitive resist and ion etch mask for high-resolution pattern transfer. By using high-resolution electron beam lithography, chemically assisted ion beam etching, and in-situ metallization, we have fabricated ultra-narrow gates with lateral dimensions below 20 nm, spaced with <50 nm pitch on high mobility 2D electron gas material. This technique, which is thought to provide extremely small lateral electron depletion lengths and well defined confienement potentials, allows us to produce new and more complicated structures for the study of quantum transport.

1. INTRODUCTION

Lift-off technology often limits the ultimate sizes of structures which can be transferred into semiconductor materials. To avoid such limitations, it is desirable to combine the function of a high-resolution resist with that of an etch mask. This has previously been accomplished by using inorganic materials, such as fluorides[1], as both resist and etch mask. However, the application of these materials to high-resolution patterning is limited either by the inherent grain size or the low sensitivity of these inorganic resists. Instead of optimizing such new resist schemes, we have therefore developed selective ion beam etching conditions which allow us to apply a common positive electron beam resist, polymethylmethacrylate (PMMA), as a durable etch mask.

2. PROCEDURE

We use thin layers of PMMA with molecular weights of approximately 950,000 baked at 160° for 2 hours. These layers are exposed in an electron beam lithography system either at 25 kV or at 250 kV, and developed in a 3:7 cellusolve:methanol mixture. The lithographically defined PMMA stencils are then used as etch masks in a chemically assisted ion beam etch (CAIBE)[2] process, and we selectively transfer the beam-written pattern into the semiconductor substrate (Fig.1)[3].

3. RESULTS AND DISCUSSION

3.1 Optoelectronic structures

Electron beam lithography and CAIBE processing allows us to generate deep slits into both GaAs/A1As and InP/InGaAs structures to isolate vertical optoelectronic devices, such as detectors or surface-emitting lasers (Fig. 2). Since the relative etch rate of PMMA is only approximately 20% of that measured for GaAs, we can use 500 nm thick resist layers to transfer our electron-beam written pattern as deep as 2 μm into the substrate. This allows us to develop simple processing techniques which allow us to generate complicated optoelectronic structures, such as coherently coupled surface emitting laser arrays in which the 700 nm wide individual laser elements are separated by only 100 nm gaps[4].

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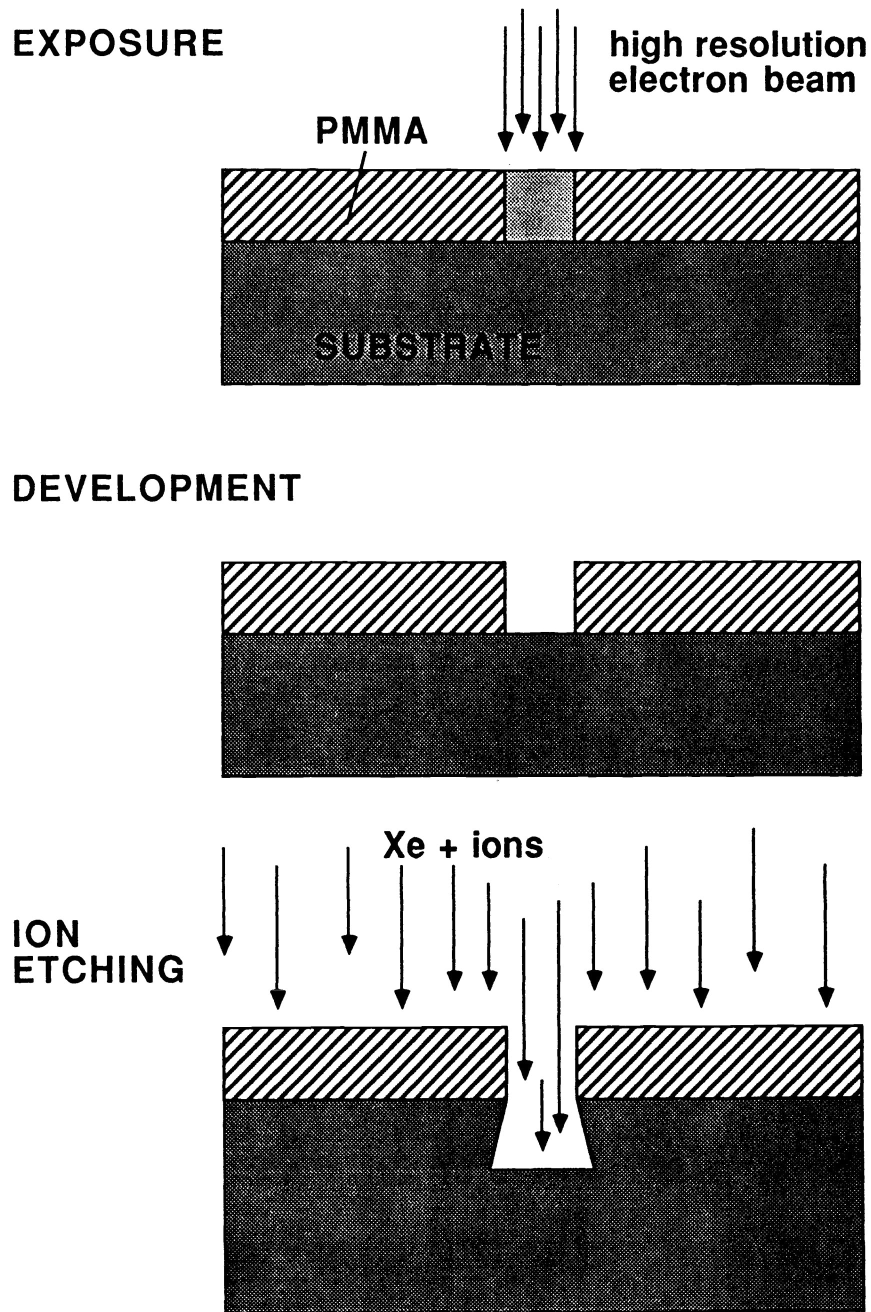

Fig.1. Description of our pattern transfer method using PMMA both as electron beam sensitive resist and etch mask.

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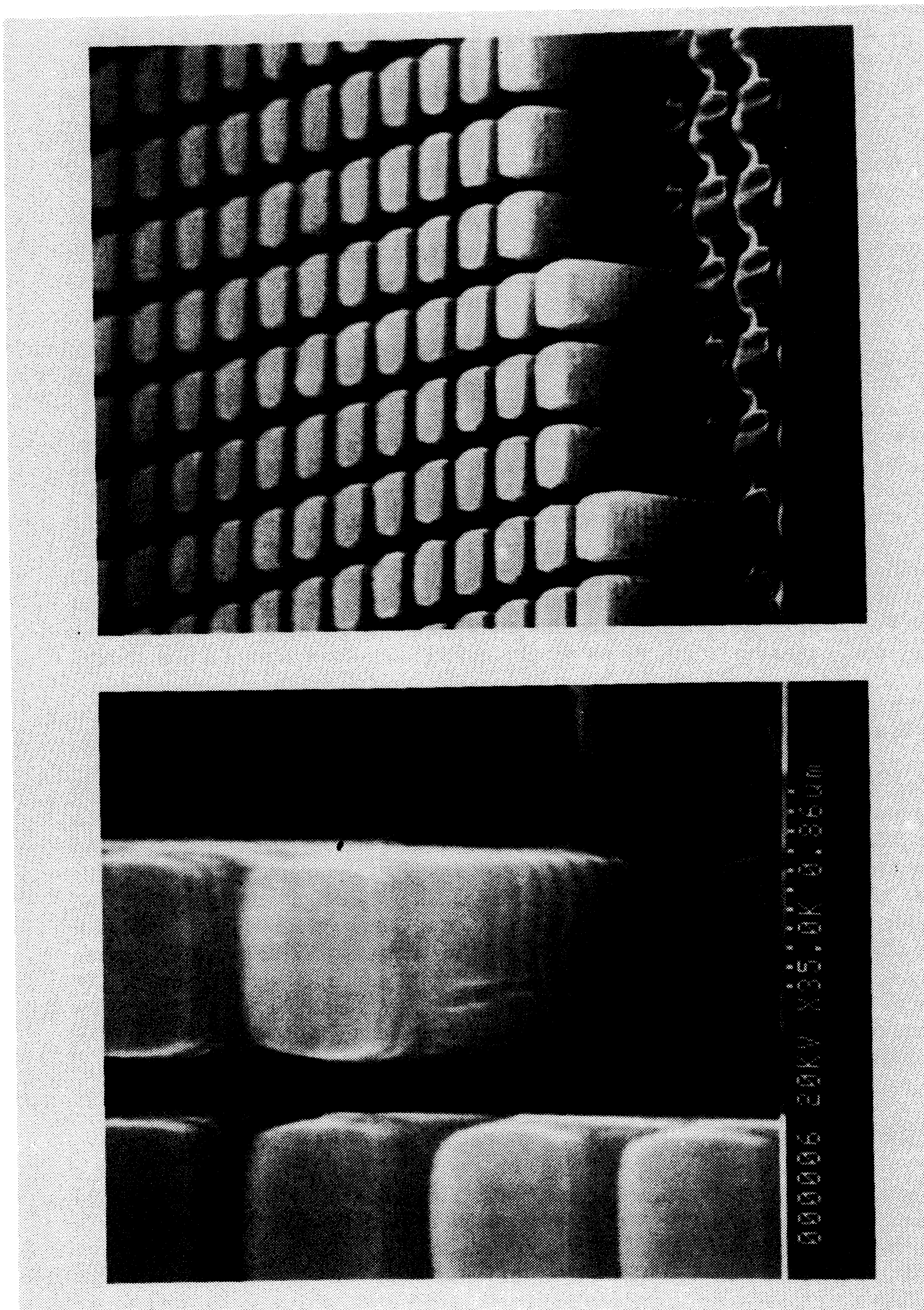

Fig.2. SEM micrographs showing coherently coupled 700 nm wide microlaser elements separated by 100 nm.

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3.2 High mobility 2D electron gas structures

We can also use the patterned PMMA layer as a ion damage mask for device isolation. We find that a 1 kV He+ beam produces ion damage as deep as 200 nm deep in GaAs/AlGaAs MODFET material[5], but can be shielded by only a 20 nm thick PMMA layer. Similarly, 500 V Ne+ ions generate damage more than 70 nm deep[6], but are masked by a 15 nm thick PMMA layer. We can therefore define isolation patterns by electron beam lithography, and require only very thin masks for the selective low voltage ion beam exposure. Through this process, we generate high-resolution geometries in 2D electron gases (2DEGs) for both room- and low-temperature measurements, where the resolution is primarily limited by the relatively short depletion lengths of 10 to 20nm[6]. We have used this technique to generate periodic arrays of scattering centers in high-mobility 2D electron gases (Figure 3), and we observe that in material with mobilities of 950,000 $cm^2/V \cdot sec$, "anti-dot" spacings below 250 nm still conduct and yield very interresting low-field features[7].

In order to further improve the resolution of such patterns on high-mobility 2DEG structures, a combination of ion etching and gating, similar to the more commonly used "recessed gate" technology, may be used. With this technique, depletion lengths below 10 nm are thought to be obtainable. The combination of high voltage electron beam lithography and ion etching can transfer the closely spaced features which are required to obtain structures with dimensions far below the electron coherence length. High voltage electron beam lithography improves the pattern resolution[8], since the incident electron beam is broadened only slightly through forward scattering, and the overall back-scattered electron contribution to the resist exposure is significantly reduced. We thus obtain a larger development latitude at such high energies, which allows thicker resists to be processed with high resolution patterns. Furthermore, we have shown in previous work that, at energies below 300 kV, electrons do not introduce any significant damage into the lattice. This allows us to pattern nanostructures even on extremely damage-sensitive high-mobility 2DEG structures[9].

3.3 Microfabrication of a surface superlattice

Since, even using high voltage lithography on bulk substrates, the PMMA resist profile observed after closely-spaced structures are developed is typically not ideal for lift-off processing, it is often desirable to improve this profile with a subsequent ion etching step. The effective thickness of the resist is thereby increased if the semiconductor can be etched selectively. An application of this contrast enhancement effect is shown in Figure 4, where we show a schematic describing the processing sequence for defining a series of narrow gates on GaAs. The gate metallization can also be performed in the etching chamber immediately after the ion beam exposure, avoiding surface oxide formation and improving the adhesion of the metal. Evaporation on such cleaned surfaces, in addition to the undercut liftoff profile allows us to successfully pattern closely spaced gold gates on 2DEG material. Figure 5 shows back-scattered electron images from such lift-off gates, which show that continuous inter-digitated lines with 60 nm center to center spacing are readily produced.

3.4 Cross-sectional TEM analysis

For more detailed examination, we have obtained crossectional TEM images[10] of the resulting gated structures by lithographically depositing a SrF_2 mask perpendicular to the gates (Fig.6). Figure 7a shows a bright-field image of such a crossection, where the Au gates are clearly delineated through mass-thickness contrast. Figure 7b shows a similar bright-field image, whereas in Figure 7c the corresponding dark-field image, showing the GaAs substrate, are shown. From these images, we note that the PMMA mask is undercut during the ion etch process, and the total etch depth is approximately 30 nm deep. Even after removing more than 30% of the cap and donor layer of our 2DEG structure, only negligible changes in the 4-terminal resistance at 4.2 K are observable. Since

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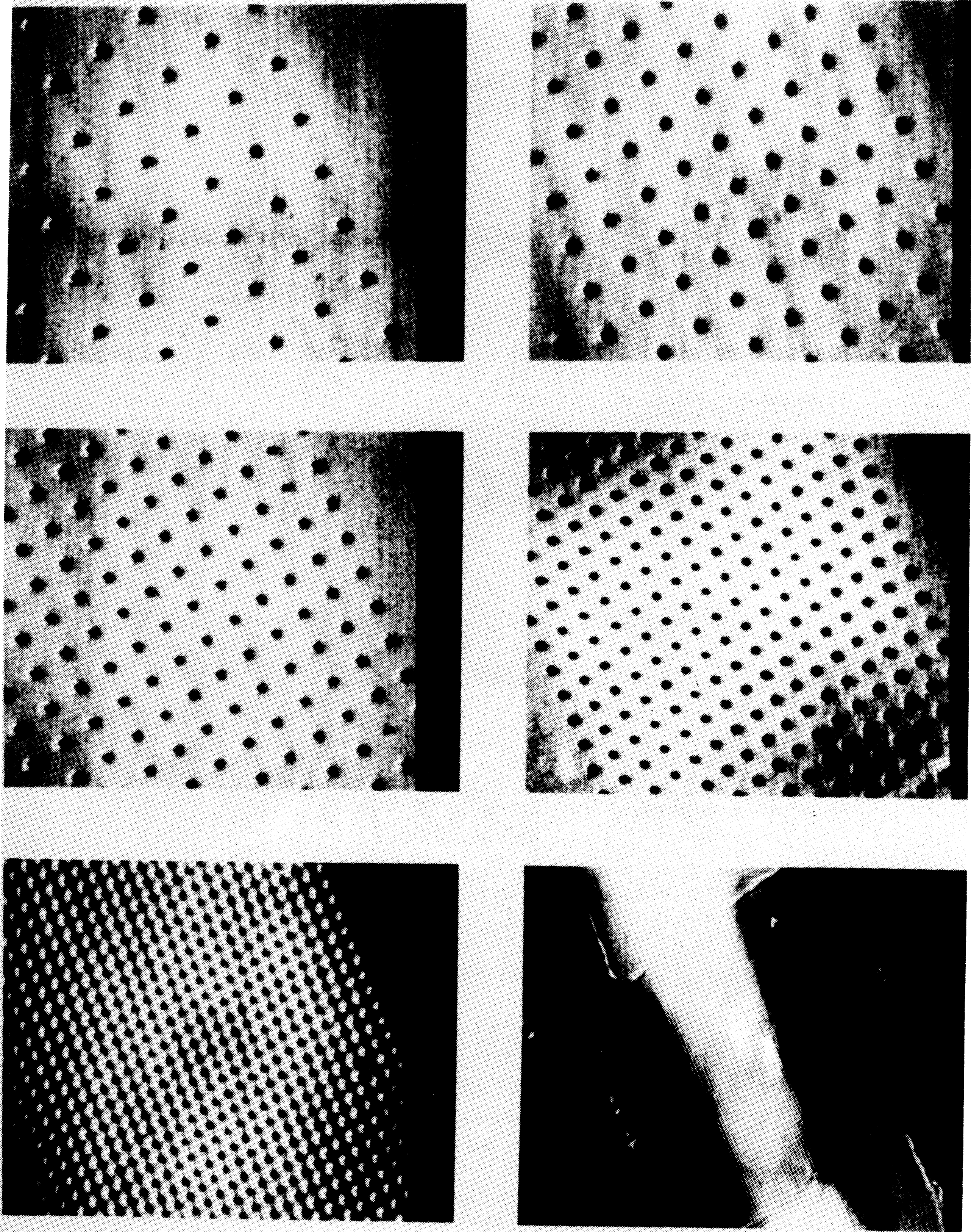

Fig.3. SEM images of periodic scattering centers used to influence the low-temperature magnetoresistance behavior of a 2DEG in a Hall bar.

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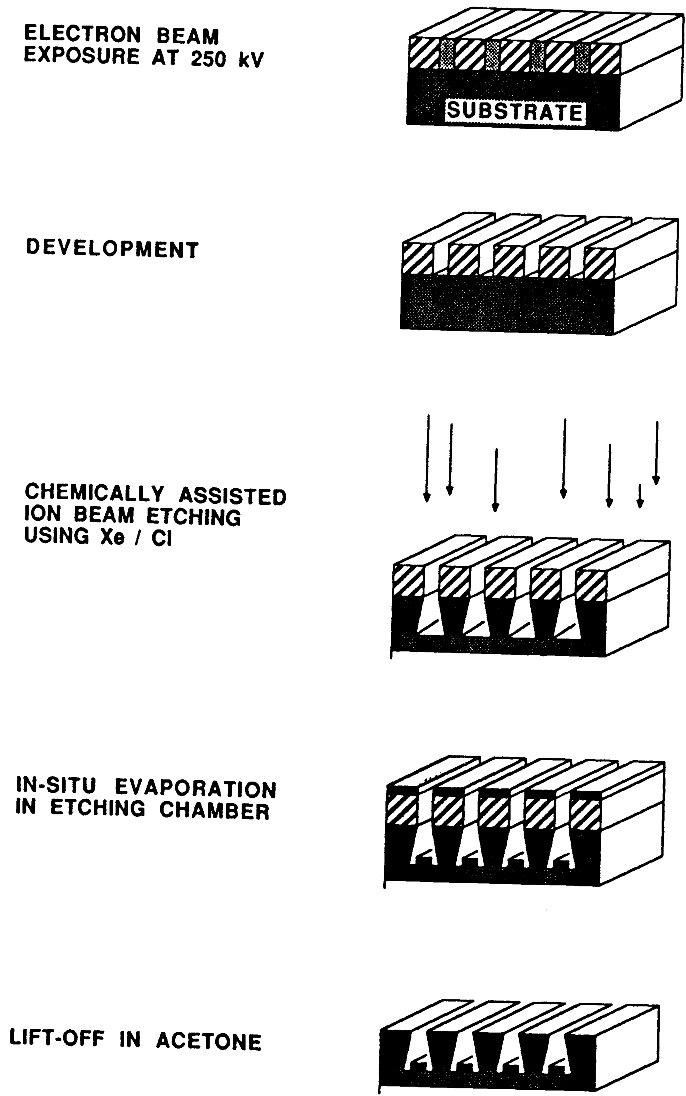

Fig.4. Schematic of process used to produce closely spaced gates on a 2DEG structure.

the distance of the gate to the bottom of the donor layer is approximately 15 nm, we can infer that the layer electrically damaged by our 500 eV Xe+ ion beam is less than 10 nm thick.

3.5 Ultimate resolution of high-voltage lithography on PMMA

To determine the limitations of this lithographic technique, we have varied the pitch of our line structures. Figure 8 shows a series of micrographs showing 10 nm wide lines spaced 60nm, 40nm and 30nm apart. These structures were all etched into GaAs 2DEG structures using 500 eV Xe+ assisted by Cl_2 gas jets. From these pictures, we observe that, below 40 nm, the structural integrity

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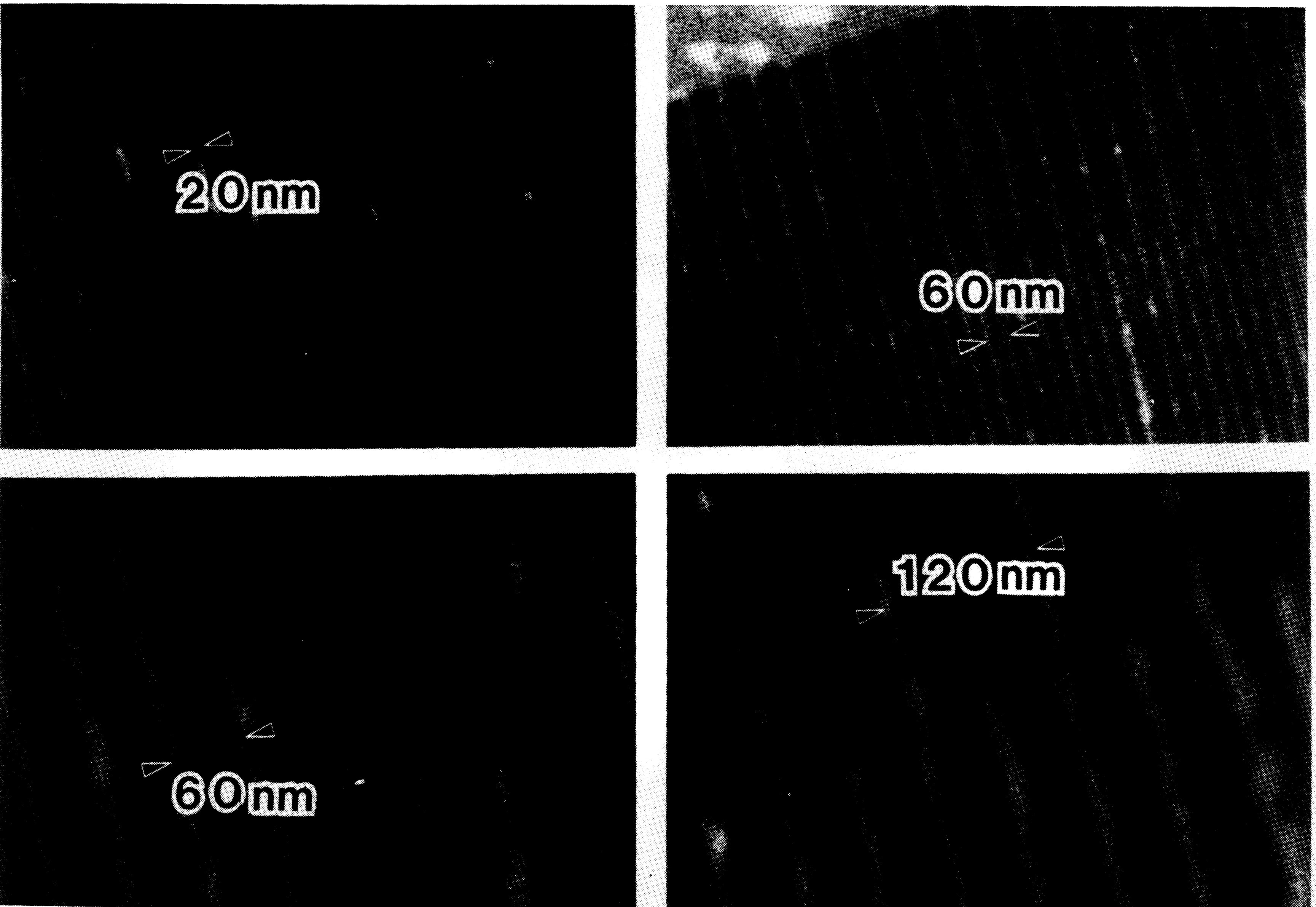

Fig.5. Backscattered electron image of interdigitated 20 nm gold lines with 60 nm pitch.

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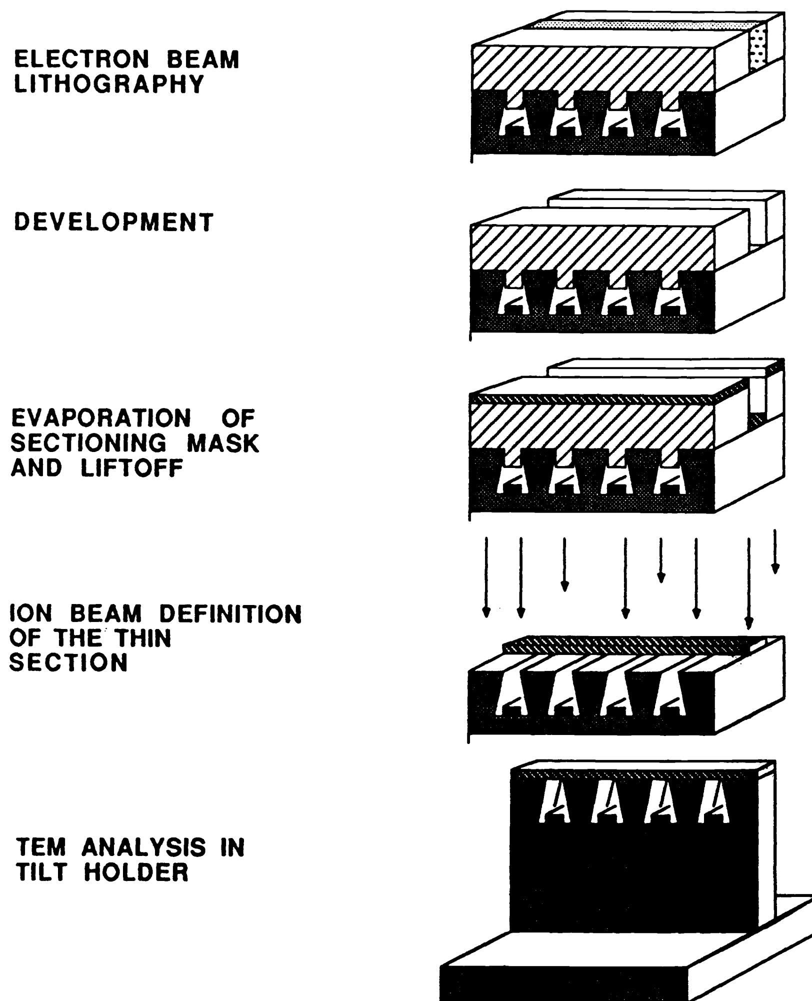

Fig.6. Microfabrication process used to obtain a thin section to analyse interdigitated gates.

of our PMMA resist limits the pattern resolution. At this pitch, the 60 nm thick resist fins, which are separated by only 10-20 nm after development, are found to bend towards each other and fill in the lithographically defined gaps. This distortion of the mask results in discontinuous slits in the GaAs after ion beam etching (Figure 8c). This structural problem, which is inherent to PMMA, can be solved by either reducing the resist thickness, or alternatively by increasing the development time. Once the electron beam lithography conditions are optimized, however, 10 nm lines with 40 nm pitch can be consistently fabricated in an interdigitated geometry (Figure 9a) over 2DEG structures. In these structures, we can modulate the potential within less than the Fermi wavelength of our high-mobility material.

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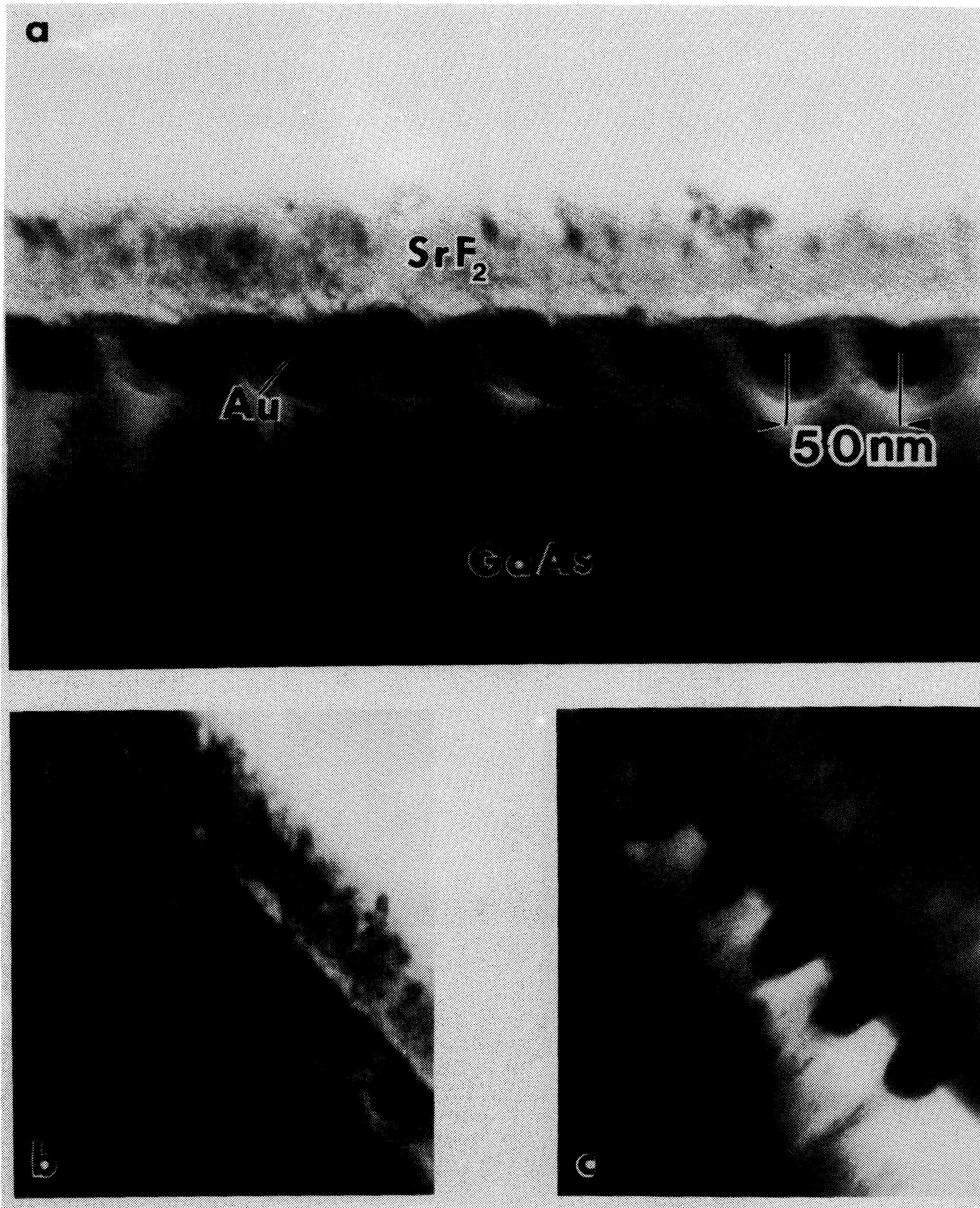

Fig.7 TEM bright-field and dark-field images showing the GaAs containing the Au gates spaced 50 nm apart obtained from our microfabricated thin-section.

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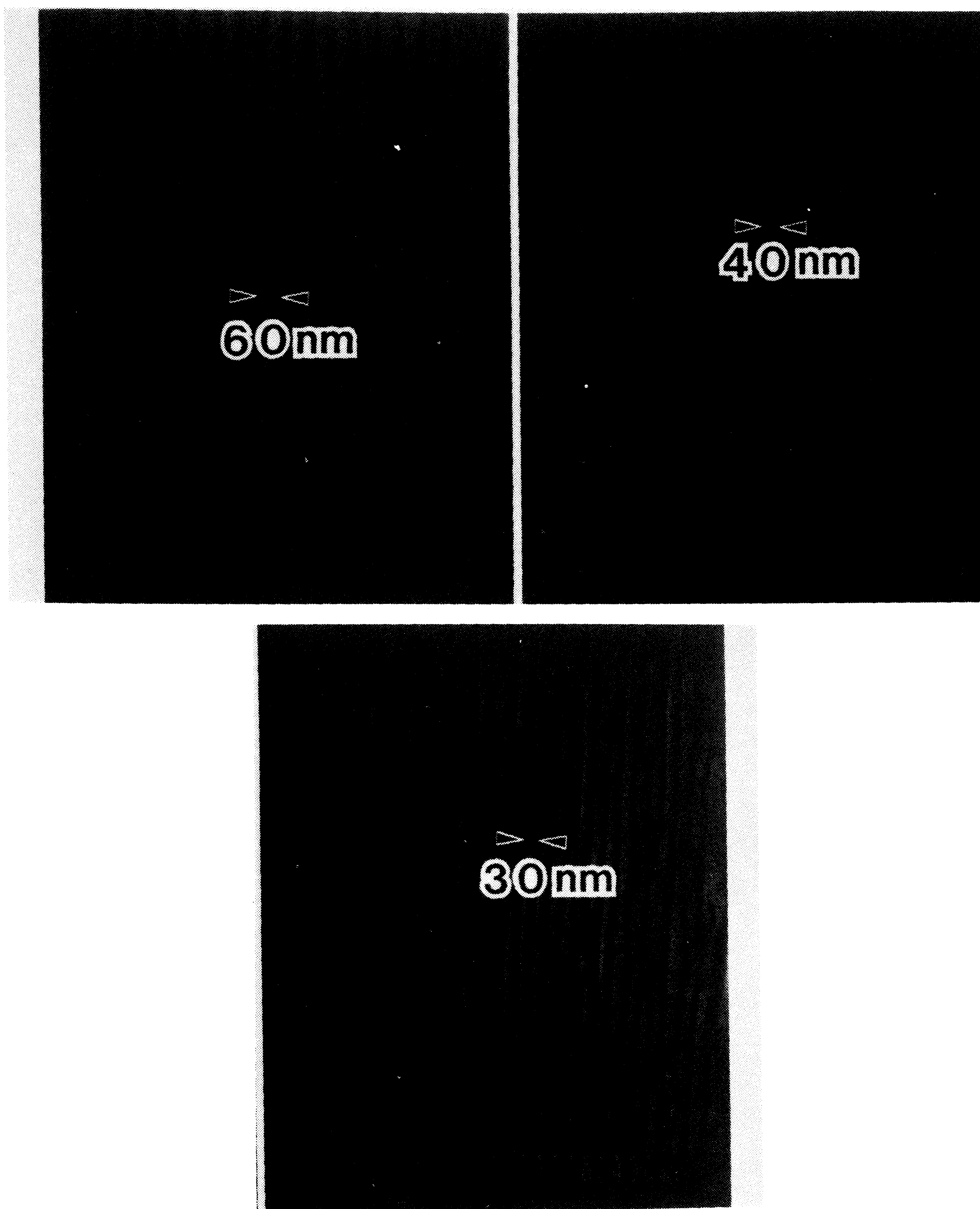

Fig.8. SEM micrographs of 10 nm wide etched lines in 2DEG material spaced 60, 40 and 30 nm apart.

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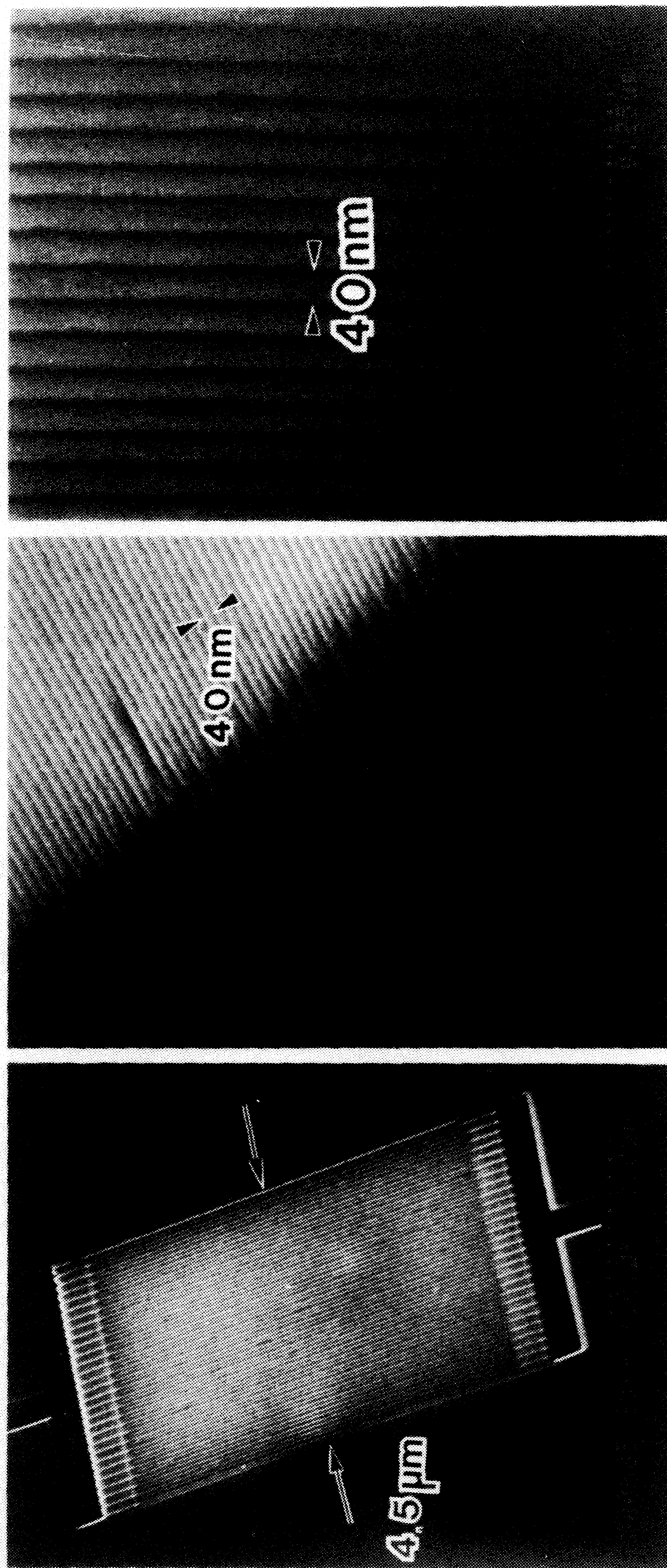

Fig.9. SEM micrographs showing an interdigitated structures with 40 nm pitch.

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4. CONCLUSIONS

When ion etching conditions are optimized, high semiconductor etch rates selectivities can be obtained even when using high-resolution organic resists, such as PMMA. This allows direct pattern transfer from such resists into semiconductor substrates, without the requirement of a lift-off and allows us to produce extremely small structures with very close spacings. Very closely spaced high resolution structures make possible the fabrication of intricate optical and transport structures. Furthermore, if PMMA is used as resist, etch mask, and lift-off mask, electrostatic gates can be deposited by in-situ metallization after the dry etching process, and complex new devices for low-temperature transport measurements and spectroscopy can be developed.

5. ACKNOWLEDGMENTS

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