Power-Amplifier Modules Covering 70–113 GHz Using MMICs

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***Abstract*—A set of W-band power amplifier (PA) modules using monolithic microwave integrated circuits (MMICs) have been developed for the local oscillators of the far-infrared and sub-millimeter telescope (FIRST). The MMIC PA chips include three driver and three PAs, designed using microstrip lines, and another two smaller driver amplifiers using coplanar waveguides, covering the entire W-band. The highest frequency PA, which covers 100–113 GHz, has a peak power of greater than 250 mW (25 dBm) at 105 GHz, which is the best output power performance for a monolithic amplifier above 100 GHz to date. These monolithic PA chips are fabricated using 0.1-μm AlGaAs/InGaAs/GaAs pseudomorphic T-gate power high electron-mobility transistors on a 2-mil GaAs substrate. The module assembly and testing, together with the system applications, will also be addressed in this paper.**

***Index Terms*—GaAs, HEMT, millimeter wave, MMIC, power-amplifier module.**

TABLE I
FREQUENCY RANGE OF THE PA CHIP SET AND THE ASSOCIATED FREQUENCY MULTIPLICATION PLAN AS DRIVERS FOR LO SOURCES AT FREQUENCIES INTO THE TERAHERTZ RANGE

	71-79 GHz	80-92 GHz	88-99 GHz	92-106 GHz	106-112.5 GHz
X2	142-158	160-184	176-198	184-212	212-225
x2x2	284-316	320-368	352-396	368-424	424-450
x2x3		480-552 Band 1a		552-636 Band 1b	
x2x2x2		640-736 Band 2a	704-792 Band 2b	736-848 Band 3a	848-900
x2x2x3	852-948 Band 3b	960-1104 Band 4a	1056-1188 Band 4b	1104-1272 Band 5	1272-1350
x2x2x2x2			1408-1584 Band 6a	~~1472-1696~~ Band 6a	
x2x2x3x2	1704-1896 Band 6b			2400-2544 Band 7a	2544-2700 Band 7b

I. INTRODUCTION

W-BAND MMIC power amplifiers (PAs) have been developed for transmitter applications [1], [2]. These amplifiers can be used as drivers for local-oscillator (LO) sources at frequencies into the terahertz range. The LOs for the far-infrared and sub-millimeter telescope (FIRST) will be comprised of synthesizers and active multipliers to provide output frequencies of 71–112.5 GHz, PAs to amplify these W-band signals, and finally, chains of Schottky diode multipliers to achieve terahertz frequencies. Table I presents the frequency range of the PA chip set and the associated frequency multiplication plan. The PA frequency breakdown is a trade of the power output and the bandwidth based on state-of-the-art capability of current GaAs power high electron-mobility transistor (HEMT) monolithic-microwave integrated circuit (MMIC) technology. The motivation of this paper is to develop a set of W-band PAs, which could be used for the FIRST LO chains.

This paper presents the results of these W-band PA modules, as well as the MMIC PA chips. The MMIC chips are fabricated using 0.1-μm AlGaAs/InGaAs/GaAs pseudomorphic (PM) T-gate power HEMT MMIC technology on a 2-mil GaAs substrate. Although InP-based HEMT MMICs have demonstrated excellent power performance at W-band [2], GaAs-based HEMT MMIC technology was selected for this project due to the process maturity. The 2-mil GaAs HEMT PAs not only demonstrated good power performance with high yield at W-band (94 GHz) [1], but also showed impressive results from Ka- to V-band [3]–[6]. In this paper, three sets of PA chips and their driver amplifiers covering 72–81, 90–101, and 100–113 GHz were designed using microstrip lines. The three-driver amplifiers were designed with a common-output gate periphery of 640 μm, while the PAs had 1280 μm, to fulfill output power requirements. Another two medium driver amplifiers with gate peripheries of 160 and 320 μm were designed with coplanar waveguide (CPW) to cover frequency bands of 70–100 and 80–115 GHz. The measurement results indicated each microstrip-line driver amplifier and PA provide at least 20 and 22 dBm (160 mW), respectively, in the frequency range that it covered, while the CPW designs have output power level of 14–17 dBm (25–50 mW). For the first time, the full power data as a function of frequency are presented in W-band and the wide-band capability is demonstrated. Moreover, the 100–113-GHz PA has a peak power of greater than 250 mW (25 dBm) at 105 GHz, which is the best output power performance for a monolithic amplifier above 100 GHz

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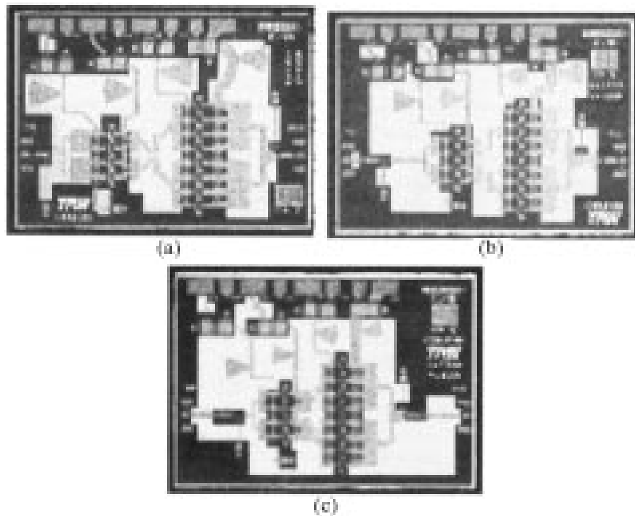


Fig. 1. Three microstrip-line W-band monolithic PAs. (a) 72–81 GHz. (b) 90–101 GHz. (c) 100–113 GHz. The chip sizes are 2.3 × 1.6 mm^2.

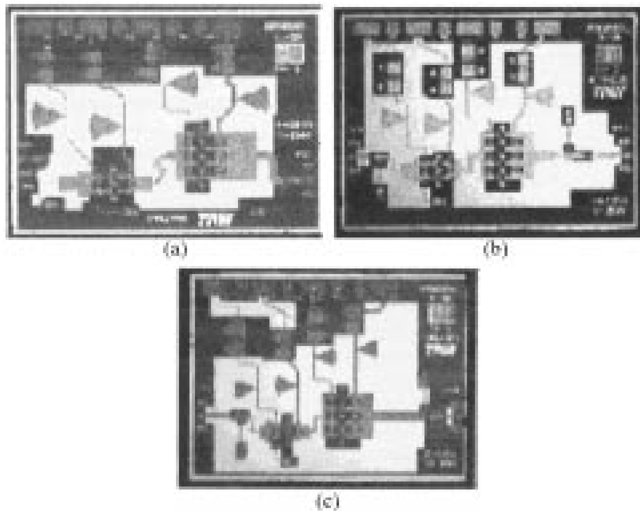


Fig. 2. Three W-band microstrip-line drive amplifiers. (a) 72–81 GHz. (b) 90–101 GHz. (c) 100–113 GHz.

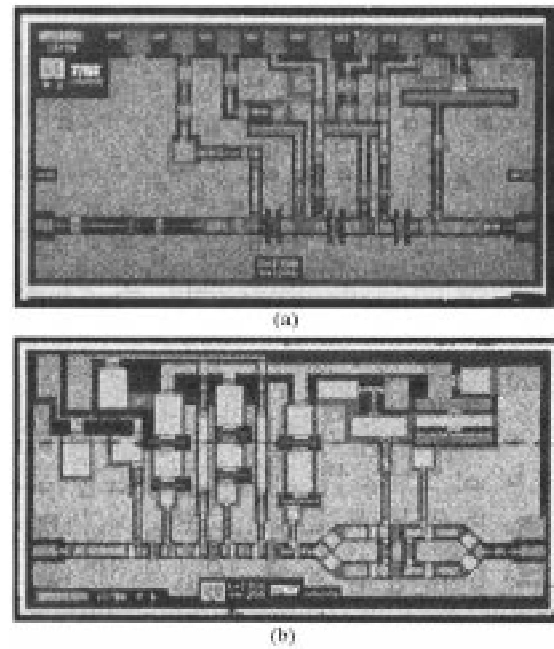
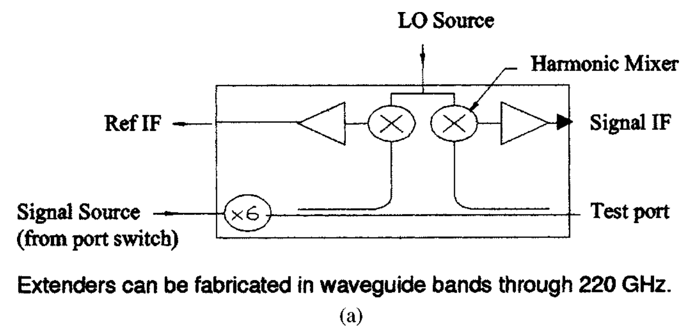
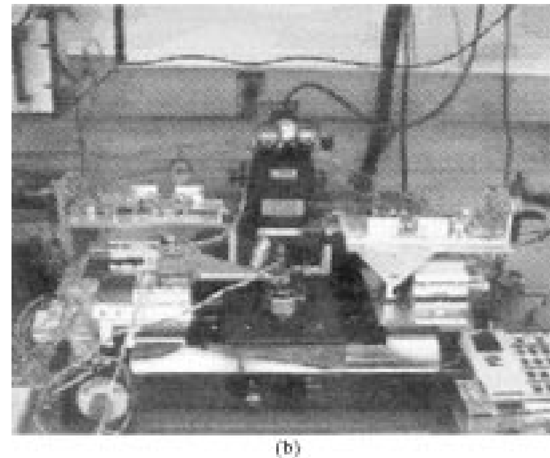


Fig. 3. Two W-band medium power CPW drive amplifiers. (a) 65–102 GHz. (b) 80–115 GHz.



(a)



(b)

Fig. 4. 70–115-GHz on-wafer small-signal S-parameter test set. (a) Block diagram. (b) Photograph.

to date. The MMIC PA chip testing and module assembly with the WR-10 waveguide input/output ports will also be included in this paper.

II. MMIC Process and Device Characteristics

The 0.1-μm power HEMT device development has been reported [7]. The HEMT structure is grown using molecular beam epitaxy (MBE) on 3-in substrates and uses a PM $In_{0.22}Ga_{0.78}As$ channel. The HEMT device structure is based on a double heterostructure design to achieve a high-aspect ratio for 0.1-μm gate lengths. The devices typically exhibit a gate-to-drain breakdown voltage of 6 V measured at a gate current of 0.1 mA/mm, a peak dc transconductance of 600 mS/mm, a maximum current of 600 mA/mm, a unit current gain frequency f_T of 130 GHz, and a maximum oscillation frequency $f_{\max}$ of greater than 200 GHz.

The HEMT linear small-signal equivalent-circuit parameters are obtained from careful fit of the measured small-signal S-parameters to 50 GHz. These parameters are consistent with estimation based on device physical dimensions and parameters. The Curtice–Ettenberg FET asymmetric model was used to describe the HEMT device nonlinear behavior [8]. The nonlinear transconductance coefficients were then obtained from fitting the dc–I-V measurement of the devices. The device models have been verified by comparing the measured and simulation results of simple prematched device structures [1].

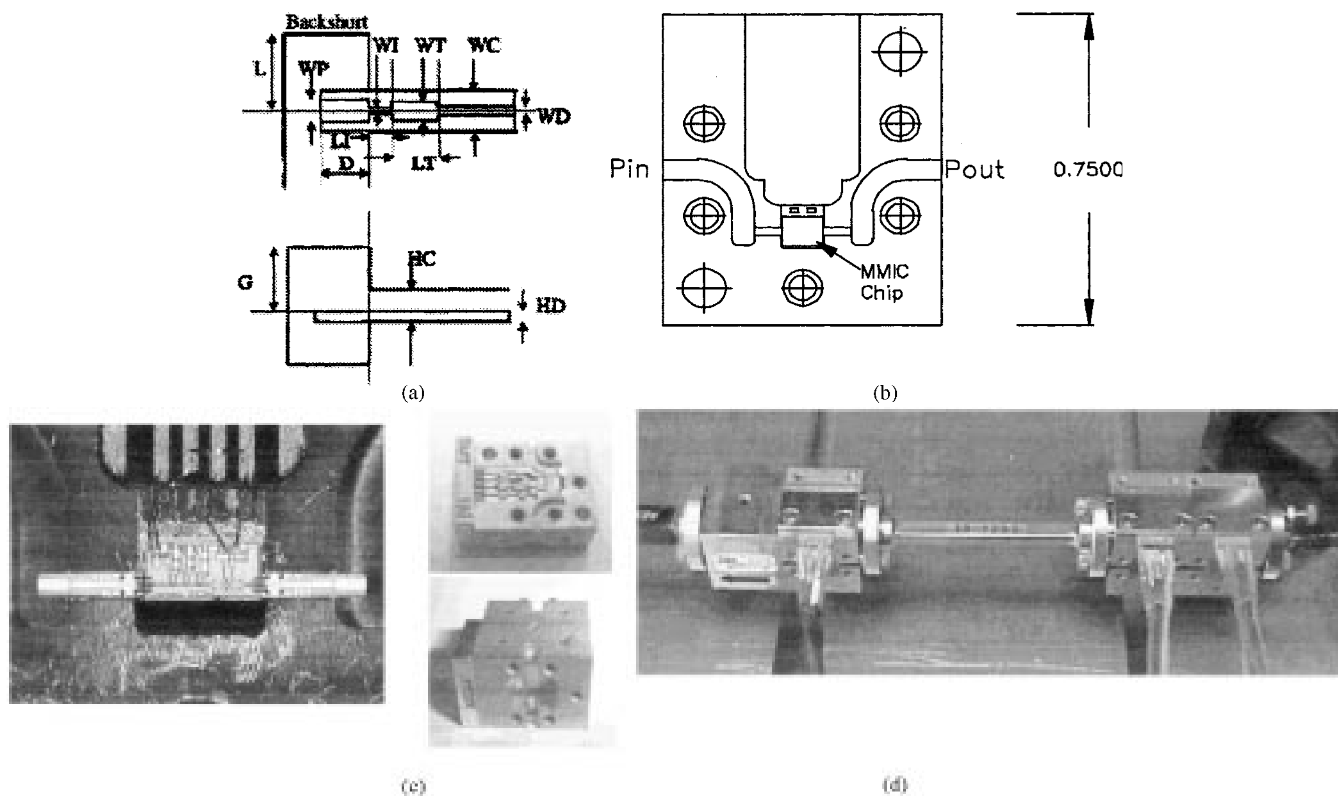


Fig. 5. (a) Configuration for longitudinal transition. (b) Drawing of the module housing design. (c) Photographs of a CPW driver amplifier chip mounted in the module. (d) Cascaded associated driver or PA modules in the same frequency bands.

III. MMIC PA DESIGN

The MMIC PAs can be designed using either microstrip line or CPW. CPW has the advantage for ease of a shunt element, i.e., for a single HEMT with common source configuration, it can be easily implemented in the layout design. However, for large device periphery (high-output power) designs, since a number of HEMT devices need to be combined, it becomes difficult to arrange in the layout because a source ground cannot be easily realized, especially in millimeter-wave frequency range. On the other hand, microstrip-line environment is preferred to stack common transistors device in parallel with a via-hole source ground between the HEMT devices. Therefore, the microstrip line is used to design the high-output PA and driver chips, while the CPW is used to design the medium driver amplifiers in this paper.

Fig. 1 shows the three PA chips (covering 72–81, 90–101, and 100–113 GHz). All the three PAs follow a common circuit architecture, which is a single-ended two-stage design. The first stage employs four cells of eight-finger, 160-μm HEMT devices, and second stage has twice the device periphery with eight HEMT devices. The topology used for the PA designs has been reported in [1], with matching networks realized by high–low-impedance transmission lines. For these new designs, reactive matching elements were optimized for increased bandwidth and higher frequency performance. EM simulations were performed for all the passive structures using Sonnet [9]. The driver amplifiers also follow a common circuit architecture, which is similar to that of the PAs with half of the gate peripheries for both the first and second stages. Fig. 2 shows the chip photographs of the three driver amplifiers. The chip sizes for all of the amplifiers are 2.3×1.6 mm^2, in order to facilitate ease of dicing of the wafers.

The photographs of the two CPW medium power-driver amplifiers are shown in Fig. 3. They are both broad-band designs. The first one (Fig. 3(a), chip size 2.3 mm $\times$ 1.2 mm) is a three-stage amplifier designed to cover a frequency range of 70–100 GHz, while the second one [see Fig. 3(b)], with the same chip size, is a four-stage design to cover 80–115 GHz. The matching networks are also implemented with high–low-impedance transmission lines with metal–insulator–metal (MIM) capacitors used in the interstage matching networks for dc block and bias networks for RF bypass. The device peripheries are 160-160-160 μm and 160-160-160-320 μm, respectively. Compared with the microstrip two-stage designs, these two CPW designs have higher input/output impedance at the device end and, thus, are easier to obtain broad band. In addition, the three- and four-stage selections also provide more gain margin to tradeoff bandwidth. Since the eight-finger, 160-μm HEMT device is used for a unit device cell, the output stage of the first CPW amplifier (320-μm total gatewidth) is composed of two separate unit HEMT device and combined with a CPW Y-junction. If more devices were to be combined in parallel, higher N-way combiners (junctions) with low loss in CPW must be carefully designed.

IV. PA MEASUREMENT

On-wafer small-signal S-parameter measurements were performed on the MMIC PAs for screening purposes before the

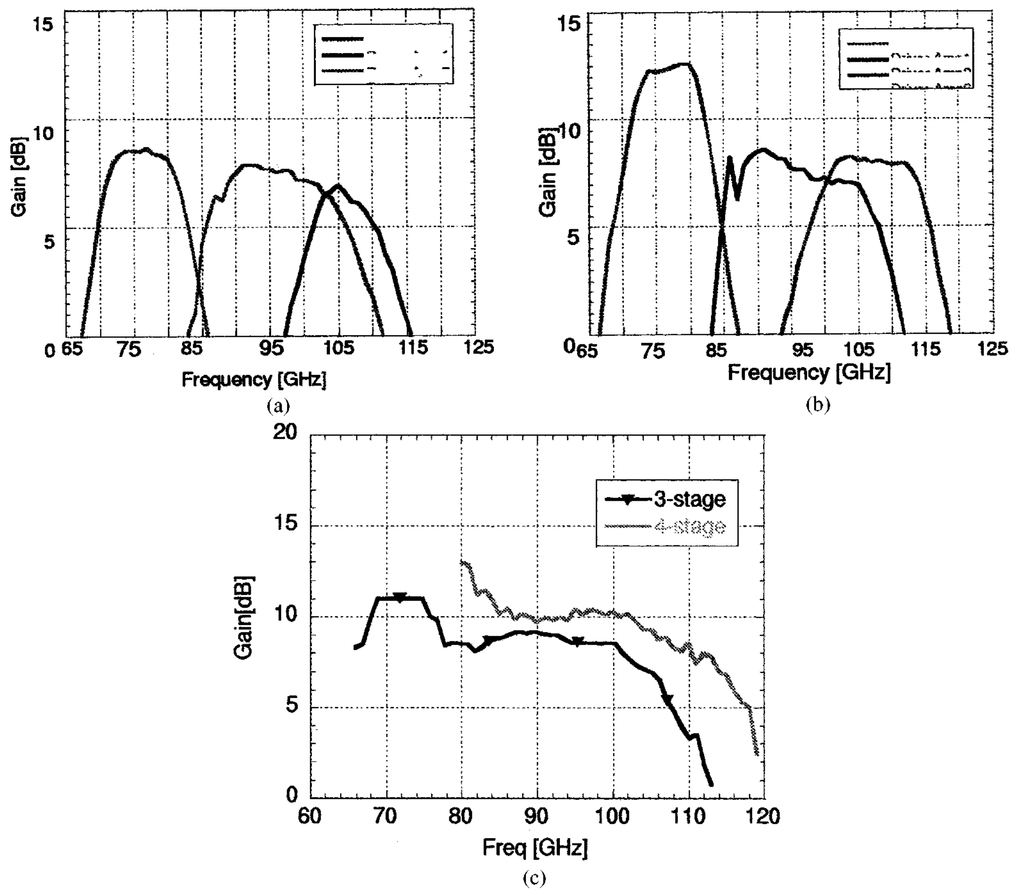


Fig. 6. Measured on-wafer small-signal gain versus frequency of the: (a) three W-band PAs, (b) three W-band driver amplifiers, and (c) two CPW driver amplifiers.

wafer was diced. The block diagram of the test set is depicted in Fig. 4(a). Standard vector-network analyzers from HP and Anitru can be readily adapted to high frequencies with external extenders. The extenders can be fabricated in waveguide band through 220 GHz. Fig. 4(b) depicts a photograph of this 70–115-GHz wafer probe test set. This test set has full two-port S-parameter test capability with large dynamic range [11].

For the output power measurement, W-band on-wafer pulsed-power capability has been demonstrated to resolve the thermal issue and the correlation with in-fixture was also verified [12]. However, there are two critical requirements, i.e., the W-band pulser and power drive for the test set must cover the probe path loss with enough bandwidth. Both of them may not be easy to acquire at this frequency. Therefore, the PA chips were tested in a WR-10 waveguide module for the output power performance. The waveguide-to-microstrip-line transitions used in the PA modules are longitudinally mounted in the waveguide, meaning that the surface of the alumina substrate aligns along the direction of propagation of the waveguide [10], as shown in Fig. 5(a). This transition demonstrated a total loss of 1 dB and a return loss of better than 15 dB from 85 to 107 GHz for a pair of back-to-back transitions. The drawing of the module housing design is depicted in Fig. 5(b) and the photographs of a CPW driver amplifier chip mounted in the module are shown in Fig. 5(c). The power test set utilized a backward wave oscillator (BWO) as the tunable source at the input. A calibrated power meter with W-band sensor attachment was used to measure the output module. The extra power required at the input port for high output PAs evaluation are obtained by cascading the associated driver or PA modules in the same frequency bands, as shown in Fig. 5(d).

V. Measurement Results

The MMIC PAs were first tested for gain using on-wafer small-signal S-parameter measurements. A measured typical small-signal gain of at least 8, 7, and 4 dB is achieved at 72–81, 90–101, and 100–113 GHz, respectively, at a drain voltage (V_d) of 1.5 V with a total drain current (I_d) of 500 mA for the three PAs, as shown in Fig. 6(a). The three microstrip-line driver amplifiers depict higher gain performance of 12, 7, and 7 dB, as shown in Fig. 6(b), at $V_d = 1.5$ V and $I_d = 250$ mA. Fig. 6(c) presents the small-signal gain performance of the CPW medium power driver amplifiers from 65 to 115 GHz. The three-stage design demonstrated small-signal gain of more than 8 dB from 65 to 100 GHz at $V_d = 2.5$ V and $I_d = 150$ mA, while the four-stage design showed more than 10-dB gain from 80 to 100 GHz and greater than 8 dB up to 110 GHz at $V_d = 2.5$ V and $I_d = 210$ mA.

For the PA module testing, individual PA modules were evaluated for output power. The measurements were performed at $V_d = 2.5$ V to maximize output power and bandwidth of the chips. The driver amplifiers showed up to 100 mW of peak output power, and the PAs typically exhibited 200 mW of output

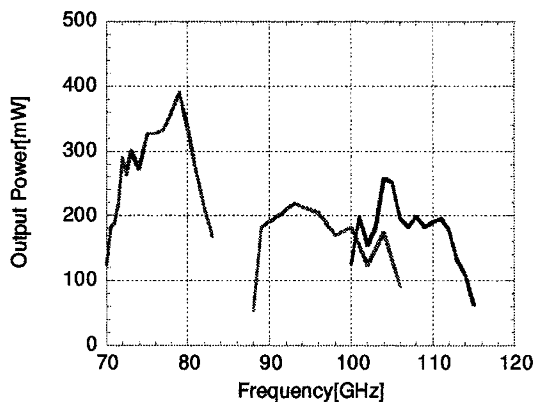


Fig. 7. Output power versus frequency plot of the three W-band packaged PAs.

power. The amplifier modules were then cascaded in order of increasing output stage gate periphery: the driver (640 μm) was followed by a PA (1.28 mm). Fig. 7 shows the maximum output power performance versus frequency at the output of the cascaded modules. Three frequency bands are covered in three separate pairs of modules. Each amplifier chain demonstrated at least 22 dBm (158 mW) in the frequency range it covers. The 100–113-GHz PA has a peak power of greater than 250 mW (25 dBm) at 105 GHz, which is the best output power performance for a monolithic amplifier above 100 GHz to date. It is also noted that the waveguide transition has an insertion loss of 0.35 dB up to 107 GHz, and 0.5 dB from 107–115 GHz [10]. For the output power results at the MMIC chip end, the numbers mentioned above need to be corrected by this loss factor.

Typical power-added efficiencies for an amplifier chain are in the range of 4%–9%, with dc input power levels of 2.5–3.5 W. For example, as the results indicated, by the evaluation of a chain of the 72–81-GHz driver amplifier module (APH350C) cascaded with PA module (APH351C). Fig. 8(a) shows the small-signal gain and return-loss responses of this cascaded chain from 65 to 118 GHz. It demonstrates a peak gain of 29 dB at 75 GHz and greater than 24 dB from 72 to 81 GHz. The bias condition is $V_d = 2.5$ V with $I_d = 250$ and 500 mA for the driver amplifier and the PA, respectively. The output power versus frequency is already shown in Fig. 7, and the drain efficiency from 70 to 83 GHz is plotted in Fig. 8(b).

Another chain of 90–101-GHz PA modules, formed by cascading a CPW medium driver amplifier module (APH352C), a driver amplifier module (APH348C), and PA (APH349C) module. The small-signal gain and return loss from 80 to 120 GHz is presented in Fig. 9(a) with $V_d = 2.2$ V and total $I_d = 800$ mA. The peak gain is 31.2 dB at 92.6 GHz and greater than 20 dB from 88 to 102 GHz. The output power and gain versus input power at 93 GHz are depicted in Fig. 9(b). It shows a 3-dB compression at 16-dBm output power and a saturation output power (P_{sat}) of 24.5 dBm.

In the output power measurements and the small-signal gain measurements, 1–5 dB of ripple is present in the cascaded-module experimental data, with a periodicity of approximately 3 GHz. To explain this phenomena, we will discuss the problem of cascading two amplifier modules together: a microstrip driver amplifier followed by a microstrip PA.

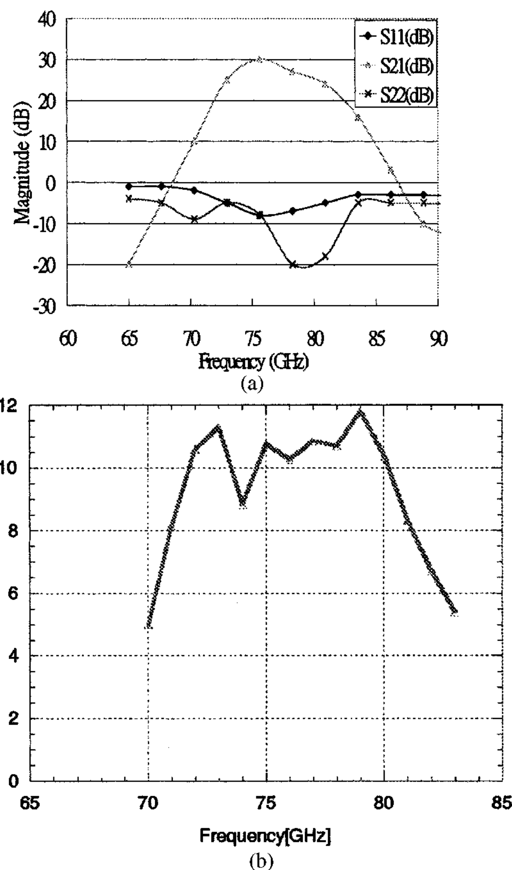


Fig. 8. Performance of the 72–81 GHz amplifier chain (microstrip driver + PA). (a) Small-signal gain and return loss versus frequency. (b) Drain efficiency versus frequency.

Both modules include a waveguide input, input alumina probe transition, microstrip chip, output alumina probe transition, and output waveguide, as shown in Fig. 5(c). A small mismatch between the chip and probe transition at the output of the first module, and another mismatch between the probe transition and chip at the input of the second module, is responsible for reflections with a periodicity related to the electrical length between the two chips. In Fig. 10(a), we present the theoretical gain of the two amplifier modules cascaded together, illustrating the ripple present in small-signal gain. For the prediction, the theoretical probe transition data [10] was used to simulate the effect of the probe, the power–current definition of waveguide impedance (Z_{pi}) was used to simulate the length of waveguide between the chips, and the measured on-wafer gain of two representative amplifier chips were used to model the PA chips. Fig. 10(b) shows the experimental result of cascading the modules. While Fig. 10(a) and (b) does not agree *exactly*, our crude theoretical model predicts the ripple effect reasonably well. The differences between theory and experiment most likely have to do with chip-to-chip variation (the on-wafer data is taken from a different chip than the packaged chip), as well as tuning effects present in each module due to variations in packaging. In order to reduce this ripple, a better match must be provided between the PA chip inputs and outputs, and the probe transition. Improving the return loss of the chips is also likely to reduce the ripple.

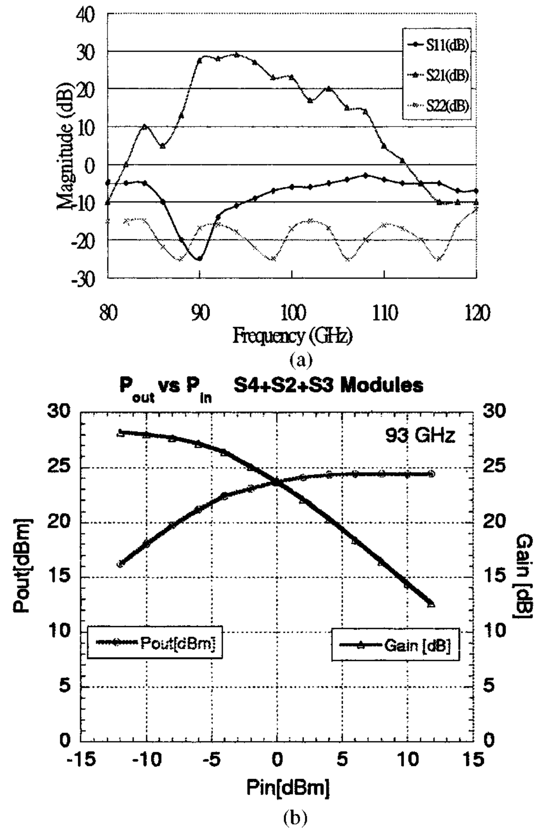


Fig. 9. Performance of the 92–101-GHz amplifier chain (CPW driver + microstrip driver + PA). (a) Small-signal gain and return loss versus frequency. (b) Output power and gain versus input power at 93 GHz.

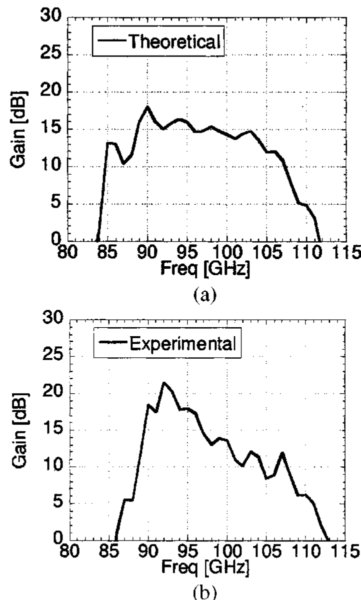


Fig. 10. Small-signal gain of a microstrip-line driver-amplifier module cascaded with a microstrip-line PA module. (a) Theoretical gain using simulated probe transition. (b) Measured gain.

A 89–105-GHz amplifier chain was cooled to 100 K using a cryogenic refrigerator to test the cryogenic performance. The chain consisted of one microstrip-line driver amplifier followed by a microstrip-line PA. A BWO supplied the input RF power. A marked increase in the observed output power was observed

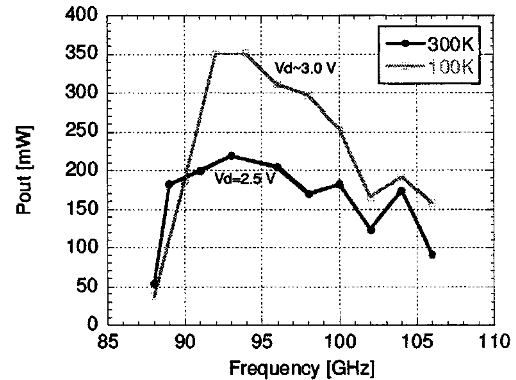


Fig. 11. Output power of a 89–105-GHz chain of two amplifiers as a function of frequency, measured at 100 and 300 K.

upon cooling the amplifier modules. Fig. 11 shows the comparison between the room-temperature output power measurement and the 100-K measurement. A slightly higher drain voltage was used for the measurement at 100 K, to maximize the peak output power. A peak power of 350 mW is observed at 93–94 GHz for the 100-K measurement, an increase of over 100 mW. A 1–2 dB increase was observed across the band. An additional experiment was performed where the drain voltage was increased to 5 V with the amplifier kept at 100 K. We observed that the output power increased to 0.5 W at 94 GHz. This result is in contrast with the room-temperature data, where increases in drain voltage did not result in increases in output power beyond $V_d =$ 2.5–3 V. When cooled, the PAs can be operated at a higher drain voltage and drain current and, thus, results in approximately a factor of two increase in output power over the room-temperature data. We did observe that when a large RF signal was applied to the PAs at $V_d = 5$ V, the amplifier failed due to excessive gate leakage current. Fortunately, we can run the amplifiers well below the breakdown condition and still meet the output power requirements.

VI. Applications to FIRST

The PA results are particularly significant for the needs of FIRST applications. Foremost, referring to Fig. 7, a single chain of a driver amp cascaded with a high-power chip produced more than 100 mW from 70 to 83 GHz (about 17% bandwidth), and over 300 mW from 75 to 80 GHz. The peak output power for this chain occurred at 79 GHz, with 390 mW of output power. The high power between 79 and 80 GHz is particularly significant for the 1.9 THz (79 GHz $\times$ 2 $\times$ 2 $\times$ 3 $\times$ 2) line of the fine structure transition of singly ionized carbon (CII), to be observed with a heterodyne instrument for FIRST (HIFI). Other significant results include a record power bandwidth of greater than 100 mW from 89 TO 105 GHz, and better than 100 mW from 100 to 114 GHz. A few selected spectral lines of interest to FIRST, along with their frequencies, required PA band, and current state-of-the-art PA results, are shown in Table II.

VII. Summary

In this paper, we have presented a set of monolithic W-band PA modules using 2-mil 0.1-μm AlGaAs/InGaAs/GaAs PM T-gate power HEMT MMIC production process technology

TABLE II
A FEW SELECTED SPECTRAL LINES OF INTEREST TO FIRST, ALONG WITH THEIR FREQUENCIES, REQUIRED PA BAND, AND CURRENT STATE-OF-THE-ART PA RESULTS. SINGLY IONIZED NITROGEN (NII), SINGLY IONIZED CARBON (CII) SINGLY IONIZED NITROGEN (NII), DEUTERATED HYDROGEN (HD)

Spectral Line	Frequency [THz]	Power Amp Frequency Required [GHz]	Pout[mW]
NII	1.461	91-92	200-230
CII	1.900	79-80	340-400
NII	2.459	102-103	100-150
HD	2.674	111-112	160-190

for LO sources, which are useful for astronomical telescope applications. Measurement results show that at least 22-dBm output power can be provided for the frequency bands of 72–81, 90–101, and 100–113 GHz. The 100–113-GHz PA and driver amplifiers are the first reported MMIC PAs above 100 GHz. The MMIC design, module assembly, as well as the system application of these modules have been discussed in this paper.

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Alejandro Peralta has been involved in Research and Development with three companies over the past nine years. He was with the Automotive Division, TRW Inc., where he heavily supported product development engineering and packaging engineering on air-bag crash sensors. He then joined the TRW Space and Defense Division, where he performed on-wafer testing and packaging of MMIC low-noise and PAs. In 1998, he joined the Jet Propulsion Laboratory (JPL), Pasadena, CA, where he continued his involvement on millimeter-wave amplifier testing and packaging. He is currently a Product Development Engineer and Prototype Coordinator with the BEI Duncan Electronics Division Sensors and Systems Company.

Mr. Peralta's research resulted in TRW receiving the FORD Q1 Award. He was also the recipient of a Technical Award of Excellence.

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Y. C. Leong, photograph and biography not available at time of publication.

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In 1994, he joined the Hughes Aircraft Company, where he participated in the development of GaAs PM HEMT and HBT technologies for X-band high-power and high-efficiency amplifier applications. In October 1995, he joined the Space and Electronics Research Group, TRW Inc., Redondo Beach, CA. Over the past five years he has been responsible for the development of InP-based HEMTs for high-power and high-efficiency applications. His effort has led to the demonstration of world-record InP HEMT MMIC PAs at 62 and 94 GHz. He is currently in charge of TRW's GaAs HEMT production technology. His research interests cover device physics, device and MMIC manufacturing technology, and design of MMICs and modules.

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In 1991, he joined the Advanced Microelectronics Laboratory, TRW, Redondo Beach, CA, as a Product Engineer, where he was involved in the research, development, and production of advanced GaAs- and InP-based HEMT device and MMIC technologies into various military and commercial MMW applications. Since 1994, he has been the Principal Investigator for an advanced HEMT research and development project at TRW. Since 1997, he has been the Manager for the HEMT MMIC Products Section, TRW. He has authored and co-authored over 100 papers and conference presentations in the area of advanced GaAs- and InP-based device and circuit technology, establishing world-record performance for low-noise amplifiers, high-frequency amplifiers and PAs.

Dr. Lai was the recipient of three TRW's Chairman's Award for Innovation in 1996 and 1999 for his work on GaAs power HEMT MMIC development and InP HEMT MMIC development. In 1998, he was the recipient of a Paper of the Decade Award presented at the International Conference on InP and Related Materials. In 1999, he was the recipient of the Jet Propulsion Laboratory Award for Excellence for his work on InP HEMT MMIC development.