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ABSTRACT

A charge coupled device designed for celestial spectroscopy has achieved readout noise as low as 0.6 electrons rms. A non-destructive output circuit was operated in a special manner to read a single pixel multiple times. Off-chip electronics averaged the multiple values, reducing the random noise by the square root of the number of readouts. Charge capacity was measured to be 500,000 electrons. The device format is 1600 pixels horizontal by 64 pixels vertical. Pixel size is 28 microns square. Two output circuits are located at opposite ends of the 1600 bit CCD register. The device was thinned and operated backside illuminated at -110 degrees C. Output circuit design, layout, and operation are described. Presented data includes the photon transfer curve, noise histograms, and bar-target images down to 3 electrons signal. The test electronics are described, and future improvements are discussed.

1. CCD READOUT CIRCUIT NOISE

The state of the art silicon substrate quality and wafer fabrication can combine to produce CCD registers with nearly perfect charge transfer efficiency (CTE)[1]. By cooling such a CCD to a sufficiently low temperature to reduce the dark current, single photo-electrons can be transferred to the CCD output circuit. Readout noise then limits the signal to noise ratio for very low background CCD applications. In this paper we explain the problems and a solution for obtaining sub-electron readout noise. The two most common forms of CCD output circuits, floating diffusion and floating gate, are considered for sub-electron noise operation. Other output circuits have been proposed[2], but require additional wafer processing complexity, and so are not likely to be adopted by manufacturers of large format CCD's.

1.1 Floating diffusion output circuit

Electrons that are clocked out of the CCD onto the output node cause a voltage change according to the equation $Vo = qN/C$ where q is the electron charge, N is the number of electrons, and C is the output node capacitance. In general, minimizing C increases the output sensitivity and reduces the noise, as we will show later. The minimum value of C is limited by the layout rules which are set by mask alignment tolerances and lithography limitations.

1.2 Floating gate output circuit

Another type of output circuit is the floating gate (FG) output circuit[3], which also exists in "distributed" form using multiple floating gates. The resettable FG output has a slightly higher output node capacitance than the FD output due to the additional capacitance of the floating gate over the CCD channel. The floating gate cannot be made arbitrarily small, because it must be large enough to hold the desired maximum charge. For the FD output, the output node capacitance can be made as small as the layout rules allow. For the same output MOSFET, therefore, the higher node capacitance of the FG output will result in a slightly higher noise level than for the FD output. The FG output has the option of being operated with a reset pulse every line of pixels instead of every pixel. For lowest noise, however, the correlated double sampler (CDS) must still sample the output before and after each pixel output, in order to suppress the MOSFET 1/f noise as much as possible.

1.3 Noise reduction limit

For either FD or FG outputs, if the output MOSFET gate area is decreased in order to increase the CCD output sensitivity, the 1/f noise component increases inversely proportional to the MOSFET gate area[4]. At high clock frequencies the 1/f knee is typically well below the clock rate. Since 1/f noise is not a problem at high frequencies, much progress has been made in reducing the readout noise of outputs operating at multi-megahertz clock rates by increasing the sensitivity. These same output circuits suffer greatly from 1/f noise if operated at kilohertz data rates. The 1/f noise problem is illustrated in figure 1. The input noise of a MOSFET with a 20KHz

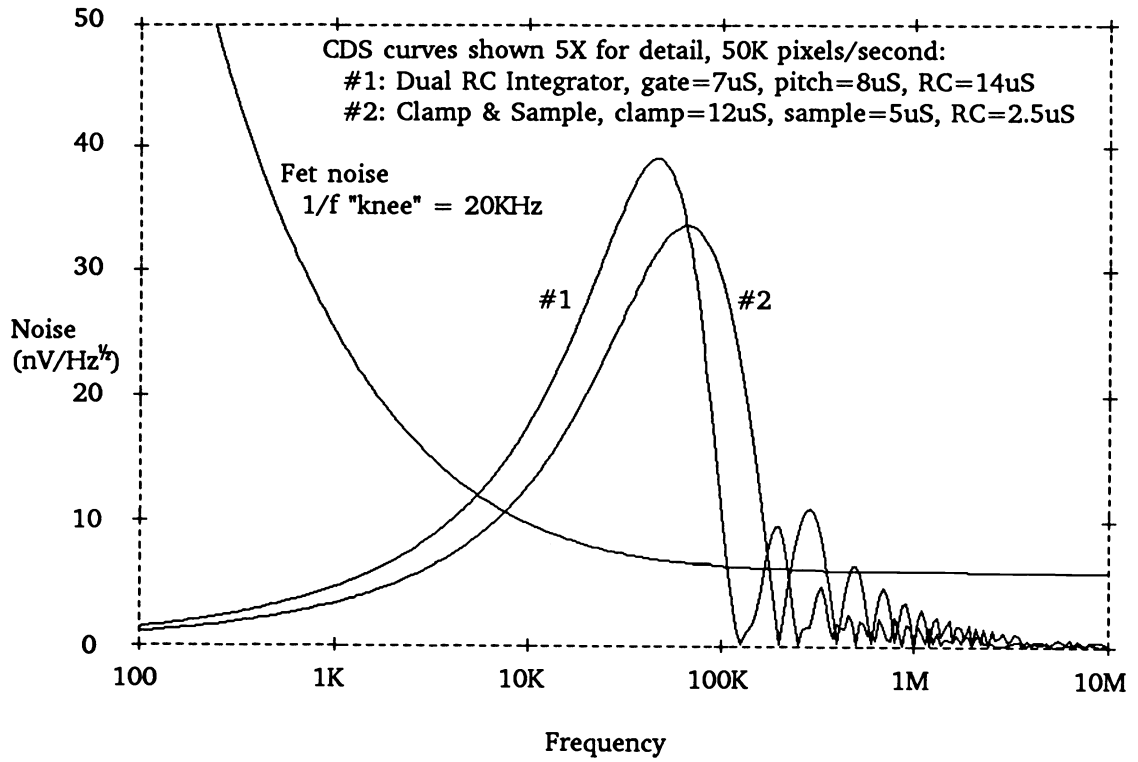

Figure 1. MOSFET noise and CDS response

1/f knee is plotted along with the resulting noise spectrum after CDS. The two curves show the clamp-and-sample and the reset integrator CDS response normalized to an equal signal level for a pixel rate of 50KHz. Appendix A explains how the curves were calculated. With either type of CDS, if the operating frequency is reduced from 50KHz, the CDS response peak will increasingly overlap with the 1/f noise, preventing a significant

decrease in the readout noise. If MOSFET's could be made (compatible with CCD wafer processing) without 1/f noise, then sub-electron readout noise would be rather easy to obtain. Since without 1/f noise the readout noise would vary inversely proportional to the square root of the clock rate, an output achieving 5 electrons noise at 50KHz could reach 1 electron noise at (50KHz)/(5×5) or 2KHz. With a special output circuit and the appropriate signal processing techniques, the ever-present 1/f noise barrier can be broken, as will now be described.

2. AVERAGING FLOATING GATE OUTPUT CIRCUIT

The approach taken in this work was to surround a FG output circuit with CCD gates to enable repetitive, non-destructive readout of the signal charge. Thus, the output circuit timing can be adjusted such that the CDS response is above the MOSFET 1/f noise regime, and multiple readouts of the same signal can be averaged off-chip to reduce the noise. For a device cooled below -100 degrees C, the slowest tolerable frame rate will determine the maximum number of averages, not a theoretical limit. For applications that cannot be cooled sufficiently, dark current generation will be the limit. A dark signal of only one electron every four pixels is 0.25e average, or 0.5e rms noise.

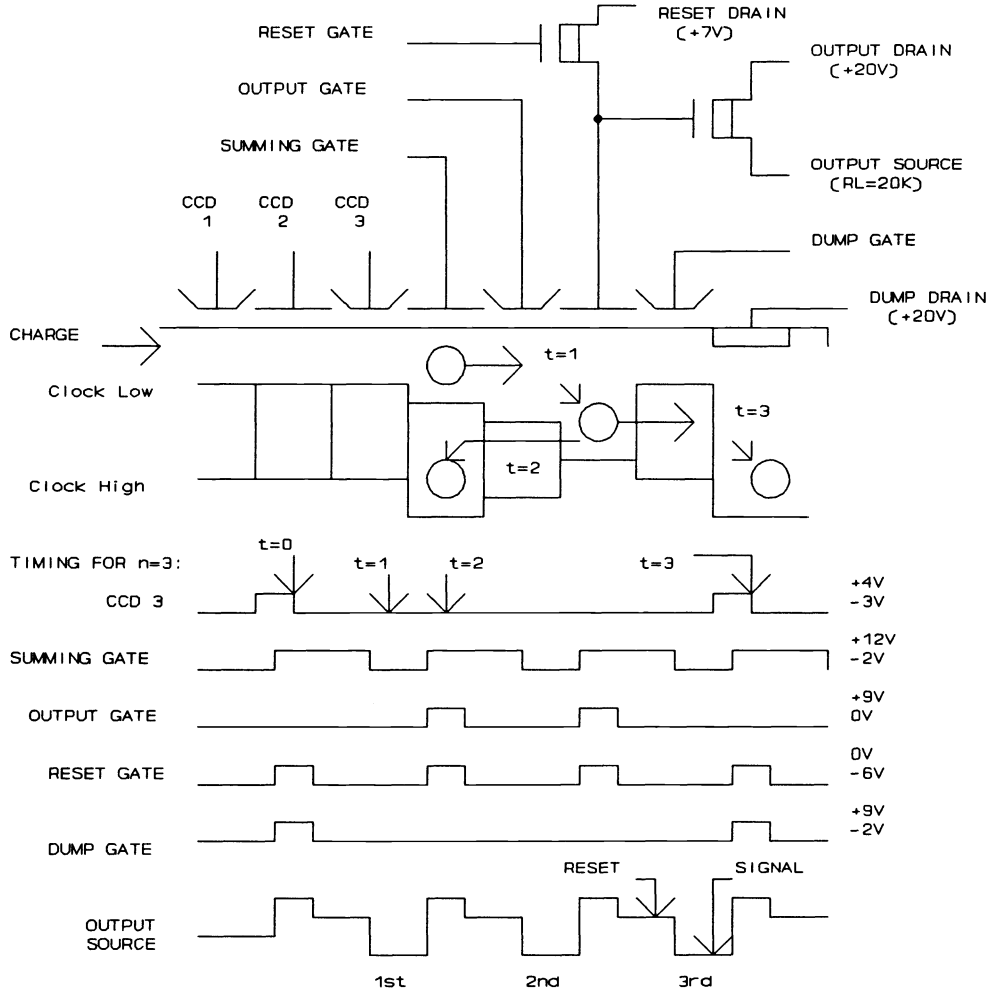

Figure 2. Output circuit operation

2.1 Circuit operation

The averaging FG output circuit is shown schematically in figure 2, along with the clock timing and clock voltages. The charge sensitive node is a floating gate over the CCD channel, connected to the gate of a MOSFET source follower. Another MOSFET is connected as a switch to the floating gate in order to reset it to the reset drain (RD) voltage. On the input side of the floating gate is the CCD output gate (OG). Between the OG and the CCD phase clocks is the summing well gate (SW). In operation, charge is clocked out of CCD phase 3 into the summing gate, while the reset MOSFET sets the floating gate to the RD voltage (t=0). The off-chip CDS then captures the reset level. Then SW is clocked low, forcing the charge over OG and under the floating gate (t=1). Because the gate is floating at this time (reset gate off), the voltage on the gate decreases in proportion to the number of electrons in the charge packet. The CDS captures the signal level and subtracts the reset level. During the next reset gate (RG) pulse, OG is clocked high, transferring the charge back into SW (t=2). After the desired number of readouts of one pixel, the dump gate (DG) is pulsed and the charge is discarded into the dump drain (DD) at t=3. The floating gate is reset every readout to precisely control the DC level of the gate and add immunity to parasitic clock coupling.

2.2 Design and layout considerations

Figure 3 shows the actual mask layout of the array's bottom-left output circuit, with charge traveling from right to left in the CCD channel. In order to minimize the floating gate node capacitance, the CCD channel width is reduced from 60μm first to 30μm and then to 15μm. The output MOSFET has a channel width of 100μm and a gate length of 9μm. Two levels of polysilicon electrodes are required with a total of only six mask layers for the circuit (the sixth layer defines the bonding pads and is not required in the area shown). Compared to a FD output, two leads (dump gate and dump drain) have been added. Usually the dump drain can be connected to the output drain.

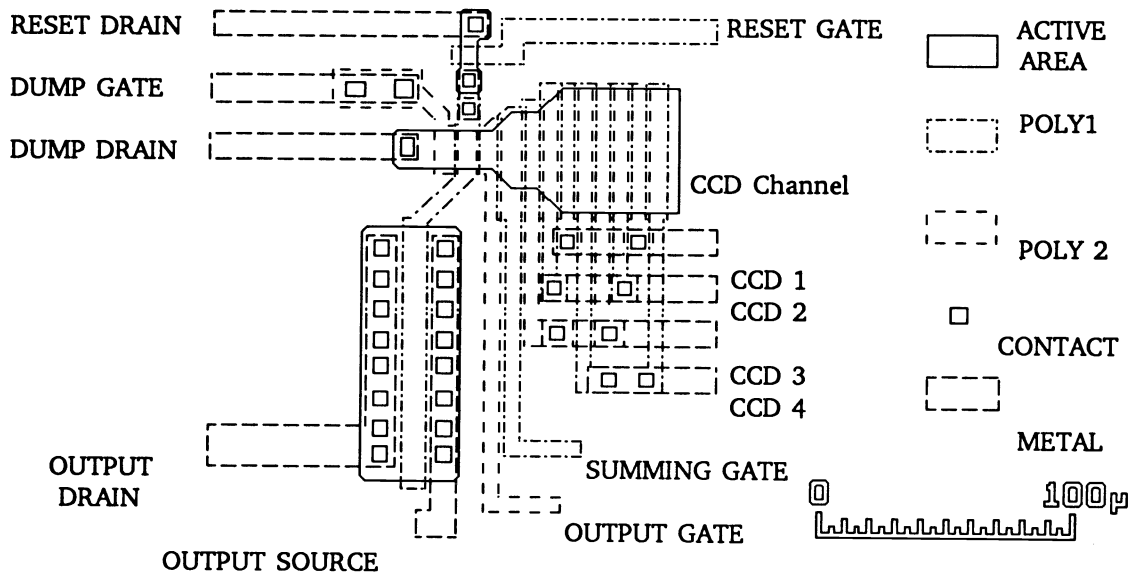

Figure 3. Output circuit mask layout

Design equations that could accurately predict the readout noise level would depend heavily on the details of the MOSFET white and 1/f noise behavior. Since this in turn varies due to wafer processing parameters, such as the surface state density, these equations are only approximations based on empirical calibrations. As a design aid, though, even a simple equation is valuable. Consider the readout noise N_R (electrons) expressed as the total

MOSFET equivalent input noise voltage V (not versus frequency) divided by the output conversion gain G (volts/electron):

$$N_R = V/G = (CV)/q \quad (1)$$

where C is the total output node capacitance consisting of 1) the fixed parasitic capacitance Cp independent of MOSFET geometry, 2) the total capacitance that depends on the MOSFET gate width (primarily the MOSFET drain and source to gate edge capacitance) $W\times(C_1)$ (W=gate width), and 3) the total capacitance that is a function of the MOSFET gate area (primarily the MOSFET gate area capacitance) $W\times L\times(C_2)$ (L=gate length). The MOSFET noise voltage is[4]

$$V = [8KTB\alpha/(3gm)]^{1/2} + 1/f \text{ term} \quad (2)$$

where $\alpha \geq 1$ is an empirical constant that depends on the wafer process, T=temperature (Kelvin), K=Boltzmann's constant, B=bandwidth, and

$$gm = W\mu(C_2)Vg/L \quad (3)$$

where μ=mobility and Vg=gate voltage above threshold. Combining equations 1 to 3 yields

$$N_R = (Cp/W + (C_2)L + C_1) \times \{[8KTB\alpha WL/(3\mu(C_2)Vg)]^{1/2} + kf/L\}/q \quad (4)$$

The 1/f noise contribution is set by the parameter kf. If we fix all the parameters except for W, and start with W≈L, the Cp/W term dominates and the noise is relatively large. As W increases, the noise decreases until Cp/W is dominated by $(C_2)L$, at which time the square root of W term causes the noise to gradually increase. This is shown in figure 4a, where equation 4 is plotted for three values of kf (T=170K, α=3, μ=0.15m^2/V-s, Vg=1, C_2=1.5e-4F/m^2, C_1=3e-10F/m, Cp=8e-14F, B=60KHz). There is a broad minimum in the noise for W≈10×L, and it is less noisy to err on the side of W too large than to err on the side of W too small. A similar situation is observed if all the parameters are fixed except for L, as is shown in figure 4b. As the gate length is reduced below 4μm, short channel effects cause an increase in drain conductance, and excess white noise is encountered. A typical minimum size for a buried channel FET is W=25μm, L=4μm.

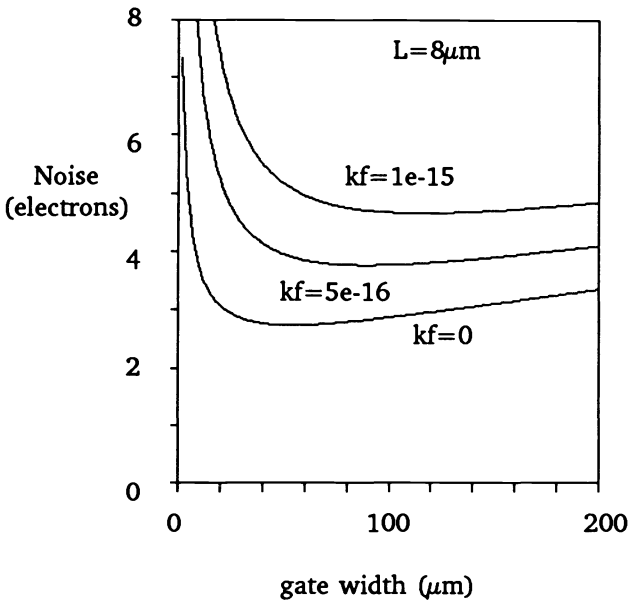

Figure 4a. Noise versus gate width

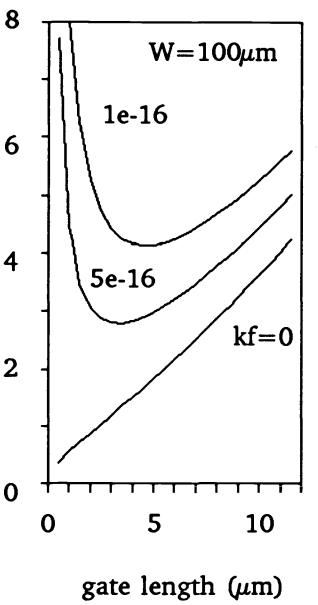

Figure 4b. Noise versus gate length

A general procedure for designing the averaging floating gate output circuit can be described in four steps:

1) Determine from the application what the maximum number of electrons capacity (N) is required. Find the effective gate capacitance (Ce) of the CCD electrode (oxide capacitance and channel capacitance in series). This can be found by measuring the charge output versus gate voltage of a fill-and-spill input circuit. A typical value is one third of the gate oxide capacitance. Next choose the voltage on RD high enough above the low level of OG so that the floating gate can hold the maximum charge. Do not make RD too high or an excessive voltage will be required on the summing well (SW) to transfer the charge back out. However, at least about 6 volts is required in order for the buried channel reset FET to shut off. A typical value for RD is 7 volts. A typical low level for OG is zero. Then set an upper limit for the value of the sensitivity G. The value of Ce is typically 1.5e-16 F/μm^2. Then the required floating gate area is

$$A = qN/[Ce(RD - OG - N \times G)] \quad (5)$$

For N=500,000 electrons, RD=7, OG=0, G=2e-6, A=89 square microns (the area of the floating gate in figure 3 is 130μm^2). It is best to make the floating gate a little larger and approximately square, to maximize the area to perimeter ratio (less parasitic capacitance).

2) From the layout, estimate the total capacitance of the floating gate node, not including the output MOSFET. Include the floating gate itself, any wiring, the electrode overlap capacitance to OG and DG, the reset FET source capacitance to substrate and RG.

3) Choose a MOSFET gate length and width that will minimize the white noise, keeping the W/L ratio ≥6. The effective gate capacitance should dominate the total parasitic capacitance found in step 2. For extremely small CCD's operating at very high frequencies, making the FET surface channel and operating at a lower drain voltage enables the smallest values of W and L, at the expense of complicating the wafer process. For relatively large pixel CCD's with higher parasitic capacitance (such as the one in figure 3), increase the FET size. This will reduce the output circuit sensitivity and the frequency response but will result in lower readout noise because the FET will have less white and 1/f noise.

4) Operate the circuit at a high enough frequency such that the 1/f noise contribution is minimal, and use averaging to reduce the effective noise level and return to the desired data rate. If the electronics has a readout rate limit, it is best to use a large enough FET to keep the 1/f knee below the CDS response at that operating limit, even though a smaller FET could be used to gain sensitivity.

In general, large signal handling output circuits will always have more readout noise than small, more sensitive circuits. The larger circuits will also be limited to a lower operating frequency. One possible compromise is to place two different output circuits on the CCD, one for small signals and one for large signals. The user can then wire whichever suits the particular application.

3. 1600 BY 64 PIXEL ARRAY

3.1 Architecture

The schematic of the CCD array is shown in figure 5, incorporating two of the averaging FG output circuits. Pixel size is 28 microns square. The left and right sides of the chip are mirror images of each other. Each side is 800 pixels horizontal by 64 pixels vertical. The two sides are connected such that the device can be operated as one 1600 by 64 array using either output if desired. The array CCD is 3 phase 3-level polysilicon while the serial CCD is 4 phase 2-level polysilicon. It was felt that a 4 phase serial CCD would have better CTE than a 3 phase design. However, it was felt that a 3 phase array would have higher manufacturing yield than a 4 phase array. In addition, this allowed the multi-pinned implant (for inverted operation)[1] to be done under phase 3 (polysilicon 3) as a blanket implant after poly 1 and 2 were present, thereby avoiding an extra mask step to

restrict the implant to only the array CCD. The output MOSFET size was chosen for low 1/f noise to be compatible with 50KHz readout rate. The floating gate area was chosen large enough to hold 500,000 electrons.

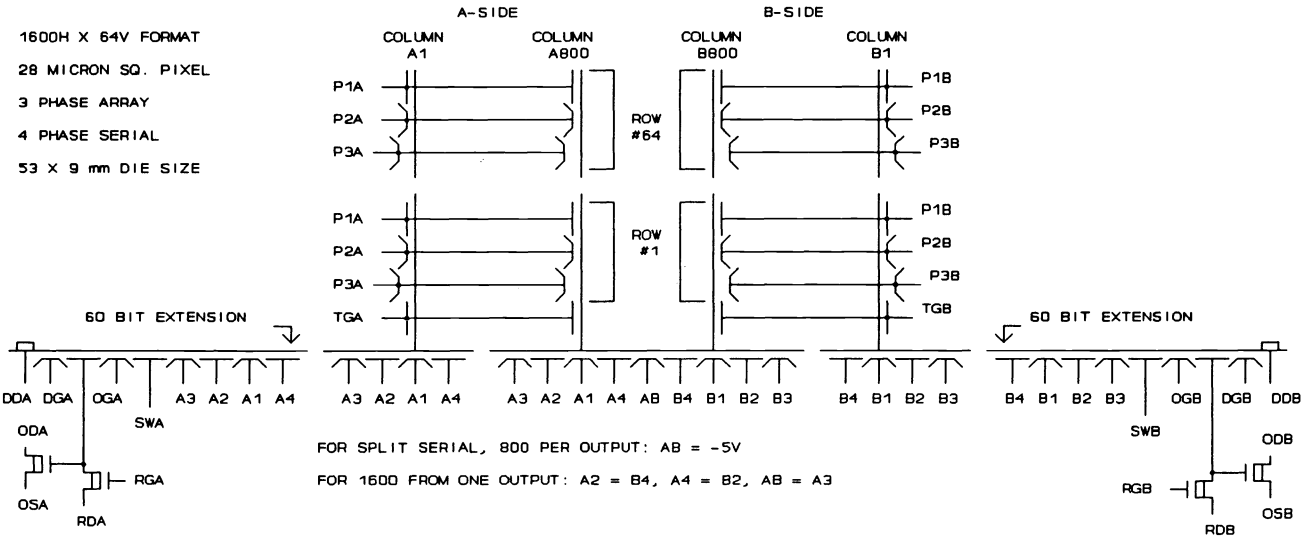

Figure 5. Device schematic

3.2 Fabrication and thinning

The devices were fabricated with an oxide-nitride gate dielectric, triple-polysilicon, NMOS buried channel CCD process. Channel formation was by phosphorous ion implantation (1.6e12 dose) and thermal anneal to produce a 0.5μm channel depth. MOSFET threshold voltage was about -10 volts. Substrates were 70-100 ohm-cm P-type epitaxial layer on P+ wafers. Thinning was accomplished after wafer sawing, with a peripheral border of about 2mm waxed to prevent etching. Volume ratio 1:1:8 of 50% HF, 50% nitric, and glacial acetic acid, respectively, was used as an etchant. Backside oxide was grown in ambient atmosphere at 250 degrees C for 36 hours. Backside charging was accomplished by UV illumination from a mercury discharge lamp during dewar evacuation.

3.3 Test methods

Device testing was done with the CCD mounted in a shielded dewar. A low noise preamplifier was mounted inside the dewar, but was not cooled down all the way to the device temperature. This is because it contained bipolar components. Also inside the dewar, next to the device and operated cold, were the clock drivers for OG, DG, and RG. These circuits used only CMOS components and hence were not degraded by low temperatures. The reset integrators in the CDS are of the form with the capacitor connected to ground, rather than in the feedback loop of an operational amplifier. This was easier to design for extended high frequency operation. The noise calculations are in appendix A and the circuitry is shown in appendix B.

The data was reduced and plotted on a Hewlett Packard A900 computer. Images were passed to an IBM ps/2 equipped with a 1024 × 768 by 64 gray level (or 256 pseudo-color) display (IBM 8514A). Hardware and software limitations of the system prevented imaging of the 800 by 64 format with more than 8 averages. Readout rates before averaging of about 60KHz were used. Typical operating temperature was -110 degrees C.

3.4 Test data

The photon transfer curve of the 1600 by 64 is shown in figure 6. Under flood illumination, rms noise is plotted versus signal level. The noise level ranges from 4.8 electrons rms for no averaging down to 1.2 electrons at 16 averages. Charge capacity was measured to be in excess of 500,000 electrons. The preamplified signal was attenuated as needed prior to CDS to maintain the signal within the 12-bit A/D range.

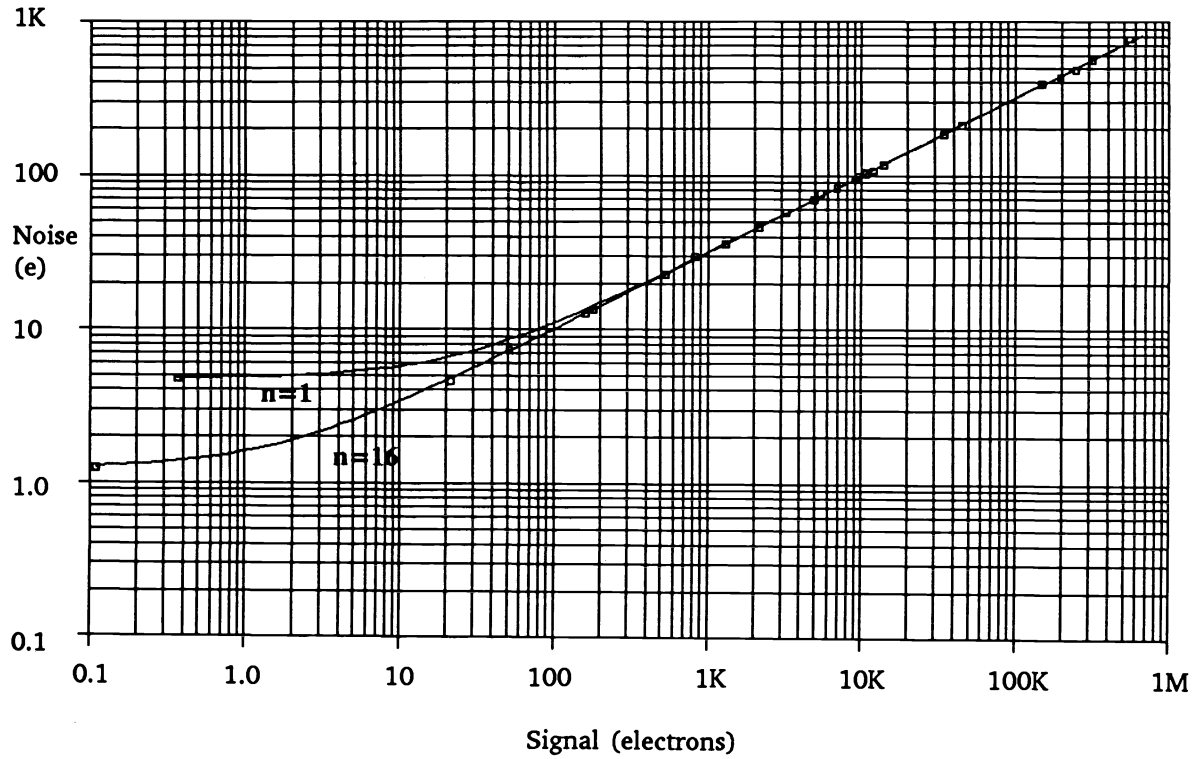

Fig 6. Photon transfer curve (1600 by 64 device)

Figure 7 shows noise histograms for different numbers of averaging. The curves are normalized for the same peak value, to show the decreasing width as the number of averages is increased. This data was from a 256 by 64 test array that had the same output circuit as the 1600 by 64. At 256 averages, 0.5e rms noise was achieved.

Figure 8 shows the relative quantum efficiency for the backside illuminated 1600 by 64 device. The absolute QE is not quoted because when calculated at 500nm, it was slightly above the theoretical value. However, the shape of the curve indicates a QE-pinned condition due to the charged backside oxide.

Figure 9 shows a series of images at 1, 2, and 8 averages for each of three illumination levels of 3, 4.5, and 11 electrons. The interesting portion of the image of the 1600 by 64 is shown (about 300 by 64), because the bar target could not cover the entire length of the device with the test optics. The top three photos are for a signal level of 11 electrons. In the middle three pictures the signal level has been reduced to 4.5e. The bottom three pictures show that a 3e image can be read out with minimal CCD distortion. The benefit of averaging can be observed. In these tests, the 1600 by 64 was operated backside illuminated with a pulsed 660nm red LED. The CCD was continuously clocked at 62.5KHz. The CDS gate width was 5μS, spaced 6μS between reset and signal samples.

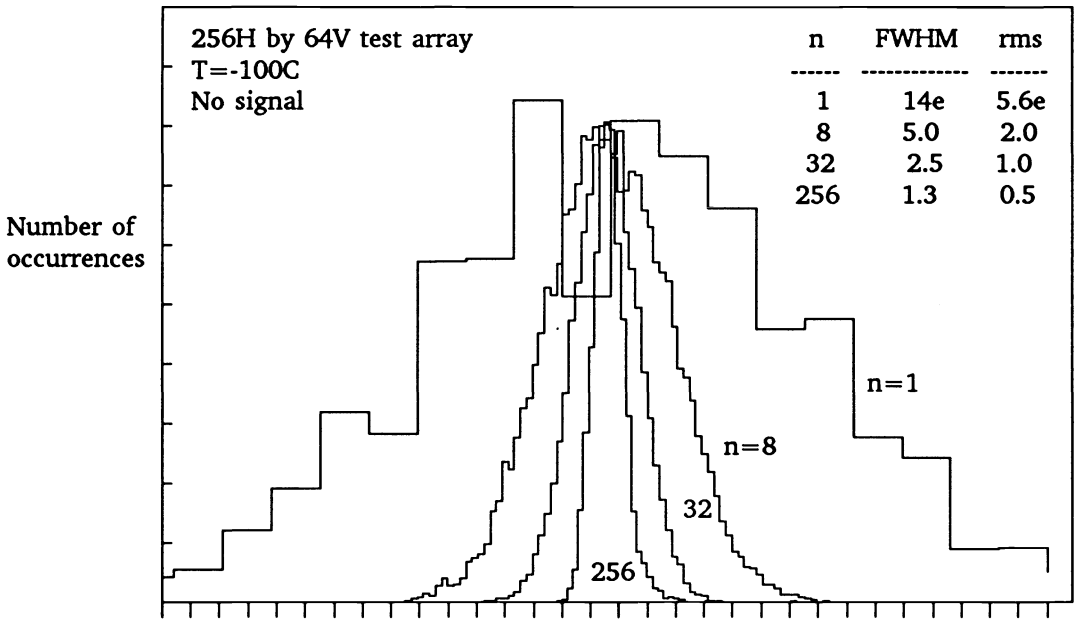

Figure 7. Readout noise histograms

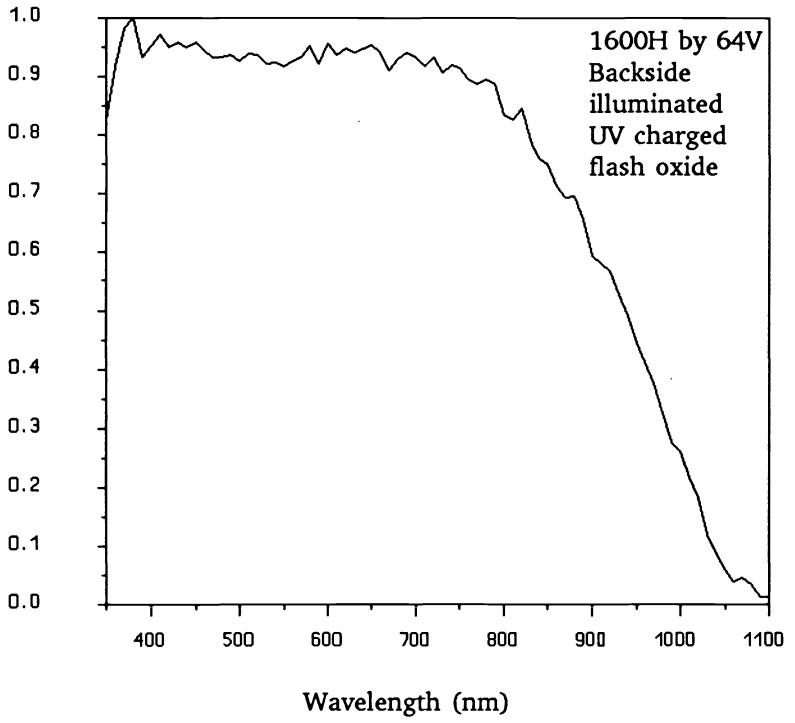

Figure 8. Relative quantum efficiency

4. DEVICE APPLICATION

The pixel size of 28um was chosen because of the desire for a large signal capacity and high dynamic range. The 28um pixel also performs well at the optical resolution and seeing conditions of the 200" telescope at Palomar Observatory. A 1600 by 1600 format array was also on the fabrication mask set, and for convenience, both devices had the same pixel size.

When imaging with a 200" telescope, the sky background is large enough to produce a shot noise greater than 30 electrons. Sub-electron noise is not required for this task. However, for spectroscopy, when the background is dispersed across M pixels, the shot noise decreases by the square root of M. Therefore it becomes useful to have an rms noise floor under one electron. Simulating the actual application, spectroscopy, was not attempted in the laboratory. However, imagine trying to detect and locate a weak signal spike in the presence of readout noise. The peak-to-peak noise, which is about five times the rms noise, needs to be minimized compared to the signal.

If we desire a minimum S/N ratio of 3 and the background illumination is zero (black), then a 1.5e rms readout noise yields a minimum signal level of 11e (9e signal for zero noise). The large, single stage FG circuit reported here cannot meet that requirement at a pixel rate of 50KHz. The averaging FG output would have to achieve 4.7e noise at 500KHz or 9.5e at 2MHz to be averageable down to 1.5e at 50KHz. Part of the difficulty is operating a single MOSFET at higher frequencies. Two stage source follower outputs have traditionally been noisier, although they can operate at much higher data rates. It was therefore decided that in order to routinely achieve 1.5e noise at 50KHz, a multi-FG output circuit was required. Noise reduction by the square root of the product of the number of FG stages and the number of averages can be realized. A two-stage output has been verified to be operational, a six-stage circuit will be tested next. It is anticipated that the six-stage averaging FG circuit will routinely achieve 1.5e rms noise at 50K pixels per second and 0.25e noise as a practical limit. At this readout noise level single electrons should be detectable.

The test results were obtained by performing the averaging in the digital domain, after the A/D converter. If the averaging is performed in the analog domain, a slower A/D converter can be utilized. Each output still needs a corresponding CDS. A gated integrator could then be operated as a summing circuit to perform the averaging. Varying the gain inversely proportional to the square root of the number of averages would produce a constant noise level into the A/D, which is desireable. Thus, as the number of averages is increased, the A/D range would slide down to a lower electron noise level and lower full scale. Finally, for a multi-FG output each summing circuit could feed a time-delay-and-integrate (TDI) circuit made up of sample-and-holds and summing amplifiers. The output of the TDI section could be digitized by a single A/D converter.

5. ACKNOWLEDGMENTS

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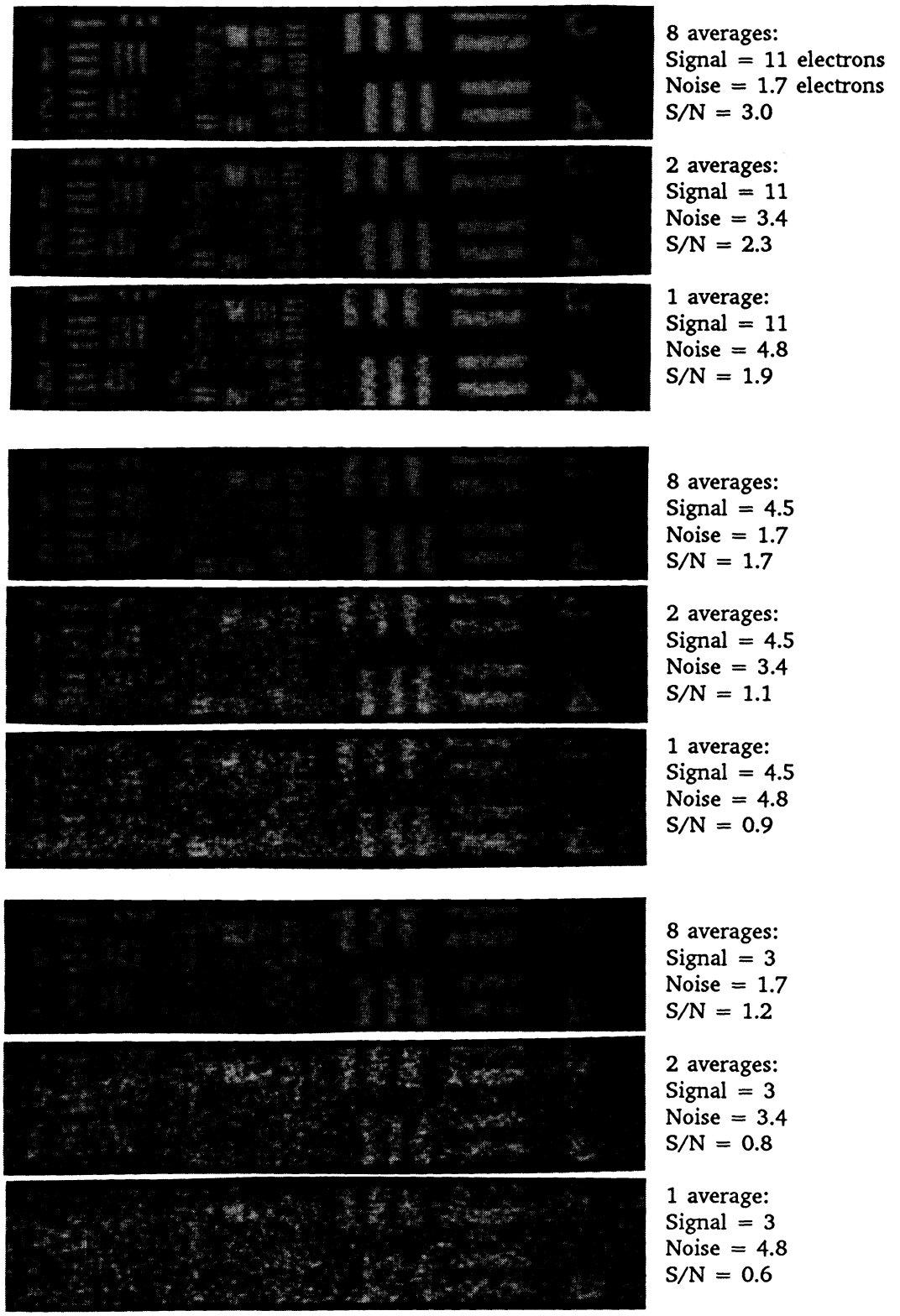

Figure 9. Images (1600 by 64 device)

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7. APPENDIX A

The clamp and sample CDS can be mathematically represented by a delta function of amplitude -1 at t=0 (clamp) and a delta function of amplitude +1 at t=Ts (sample). The Fourier transform of this is

$$1-\exp(-jw(Ts)) \ , \ w=2\pi f \tag{A1}$$

When the clamp and sample is preceded by a preamplifier with a single pole bandwidth β (radians/s), the CDS transfer function becomes[5]

$$(1-\exp(-jw(Ts))/(1+jw/\beta) \tag{A2}$$

The reset noise N_R, where K is Boltzmann's constant, T is degrees Kelvin, q is the electron charge, and C is the CCD output node capacitance, is

$$N_R = (KTC)^{1/2}/q \tag{A3}$$

To reduce the reset noise to "x" electrons requires the preamplifier to settle for time Tc during the clamp interval such that

$$x/N_R = \exp(-(Tc)\beta) \tag{A4}$$

$$\text{or} \qquad Tc = [-\ln(x/N_R)]/\beta \tag{A5}$$

Let the clamp to sample time be related to the preamplifier bandwidth by the factor k

$$Ts = k/\beta \tag{A6}$$

Let the fraction (1-y) of the clock period P be consumed by CCD clocking and output reset operations.

$$\text{then} \qquad yP = Ts+Tc \tag{A7}$$

Substitute equation A6 for Ts and equation A5 for Tc and solve for β

$$\beta = [k-\ln(x/N_R)]/(yP) \tag{A8}$$

If we ignore 1/f noise then the total noise N is approximately proportional to the square root of β, the preamplifier bandwidth. The signal S is the step response of the single pole at t=Ts, which is

$$S = 1-\exp(-k) \tag{A9}$$

Then, using equation A8, the signal to noise ratio S/N is proportional to

$$S/N \sim [1-\exp(-k)]/\{[k-\ln(x/N_R)]/(yP)\}^{1/2} \tag{A10}$$

As an example, let y=0.85, x=1 electron (the reset noise after CDS), and N_R=160e (the reset noise before CDS). The optimum value of k, from equation A10, is 2.7. PSPICE simulations show a value of k=2.0 results in 2% lower noise.

Substituting equation A8 into equation A6 gives (for k=2.0)

$$Ts = yPk/[k-\ln(x/N_R)] = 5\mu S \tag{A11}$$

and $$\beta = k/(Ts) = 4e5 \text{ radians/s or } 64KHz, \quad Tc = 20(yP)-Ts = 12\mu S \tag{A12}$$

These values of Ts and β were inserted into the CDS transfer function (equation A2) and normalized to S=1 by dividing by 1-exp(-k). The PSPICE circuit modeling program with the "analog behavioral modeling" option evaluated the result of the MOSFET noise input to the CDS response and plotted curve #2 in figure 1.

The CDS method employed in this work consisted of two matched RC integrators constructed with the capacitor connected to ground (appendix B). This integrator (RC network) has a step response of 1-exp(-at) where a=1/(RC). The derivative of the step response is the impulse response, a[exp(-at)]. The sample gate function is the impulse response over the interval t=0 to t=Tg, and is zero for t>Tg. To find the frequency response, perform the Fourier transform of the gate function:

$$F\{a[\exp(-at)]\} = a \int_0^{Tg} \exp(-at)\exp(-jwt)\,dt \tag{A13}$$

$$= a\{-\exp[-(a+jw)t]/(a+jw) \Big|_0^{Tg}\} \tag{A14}$$

$$= [1-\exp(-U-jw(Tg))]/[1+jw(Tg)/U] \quad \text{where } U=Tg/(RC) \tag{A15}$$

To account for the double sampling and subtraction, subtract the same gate function, but shifted in time by Ts (multiply the Fourier transform by exp[jw(Ts)]). Also normalize to S=1 by dividing by 1-exp(-U), the step response at t=Tg. The final formula for the frequency response is

$$\{1-\exp(-U-jw(Tg))-\exp(jw(Ts))\times[1-\exp(-U-jw(Tg))]\}/[(1+jw(Tg)/U)\times(1-\exp(-U))] \tag{A16}$$

The MOSFET noise multiplied by this CDS response is plotted by PSPICE as curve #1 in figure 1 for Tg=7μS, Ts=8μS, and U=0.5 (RC=14μS). Note that for Ts=Tg and as U approaches zero, this equation converges to the ideal reset integrator frequency response

$$[2-\exp(-jw(Tg))-\exp(jw(Tg))]/[jw(Tg)] \tag{A17}$$

PSPICE can also integrate the area under the CDS output versus frequency curve to get the total noise. Using this technique it can be shown that the dual RC integrator (for the conditions of figure 1) is 6% noisier than the ideal reset integrator (Ts=8μS). The clamp and sample CDS is 27% noisier, mainly because Ts=5μS instead of 8μS. For the clamp and sample with Ts=8μS, the noise is 5% higher, but this requires a clock period of 30μS instead of the desired 20μS.

8. APPENDIX B