A Current-Mode Position Sensitive Circuit

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Abstract

A novel technique to implement mesh-type position sensitive devices using current-mode analog VLSI is presented. By taking advantage of local analog computation this approach allows to create extremely compact circuit implementations. While in conventional approaches most sensor characteristics are adjusted by setting process parameters, our technique is fully electronically tunable and suitable to be implemented in general purpose CMOS technology. We have verified experimentally our idea designing and fabricating via MOSIS a 20 element 1D position circuit. Test results are presented demonstrating nonlinearity below 2.2% for currents in the range of 5pA to 10nA.

1. Introduction

The idea of using a resistive sheet to determine the position of a small bright spot has been used since several decades to implement position sensitive devices (PSD). The so called lateral photoeffect was first observed by Schottky in 1930 but its practical significance was pointed out only in 1957 by Wallmark [1]. PSD's give two analog outputs, one for the x-coordinate and another for the y-coordinate of a light spot projected onto the sensitive area. The main advantages of PSD over digital implementations are simultaneity of x and y measurements and simplicity in circuitry. A key feature of a PSD is the linearity of position detection. The trade-off of linearity for cost and simplicity of construction has been the focus of much research [2, 3]. Dutta [4] first introduced the concept of mesh-type PSD (MEPSD) showing the advantages of discretized resistive layers. The price paid for high response linearity is the use of ad hoc fabrication processes and off chip computation of spot position from sensor output currents.

Analog VLSI chips have been proposed to find centroid [5] and higher order moments [6] of images of bright objects. The circuits proposed so far are complex and area expensive.

Over the last few years current-mode circuits have become increasingly popular among analogue designers, enabling complex computations to be performed in the analog domain without the explicit use of differential voltage signals. A growing body of literature is now available, describing the features of the current-mode approach, as well as improved solutions to a wide area of applications [7]. In particular, current-mode subthreshold MOS [8] is remarkably suited to applications requiring low power consumption and low current detection.

In this paper we show that the current-mode subthreshold MOS methodology is well-suited for our task. In sections 2 and 3 we propose a maximally simple and compact position sensing circuit. In section 4 we discuss testing results on an implementation fabricated using standard CMOS process that demonstrate high response linearity over a range of currents spanning 3 orders of magnitude.

2. Position sensing by resistive networks

The well known idea underlying the position-sensitive device is described in Fig. 1A.

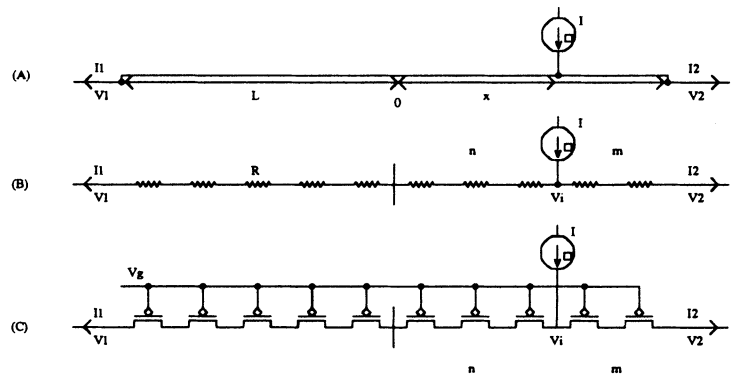

Figure 1: Resistive networks

Call $2L$ the length of the uniform 1-D resistive sheet, the point of injection of a current may be calculated from the voltages and currents at the extrema of the sheet:

$$\frac{x}{L} = \frac{I_2 - I_1}{I_2 + I_1} + 2\frac{V_2 - V_1}{I\,R} \tag{1}$$

where $I = I_1 + I_2$ is the input current, x is the coordinate of the injection point (the origin at the center so that $x \in (-L, L)$) and R is the resistance value of the sheet. If $V_1 = V_2$ the two currents flowing out of the perimeter contain enough information to extract the position by means of a simple fractional function. Unfortunately in real systems this cannot be guaranteed due to devices mismatch, therefore the voltage-dependent term is negligible only for high value of the $I\,R$ product.

Extrapolating the concept for a distribution of injected currents $I(x)$ and assuming $V_1 = V_2$ it can also be shown that:

$$\frac{\bar{x}}{L} = \frac{1}{L}\frac{\int_{-L}^{L} I(x)x\,dx}{\int_{-L}^{L} I(x)dx} = \frac{I_2 - I_1}{I_2 + I_1}$$

where $\bar{x}$ is the normalized first moment of $I(x)$.

Similarly, for a discrete 1-D uniform resistive grid (Fig. 1B) the coordinate of injection of a current is

$$\frac{x}{L} = \frac{n-m}{n+m} = \frac{I_2 - I_1}{I_2 + I_1} + 2\frac{V_2 - V_1}{I(n+m)r} \tag{2}$$

where n and m are the number of elements on the left and right side of the point x where the current is injected and r is the device resistance value. Again, the function $(I_2 - I_1)/(I_2 + I_1)$ represents a good estimate of x/L as long as the voltage-dependent term of (2) may be neglected. This requirement may be met for low values of injected current provided that r is large.

To this aim we propose the solution described in Fig. 1C where each resistor has been substituted by an MOS transistor working in the subthreshold region. This solution has the advantages of simplicity over other circuits and of small area over using passive polysilicon resistive layers.

We proceed to calculate the equivalent to (2) for this new circuit. For an p-type MOS transistor, the subthreshold current is given by $I_{ds} = I_0 e^{\kappa(V_{dd}-V_g)-V_{dd}}(e^{V_s} - e^{V_d})$ hence the currents flowing out of the two legs (Fig. 1C) are $I_2 = (I_0/m)e^{\kappa(V_{dd}-V_g)-V_{dd}}(e^{V_i} - e^{V_2})$ and $I_1 = (I_0/n)e^{\kappa(V_{dd}-V_g)-V_{dd}}(e^{V_i} - e^{V_1})$ where voltages are expressed in $\frac{kT}{q}$ units.

This leads to the following expression of the node location x:

$$\frac{x}{L} = \frac{n-m}{n+m} = \frac{I_2 - I_1}{I_2 + I_1} + 2\,I_0 e^{\kappa(V_{dd}-V_g)-V_{dd}}\frac{(e^{V_2} - e^{V_1})}{I(n+m)} \tag{3}$$

which is very similar to (2). Now notice that the voltage-dependent term of (3), which affects the trade off between offset suppression and time constant of the network, is controlled by the gate voltage V_g. So far we have shown analytically that by operating in weak inversion the relationship expressed by (3) is independent of whether one or more devices are saturated or nonsaturated even taking into account the transistor body effect. An independent study carried out by Bult and Geelen [9] has recently

demonstrated analytically this current division technique to be valid in all operating regions of an MOS transistor: strong inversion, weak inversion, linear region and saturation.

3. The computational block

The two main design issues at this point are (1) keeping the boundary voltage values at the same level while leaving the output conductance as high as possible; (2) designing a circuit to compute the $(I_2 - I_1)/(I_2 + I_1)$ ratio.

The first issue has been addressed by a two transistor current-controlled current conveyor [8] ($M0$, $M1$, $M10$, $M11$ of Fig.2) which allows currents to flow down into $M5$ and $M6$ drain without mirroring mismatches. The $(I_2 - I_1)/(I_2 + I_1)$ ratio is computed by the configuration of $M3$, $M4$, $M5$ and $M6$ illustrated in Fig.2. Using the translinear principle, which is valid because the transistors operate sub-threshold, one may see that the output current is $I_o = I_b(I_2 - I_1)/(I_2 + I_1)$ giving the required function normalized to I_b, the biasing current of the differential pair.

4. Experimental results

Two prototypes of the circuit composed of 20 nodes have been fabricated using the $2\mu m$, analog CMOS ORBIT process by means of MOSIS facilities. We have varied the transistor channel size, down to the minimum allowed by technology for a unitary aspect ratio, in order to investigate the sensitivity of the circuit with respect to device scaling. The SEM microphotograph of the smallest circuit implementation is displayed in Fig.3. The input current node is selected by an on-chip static shift register and several test points have been tied up to external pads. The first experiment was performed to verify linearity of the output current with respect to the position of the injected current. Fig.4 and Fig.5 show the steady-state position linearity characteristics of the two prototypes together with their regression line. Measurements performed on the whole chip set displayed nonlinearity in the full scale range less than 2.2% for the minimum-size device implementation with a relative RMS below 0.31%. As second experiment we have investigated the circuit performance for different values of injected current. In Fig.6 the output current is plotted versus position using different input currents displaying stable performance over three order of magnitude up to $10nA$, where the computational block transistors begin to operate in strong inversion. We also have observed a $5pA$ minimum detectable input current.

5. Conclusions

A new compact position sensitive circuit has been presented and experimentally evaluated. The feasibility of using standard MOS devices for dividing currents and for computing position has been demonstrated. The circuit has advantages over conventional applications in its simplicity of local analog computation and in its capability to be electronically tunable. Steady-state measurements have shown very good output linearity over three order of magnitude of injected current even using minimum-size device implementation.

Aknowledgements

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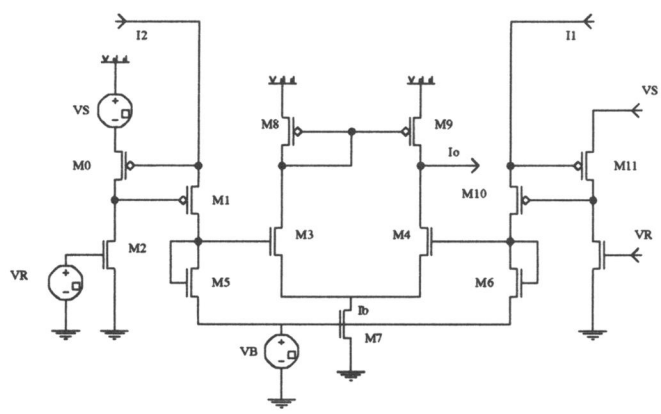

Figure 2: The $(I_2 - I_1)/(I_2 + I_1)$ function circuit

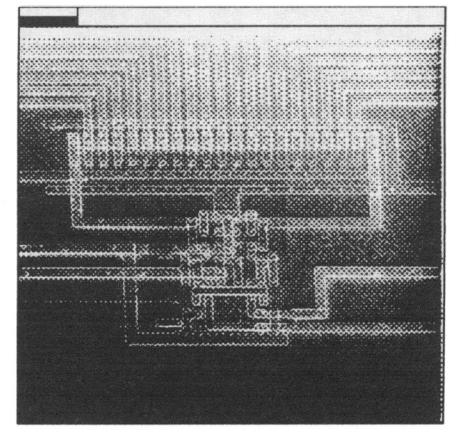

Figure 3: SEM microphotograph

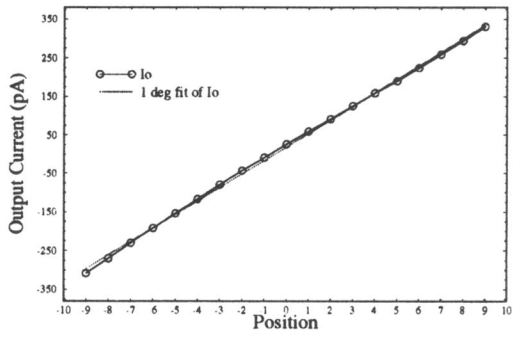

Figure 4:
Steady-state position characteristic
($50 \times 50\mu m^2$ transistor size)

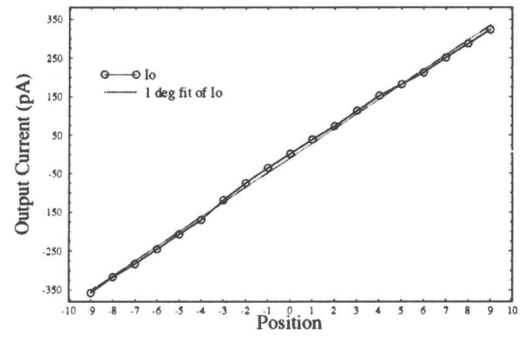

Figure 5:
Steady-state position characteristic
($4 \times 4\mu m^2$ transistor size)

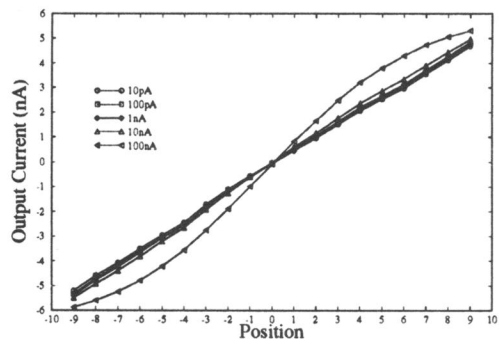

Figure 6: Input current sensitivity