A W-band GCPW MMIC Diode Tripler

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A W-band GCPW (grounded coplanar waveguide) MMIC diode tripler using GaAs PHEMT process is developed. An anti-parallel diode pair is used to produce third harmonic signal and a GCPW band pass filter is used to reject the spurious signal. The measured conversion loss is 18-20 dB from 87 to 102 GHz at 14-dBm input power. It is observed that if the filter were taken out, this tripler could be improved more than 5-dB in conversion loss without significant affecting in rejection performance. In this case, the chip could be reduced at least by half to a miniature size, that is, from 1.5 x 1 mm² to about 0.8 x 0.8 mm².

INTRODUCTION

Signal source is a key component for various system applications such as radar communication, and radio astronomy. High frequency signal source is difficult to be achieved specially in millimeter wave region. The lower frequency signal source cascade with the frequency multipliers can be used to get the high frequency signal. Another approach is using the push-push (1) or triple-push (2) configuration to achieve high frequency sources.

The frequency multipliers can be implemented in either passive or active type. The active type multipliers using transistors (7)-(10) have better conversion gain, however the bandwidth is more difficult to achieve due to the input impedance of transistors. On the other hand, passive type multipliers using diodes have wider bandwidth (3)-(6). Harmonic rejection is an important design consideration for the multipliers. It is widely reported using the quarter wavelength stub (3), (5)-(9) or balanced type (10) to reject the harmonic spurious signals. Some of the diode multipliers need dc bias to improve the performance (3)-(6). This paper presents a W-band GCPW (grounded coplanar waveguide) MMIC diode tripler without dc bias and demonstrates a measured conversion loss of 18-20 dB from 87 to 102 GHz. The conversion loss of this MMIC is comparable to the recently reported broadband tripler (4). Moreover, different from other reported W-band MMIC diode doublers and triplers (3)-(6), this MMIC is fabricated using a standard commercial available 0.15-μm high linearity InGaAs/AlGaAs/GaAs PHEMT MMIC process and therefore it can be easily integrated with other HEMT MMIC components such as amplifiers, oscillators into a single chip. Table 1 summarizes the previously reported W-band MMIC diode multipliers and this work. We estimate the size of our chip size can be reduced to 0.8 x 0.8 mm^2.

DEVICE CHARACTERISTICS AND MMIC PROCESS

The HEMT device used in this design is TRW standard 0.15-μm high linearity InGaAs/AlGaAs/GaAs PHEMT MMIC process. The HEMT device has a typical unit current gain cutoff frequency (f_T) of 70 GHz and maximum oscillation frequency (f_{max}) of 110 GHz, with a peak dc transconductance (G_m) of 580 mS/mm. The gate-drain breakdown voltage is 8 V, and the drain current at peak G_m (I_{dspk}) at 5-V drain-source voltage is 280 mA/mm. Other passive components include thin-film resistors, MIM capacitors, spiral inductors, and air-bridges. The wafer is thinned to 4-mil for the gold plating of the backside and reactive ion etching via holes are used for dc grounding.

CIRCUIT DESIGN

An anti-parallel diode pair is used in this tripler to produce third harmonic signal and suppress the even harmonic signal of the input signal (3), (4), (11). The diode is simply implemented with the gate of HEMT as the anode and the drain and source connected together as the cathode. The 4-finger 28-μm diode was used to design the tripler. The cut-off frequency is over 3 THz.

The anti-parallel diode pair can produce odd harmonic signal, so we can get not only third harmonic signal but also the fundamental signal from the anti-parallel diode pair (11). The tripler is implemented in GCPW. A GCPW band-pass-filter (BPF) is designed for spurious signal rejection. The filter consists of GCPW coupled lines and shunt short stubs (12). Via holes were added for suppressing the parallel-plate mode. The chip photo of the GCPW BPF is shown in Fig. 1.

The complete schematic of the tripler is shown in Fig. 2, and the chip photo is shown in Fig. 3. The chip size is 1.5 mm x 1 mm. The anti-parallel diode pair is shunted to ground. The 94-GHz quarter wavelength open stub is shunt to the signal line to provide short circuit for third harmonic frequency. The BPF is series after the anti-diode pair to reject the spurious signal.

The passive circuits included the BPF and the discontinuities of the transmission line were simulated by a full-wave EM simulator (Sonnet software) (13). The nonlinear simulation of the tripler was performed using harmonic balanced simulation of the AWR's circuit simulator Microwave Office (14).

CIRCUIT MEASUREMENT

The S-parameters of the GCPW BPF were measured via on-wafer probing. The measured return loss and insertion loss of the BPF are shown in Fig. 4. The return loss is better than 10 dB and the insertion loss is 5.5-8.2 dB from 87 to 97 GHz.

Fig. 5 shows the output power versus driving power for 84 GHz, 87 GHz and 105 GHz. The measured output power is -2.8 dBm while the driving power is 17.2 dBm at 87 GHz. The best conversion loss at 87 GHz is 18.1 dB while the output power is -5.1 dBm.

Fig. 6 shows the output power versus output frequency with several different driving powers. The output power is better than -5 dBm from 87 to 102 GHz while the driving power is 15.2-16 dBm. The conversion loss is better than 20 dB from 87 to 102 GHz while the driving power is 14 dBm.

It is observed that the loss of the filter is higher than expected. If the loss of the filter can be reduced, the conversion loss of this tripler will be improved at least by 3 dB as shown in our original design. Moreover, if the output is connected to a WR-10 waveguide with a properly designed waveguide transition, such as reported in (15)-(16), the fundamental and second harmonic will be rejected by the waveguide, thus the output filter may not be necessary. Also, since from the measured filter data, the return loss are better than 10 dB from 87-97 GHz, it is very likely the output matching will not affected much by taking out the filter. In this case, the chip size could be easily reduced by at least half in x-dimension. Further meandering the input open stub could also reduce the y-dimension by 20%. We estimate the chip size can be about 0.8 mm x 0.8 mm without degrading the performance significantly.

SUMMARY

A W-band GCPW MMIC frequency tripler has been designed, fabricated and tested. The tripler uses an anti-parallel diode pair configuration and was fabricated by TRW standard 0.15-μm InGaAs/AlGaAs/GaAs PHEMT MMIC process. Since the tripler was fabricated by standard PHEMT MMIC process, it can easily be integrated with other MMIC circuits such as oscillators and amplifiers. The conversion loss of this tripler is 18-20 dB from 87 to 102 GHz while the input power is 14 dBm. It also has potential to redesign to a miniature size of about 0.8 mm x 0.8 mm with a similar performance.

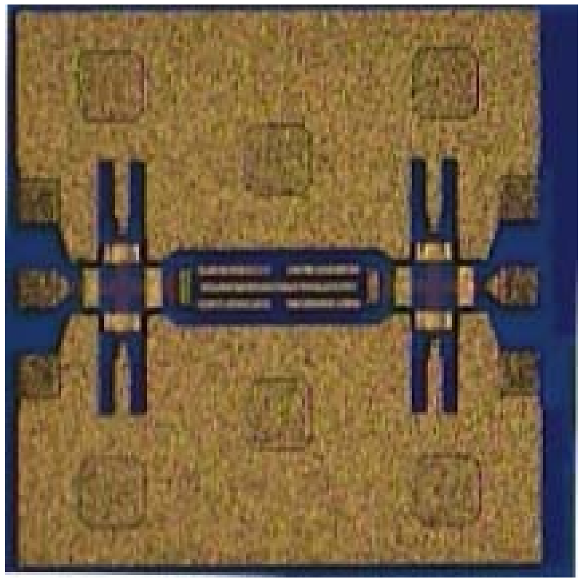

Fig. 1. The photo of the GCPW band pass filter.

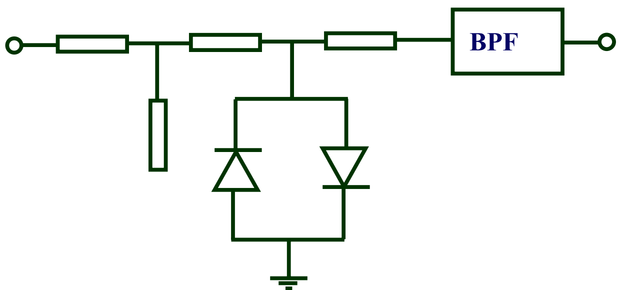

Fig .2. The schematic of the W-band GCPW tripler.

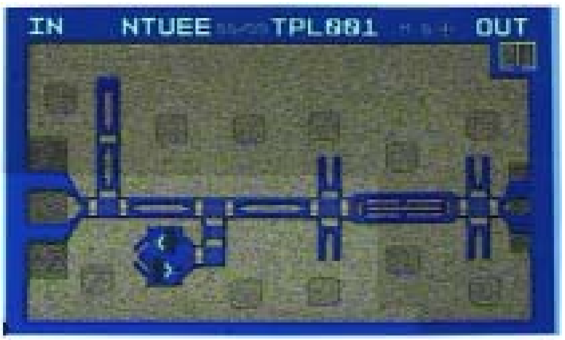

Fig. 3. The chip photo of the W-band GCPW tripler with a chip size of 1.5 mm x 1 mm.

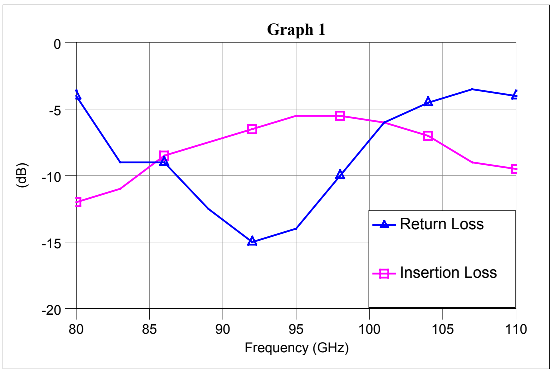

Fig. 4. The measured results of the GCPW BPF.

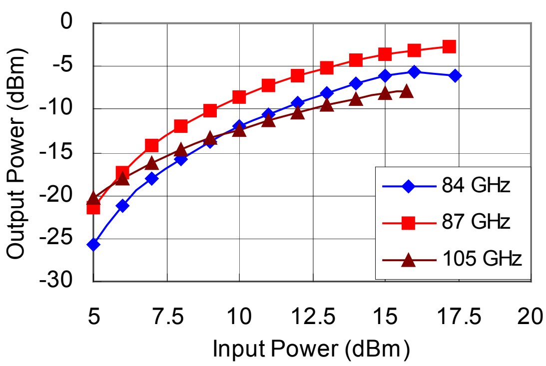

Fig. 5. Output power versus driving power.

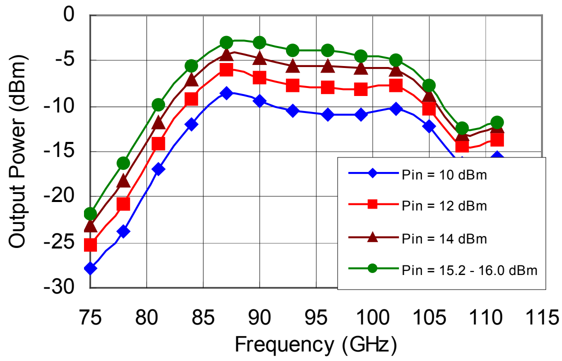

Fig. 6. Output power versus output frequency for several different driving powers.

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Table 1
The summary of previously reported W-band MMIC diode multipliers and this work.

Paper	(3)	(4)	(5)	(6)	This work
Frequency multiples	x3	x3	x2	x2	x3
Device	Schottky vertical diode	BES Schottky diode	GaAs varactor Schottky diode	Varactor diode (doping tuning for efficiency)	GaAs diode PHEMT MMIC process
Transmission line	Microstrip line	Microstrip line and GCPW	Finite ground CPW	Microstrip line	GCPW
Output frequency range (GHz)	97	75 – 110	70 – 80	94	87 – 102
DC bias	Yes	Yes	Yes	Yes	No
Output power	19 dBm at 97 GHz	> -4 dBm	20.6 dBm at 74 GHz	18.1 dBm at 94 GHz	> -5 dBm
Conversion loss over the band	-	< 20 dB	< 12 dB	-	< 20 dB
Best conversion loss	12 dB at 97 GHz	16.2 dB at 85 GHz	9.9 dB at 74 GHz	6 dB at 94 GHz	18.1 dB at 87 GHz
Chip size (mm^2)	-	2 x 0.74	-	-	1.5 x 1*

* potential to reduce to 0.8 mm x 0.8 mm