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Communication

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Enabling Simultaneous Extreme Ultra Low-*k* in Stiff, Resilient, and Thermally Stable Nano-Architected Materials

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Keywords: dielectric constant, low-k, nanolattice, porosity, Young's modulus.

Abstract

Low dielectric constant (low-*k*) materials have gained increasing popularity because of their critical role in developing faster, smaller, and higher performance devices. Their practical

use has been limited by the strong coupling between mechanical, thermal, and electrical properties of materials and their dielectric constant; low-*k* is usually attained by materials that are very porous, which results in high compliance, i.e. silica aerogels,[39] high dielectric loss, i.e. porous polycrystalline alumina,[25] and poor thermal stability, i.e. Sr-based metal-organic frameworks.[23] We report the fabrication of 3D nano-architected hollow-beam alumina dielectrics whose *k* is 1.06-1.10 at 1MHz that is stable over the voltage range of -20V to 20V and a frequency range of 100 kHz to 10 MHz. This dielectric material can be used in capacitors and is mechanically resilient, with a Young's modulus of 30 MPa, a yield strength of 1.07 MPa, a nearly full shape recoverability to its original size after >50% compressions, and outstanding thermal stability with a thermal coefficient of dielectric constant (TCK) of 2.43×10^{-5} K^{-1} up to 800 °C. These results suggest that nano-architected materials may serve as viable candidates for ultra low-*k* materials that are simultaneously mechanically-resilient, and thermally and electrically stable for microelectronics and devices.

Main Text

Designing and synthesizing low dielectric constant (low-*k*) materials has been a subject of intense research because of their potential use in high performance technological applications like computer processing,[1,2] wireless communications,[3-6] and automotive radar.[7] Lowering the *k* of the interlayer dielectric decreases the resistance-capacitance (RC) delay, lowers power consumption, and reduces cross-talk between nearby interconnects, all of which pose significant issues for modern integrated circuits (ICs).[8-10] The low-*k* property is also favored in low temperature co-fired ceramic (LTCC) technology and represents the backbone of Multi Chip Module (MCM) technology, which enables the integration of passive elements like inductors,

resistors, and capacitors, which serve as building blocks for 3D circuits for the microwave/millimeter communications industry.[11-12] For example, the antenna in a typical RF module for radiating/receiving radio waves, requires the supporting substrate whose *k* is sufficiently low to prevent surface wave propagation and to increase the bandwidth.[13]

Introducing controlled porosity into otherwise monolithic materials has been envisioned as a promising route for developing ultra low-*k* interconnect materials.[14-20] The selection of potential candidates for that is challenging because lowering the *k* of these materials through increasing porosity is often accompanied by the degradation of mechanical integrity, i.e. a 77% reduction in Young's modulus after a 46% decrease in the density of bridged organosilicates[21] and a four order of magnitude reduction in the mechanical strength of silica aerogels measured via three-point flexural test when spanning 0%-95% porosity.[22] Other properties also have been shown to degrade with introducing porosity; for example, the dielectric constant of a Sr-based metal-organic framework was reported to increase by 18% over the temperature range of 0°C-350°C,[23] the breakdown voltage field of porous SiCOH deposited using plasma enhanced chemical vapor deposition (PECVD) was reported to decrease from 5.5 MV/cm at 30% porosity to 3.6 MV/cm at 45% porosity,[24] and the dielectric loss, tan δ, of polycrystalline alumina was reported to increase over two orders of magnitude when the porosity increased from 2% to 40%.[25] The deterioration of these properties can be attributed to large variations in aggregated particle and pore sizes, disordered pore distributions, and interconnected pores.[26] The low *k* of 1.25-1.36 have been attained in aerosols at high frequencies of 0.050-1.3 GHz, and as low as 1.08 in the higher 11-12 GHz range.[27,28] To date, no material with a *k* below 1.42 (at 1 MHz), whose mechanical properties were also investigated has been reported.[19]

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Figure 1 shows the fabrication process of capacitors that contain nano-architected dielectrics. First, a nanolattice with a horizontal top plate and overall dimensions of 128 μm × 128 μm planar top area and 8 μm height, a unit cell size of 4 μm, 300 nm major axis beam diameter, and 250 nm minor axis beam diameter, was fabricated out of an acrylic polymer resin using two-photon photolithography (TPL) direct laser writing (DLW). This scaffold was written directly on a Au/Ti bi-layer (80/12 nm) that had been previously evaporated on a Si wafer (1 mm × 1 mm), which serves as the bottom electrode (Figure 1(a-b)). This polymer nanolattice was then coated with a 10 nm-thick conformal layer of alumina (Al_2O_3) using atomic layer deposition (ALD) (Figure 1c). Two opposing outer edges of the nanolattice were then removed by focused ion beam (FIB) milling, which uncapped the alumina coating on the outermost beams and exposed the interior polymer scaffold to be etched away in oxygen plasma (Figure 1d). An identical bi-layer, Au/Ti (80/12 nm), was then evaporated as a top electrode on the top plate of the nanolattice to create a parallel plate capacitor (Figure 1(e-h)). Figure 1f shows a dark field Transmission Electron Microscopy (TEM) image and a SAD pattern of an individual alumina tube that demonstrate that the film is an amorphous matrix that contains ~ 5 – 15 nm nanograins.

To investigate the dielectric properties of the nanolattice, we measured the capacitance of nanolattices with unit cell sizes of 4 μm and 8 μm and total heights of 4 μm and 8 μm (see schematics and images in Figure S1). Capacitance was measured using a Keithley 4200-SCS impedance analyzer with the ability to control the temperature and probe the top surface of the nanolattice without applying forces (see the details in the Methods Section). **Figure 2(a-c)** shows capacitance density vs. frequency plots of the fabricated samples, which convey that each nanolattice had a nearly constant capacitance density over the frequency range of 100 KHz to 10 MHz at an applied bias of 20 V. The data show that the 4 μm-single unit cell-high, 384 × 384

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μm^2 –top area sample had the highest capacitance density of 2.4 ± 0.25 pF at; both the 4 μm-double-unit-cell-high and the 8 μm-single-unit cell-high samples with top areas of 128 × 128 μm^2 had the capacitances of 1.17 ± 0.17 pF and 1.18 ± 0.14 pF, respectively. **Figure 2(d-f)** shows capacitance densities as a function of bias swept from - 20 V to + 20 V at frequencies of 100 KHz, 1 MHz and 10 MHz. These plots show that the capacitance densities were stable, with the dielectric losses of 0.034 ± 0.004 at 100 kHz, 0.026 ± 0.004 at 1 MHz, and 0.033 ± 0.005 at 10 MHz (See Figure S2 and Table S1 for more details). The C-V plots shown in Figures 2(d-f) were normalized by the relative capacitance as a function of applied voltage at varied frequencies to extract the voltage coefficients of capacitance (VCCs),[29] $\left(C - C_o\right)/C_o$, where C_o is the capacitance density at zero bias (Figure S3). These measurements revealed that VCCs were virtually non-existent for all samples, which implies that the nanolattices are stable over this voltage range. Measurements of nanolattice capacitance over 3 experiments produced approximately identical data, as conveyed in the plots in Figures 2(d-f) and S2.

We calculated the dielectric constant, k, for a parallel plate capacitor using the measured capacitance densities:[30]

$$k = Cd/\varepsilon_o A \qquad (1)$$

where ε_o is the dielectric permittivity in a vacuum (8.85×10^{-12} F/m), A is the footprint area of the electrode, d is the thickness of the dielectric layer, and C is the capacitance. To obtain the dielectric constant, the capacitance density (C/A) was inserted into Equation 1 with the proper thickness of the structure based on SEM images. To calculate the expected dielectric constant of the capacitor, we first calculated the relative density, $\bar{\rho}$, of the hollow nanolattices following the approach of Meza, et al, described fully in Methods section.[31] Using the rule of mixtures, the

relative density of the nanolattices and the dielectric constant can be related through an analytical expression:

$$k = f_a k_a + f_m k_m = f_m (k_m - 1) + 1 = \overline{\rho}(k_m - 1) + 1 \quad (2)$$

where f_a is the relative fraction of air in the structure, f_m is the fraction of solid material (i.e. the volume of the shell on the hollow structure), which is equivalent to $\overline{\rho}$, k_a is the dielectric constant of air of ~1, and k_m is the dielectric constant of the constitutive solid. The solid that comprises nanolattices in this work is ALD-deposited Al_2O_3 whose dielectric constant has been reported by Tapily, et al to be 8.[32] **Table 1** summarizes the dielectric properties - measured and calculated using Eq. 2 - of nanolattices with different unit cell sizes and relative densities. It demonstrates that the lowest k of 1.06 was attained by the nanolattice with an 8 μm unit cell; the rest of the samples had indistinguishable dielectric constants of 1.10. We found that the measured and the calculated k's match well, and the marginal underestimation of the calculated k in capacitors with a 4 μm unit cell size is likely caused by the small dimensional deviations in the periodic structure, which alters its relative density. These results suggest that the k of this material can be finely tailored by altering the relative density, following the relation in Equation 2.

The mechanical behavior of TPL-produced nanolattices has been extensively investigated and revealed their exceptional mechanical resilience,[31,33] insensitivity to flaws,[34] suppression of brittle failure,[35,36] high tensile elasticity,[37] and high strength-to-density ratio.[38] In cellular solids, the relative density uniquely defines the mechanical properties, i.e. stiffness and strength, through a scaling relationship.[31] For example, the power law scaling of Young's modulus as a function of relative density is:

$$E \propto \overline{\rho}^{n} \quad (3)$$

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where n is empirically determined. The specific scaling of stiffness with relative density for hollow alumina nanolattices has been reported to have an exponent, n of 1.61.[31] **Figure 3a** shows a representative stress vs. strain plot of an octet geometry Al_2O_3 hollow-beam nanolattice with a relative density of 1.3%, a unit cell size of 5 μm, major axis beam diameter of 1.48 μm, minor axis beam diameter of 0.37 μm, and alumina shell thickness of 10 nm during a uniaxial compression experiment.[31] To obtain accurate deformation characteristics, stiffness, and strength, the overall dimensions of samples for the compression experiments were 20 μm × 20 μm × 25 μm, which are a factor of ~3 and ~6 taller than those made for the capacitors. Load data from the nanoindenter was converted into stress by dividing it by the contact area of the sample, and displacement was converted to strain through normalizing by the sample height. The slope of the unloading portion of cyclic stress-strain data was averaged to calculate the structural stiffness, or Young's modulus, E, of the nanolattice, and the first peak in the data that corresponds to the initial layer buckling event, demarcates the yield strength, σ_Y. The data in Figure 3a reveals E of 30 MPa and σ_Y of 1.07 MPa, as well as ~98% shape recovery when strained to >50%. This stiffness of 30MPa at a relative density of 1.3% in the alumina nanolattices is roughly two orders of magnitude greater than that of similarly-dense ultralight foams; for example silica aerogels, whose modulus has been reported to be 100 kPa at approximately 1% relative density.[39] The structural order provided by the octet architecture of the nanolattices in this work enables an improved utilization of the constituent material to create samples that are two orders of magnitude stiffer than stochastic foams at similar relative densities.[40] The ability of this brittle material to recover after compression is enabled by shell buckling in the beams, a recoverable instability, which is determined by the wall thickness-to beam diameter ratio, t/a.[31] These results point to the mechanical resilience of the nanolattices

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even at relative densities of ≤ 1%, a regime where other porous materials permanently deform. Since the dielectric constant of architected materials appears to be governed by the intrinsic dielectric constant of the solid material that comprises it and the relative density, one can expect little change to k after recovery. Investigation of the changes in dielectric constant during compression is currently underway.

Figure 3b shows a plot of Young's modulus vs. dielectric constant for several existing low-k dielectrics, with hollow alumina nanolattices in this work marked as a filled diamond symbol. The relationship between Young's modulus and relative density shown in Equation 3 and one between the dielectric constant and relative density (Equation 2) allow us to postulate an analytical relationship between the dielectric constant of hollow alumina nanolattices and their stiffness:

$$E \propto \left(\frac{k-1}{k_m - 1} \right)^n \quad (4)$$

The dashed contour in Figure 3b presents the solution of Equation 4 using the appropriate parameters for the hollow alumina nanolattices. This boundary represents the available parameter space where it is possible to fabricate hollow alumina nano-architectures whose combined dielectric constant and Young's modulus outperform all other existing materials that have been reported to date in the low-k ($k < 3.9$) and ultra low-k ($k < 2.5$) regimes in the 100 kHz -10 MHz frequency range.

To further illustrate the unique position of nano-architected materials, **Figure 3c** compares the hollow alumina nanolattices to several other material systems whose porosity can be varied through processing: hyperbranched poly(amidoamine) conjugated silica (HBPCS) (RD 30-90%),[41] silica xerogel (RD 45-64%),[42] silica aerogel (RD 32-40%),[43] and polyimide aerogel with varying amounts of 2,2-bis(3,4-dicarboxyphenyl)hexafluoropropane dianhydride (6FDA) in

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the backbone of the polyimide (0% 6FDA RD 11-16%, 50% 6FDA RD 5.3-8.1%).[28] The dashed contour represents the same scaling as one shown in Figure 3b for nanolattices with relative densities between 1% and 10%. The data points and trend lines for other reported material systems represent their corresponding scaling of stiffness with dielectric constant (see SI for additional information) for the range of relative densities that have been attained using their respective fabrication techniques. The two sets of polyimide data have different formulated numbers of repeat units in the oligomers, as well as the total polymer concentration in the precursor solution, which prevents accurate formulation of the scaling. This polyimide data was taken at 11-12 GHz, well above the 1 MHz frequencies used in other studies. It has been observed that most materials exhibit lower dielectric constants at higher frequencies, as the orientation polarization typically vanishes around 1 GHz with increasing frequency.[10, 44] The relative densities of each shown material system are also depicted in the plot. This landscape conveys that (1) the dielectric constant of 1.06 for the hollow alumina nanolattices is extremely low for this frequency regime and (2) the Young's moduli of these nanolattices is at least an order of magnitude greater than what has been observed in insulating materials at such low porosity.

To investigate the dependence of the dielectric constant on temperature, we first measured the capacitance densities of an 8 μm unit cell nanolattice at a constant frequency of 1 MHz while spanning the applied voltage from -10V to 10 V. The measurements were carried out in an isothermal condition with the temperature varying from 25°C to 800ºC. **Figure 4a** shows the capacitance density vs. voltage at several representative temperatures during this experiment. The data indicate that capacitance densities were virtually constant, 0.925 ± 0.025 (pF/mm^2), and the extracted VCCs from all the measured capacitances across all temperatures were

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approximately zero (Figure S4). We also measured the variation of capacitance density as a function of frequency at different temperatures (25°C - 800ºC) as shown in **Figure 4b**, which demonstrates that the effect of temperature on capacitance density is negligible. We observed small dielectric losses within the range of 0.01 - 0.1 over the entire range of tested frequencies, temperature, and voltage (See Figure S5 for details).

The dielectric constant of nanolattices was calculated to be 1.06 ± 0.05 using the measured capacitances at the applied temperatures and frequencies, as depicted in **Figure 4c**. The temperature dependence of the relative dielectric constant is usually quantified by the temperature coefficients (TCKs) defined as:[45,46]

$$TCK = \frac{\Delta k}{k_{RT} \Delta T} \tag{5}$$

where Δk is the change in relative dielectric constant with respect to the reference dielectric constant at room temperature, k_{RT}, and ΔT is the change in temperature relative to the reference temperature. The TCK of the nanolattice was calculated to be 2.43×10^{-5} K^{-1}. The dielectric constant of a polycrystalline alumina film is strongly temperature dependent: k increases by a factor of ~1.3 when temperature increases from 300 to 400 K.[47] Thermal conductivity of materials generally decreases with introducing porosity; for instance, the thermal conductivity of bulk alumina is ~0.17 W/cmK, and that of ~75%-porous alumina is ~12 times lower, at 0.014 W/cmK.[48] The observed high temperature stability exhibited by the alumina nanolattices in this work likely stems from the low thermal conductivity of these percolating ultra-low-density nano-architectures. This stability can have significant beneficial impact for microprocessors and devices whose circuits undergo thermal fluctuations caused by the heat that is released during their operation or from the environment. It is also a stark contrast to ultra low-k organic

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polymers ($k \leq 2$), which suffer from severe restrictions in thermal processing because they decompose at low temperatures.[49-52]

We demonstrate a fabrication process to create parallel plate capacitors with three-dimensional hollow alumina nanolattices as the dielectric layer. These 3D nano-architected materials were created using two-photon lithography (TPL) and atomic layer deposition (ALD), had an octet unit cell size of 4 μm or 8 μm, 300 nm major axis beam diameter, and 250 nm minor axis beam diameter, and an alumina shell thickness of 10 nm. Direct-probing electrical measurements of the capacitors revealed the dielectric constant of the nanolattices, k, to be 1.06 at a frequency of 1 MHz; uniaxial compression experiments revealed their Young's modulus to be 30 MPa, a value 300 times higher than that of other equivalently-porous dielectrics.[39] This combination of extremely low-k and high stiffness places these 3D nano-architected materials into previously unattainable white space, outperforming all other materials that have been reported to date in the low-k and ultra low-k regimes in the 100 kHz -10 MHz frequency range. We found the dielectric constant to be stable over -20V to +20V range, 100 kHz-10 MHz frequencies, and 25°C-800°C temperatures. These structural meta-materials also offer mechanical resilience as revealed by their shape recoverability after being compressed by 50% strain. These hollow alumina nanolattices are also very temperature insensitive and chemically stable, which provides them many processing advantages over other materials currently being investigated. We believe that the nanolattice capacitors described in this work provides a new efficient pathway to resolve the long-standing problem of mechanical integrity, thermal stability, and electrical reliability of ultra low-k applications.

Methods

Sample Fabrication: Low-density octet geometry nanolattices with unit cell sizes of 4 and 8 μm and a monolithic top plate were designed in CAD software. Utilizing this code, IP-DIP 780 polymer nanolattice scaffolds were created using two-photon photolithography (TPL) direct laser writing (DLW) in the Photonic Professional TPL-DLW System (Nanoscribe GmbH) on Si wafers coated with titanium (12 nm) and gold (80 nm). These polymer nanolattices were then coated with a 10 nm-thick atomic layer deposition (ALD) alumina film in a Cambridge Nanotech S200 ALD System using H_2O and trimethylaluminum (TMA) precursors. The interior polymer nanolattice scaffold was then removed by using a focused ion beam (FIB) system (FEI Versa 3D) to remove portions of the outer alumina coating and placing the sample in a Diener Zepto oxygen plasma system for several hours. The top electrode was formed by depositing titanium (12 nm) followed by gold (80 nm) on top of the structure. This results in a vertical capacitor with an interior dielectric material composed of a hollow 3D ceramic nanolattice. The maximum 2D size for each nanolattice was typically 128 μm × 128 μm; larger structures were fabricated by stitching multiple nanolattices together.

Density Calculations: Nanolattice beams were imaged in an SEM (FEI Versa 3D) from the top and side for accurate measurements of the elliptical beams. These dimensions were used to create a representative CAD model of the polymer nanolattice. A similar CAD model was created for the composite alumina-coated polymer nanolattice. The total volume of the hollow alumina nanolattice was calculated by subtracting the volume of these two nanolattices. The total volume of the hollow top plate was calculated by summing the top flat plate of alumina with a plate of the same size with appropriately-sized holes removed for where the nanolattice meets the top plate. These two volumes were then summed and divided by the total structure envelope to calculate the relative density of the 3D architecture.

Mechanical measurements: Characterization structures were compressed quasistatically using a flat punch tip in a G200 XP Nanoindenter (Agilent Technologies) to 50% strain. Yield stress was determined by the peak stress before failure. Young's moduli were calculated from the slope of the unloading portion of cyclic experiments.

Electrical Measurements: The measurement for dielectric properties of 3D-ceramic nanolattice was carried out with a semiconductor characterization system (Keithley 4200-SCS connected to a 4210-CVU multi-frequency capacitance-voltage unit) over a frequency range of 100 kHz to 10 MHz. For temperature dependent impedance measurements, the 3D-ceramic nanolattice was placed on a ceramic heater (Linkam LTS420) controlled by a Watlow SD series temperature controller (± 0.1 °C) connected to this same characterization system. The temperature of the sample was varied from 25 to 800 ºC with a heating rate of 10 ºC/min and the measurements were taken at approximately 50 ºC intervals on heating as well as on cooling. In order to study their thermal stability, the sample was maintained for 15 minutes at each temperature before measurement. In order to avoid applying stress to the nanolattice from contact and from thermal expansion of the material during the impedance measurements, we used flexible thin tungsten hair pins (diameter = 0.4 μm) and a specially designed stage which controls its height with a step of 100 nm, allowing us to monitor the measurement using a high resolution optical microscope (OM). The resolution of the OM is 300 nm.

Supporting Information

A thorough description of the dielectric constant and loss, VCCs, and density calculations, as well as additional figures, are provided in support of the results presented above. The Supporting Information is available free of charge on the ACS Publications website.

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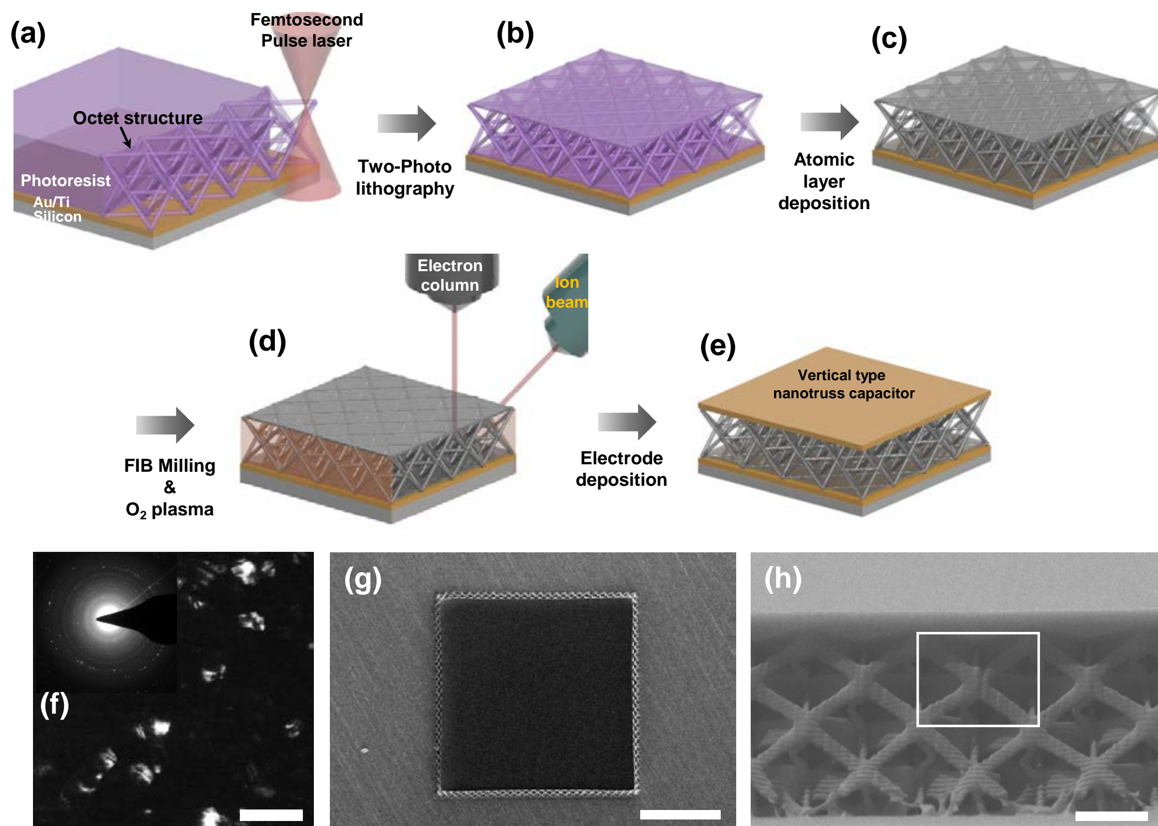

Figure 1. Schematics describing the manufacturing process of the nanolattice capacitor. (a and b) Fabrication of a polymer scaffold via two-photon photolithography (TPL) direct laser writing (DLW). (c) Alumina coating on the polymer nanolattice using ALD. (d) Removal of the polymer scaffold using FIB and oxygen plasma etching. (e) Deposition of the top electrode layer. (f) TEM dark field image and SAD pattern of a single alumina tube. The scale bar is 50 nm. (g and h) Top and side view SEM images of the nanolattice capacitor (4 μm unit cell, 8 μm sample height, and 128 μm × 128 μm planar top), respectively. The boxed area indicates a unit cell. The scale bars of (g) and (h) are 50 μm and 3 μm, respectively.

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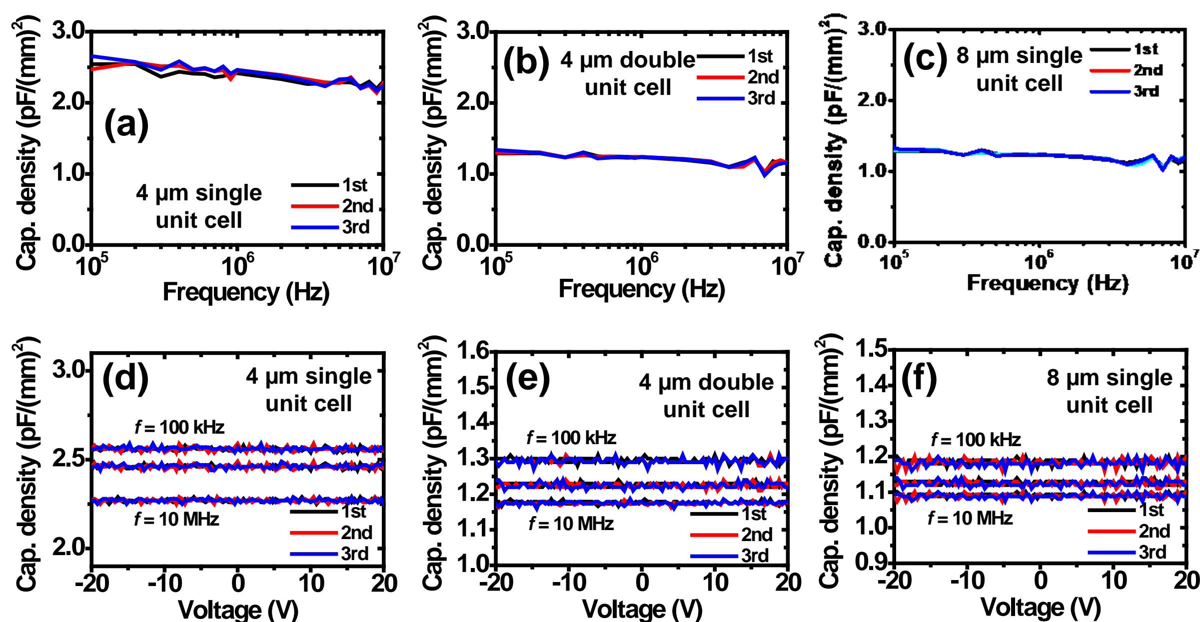

Figure 2. Dielectric properties of nanolattice capacitors. (a-c) Frequency dependence on capacitance density of the three capacitors. (d-f) Voltage dependence on capacitance density of the three capacitors.

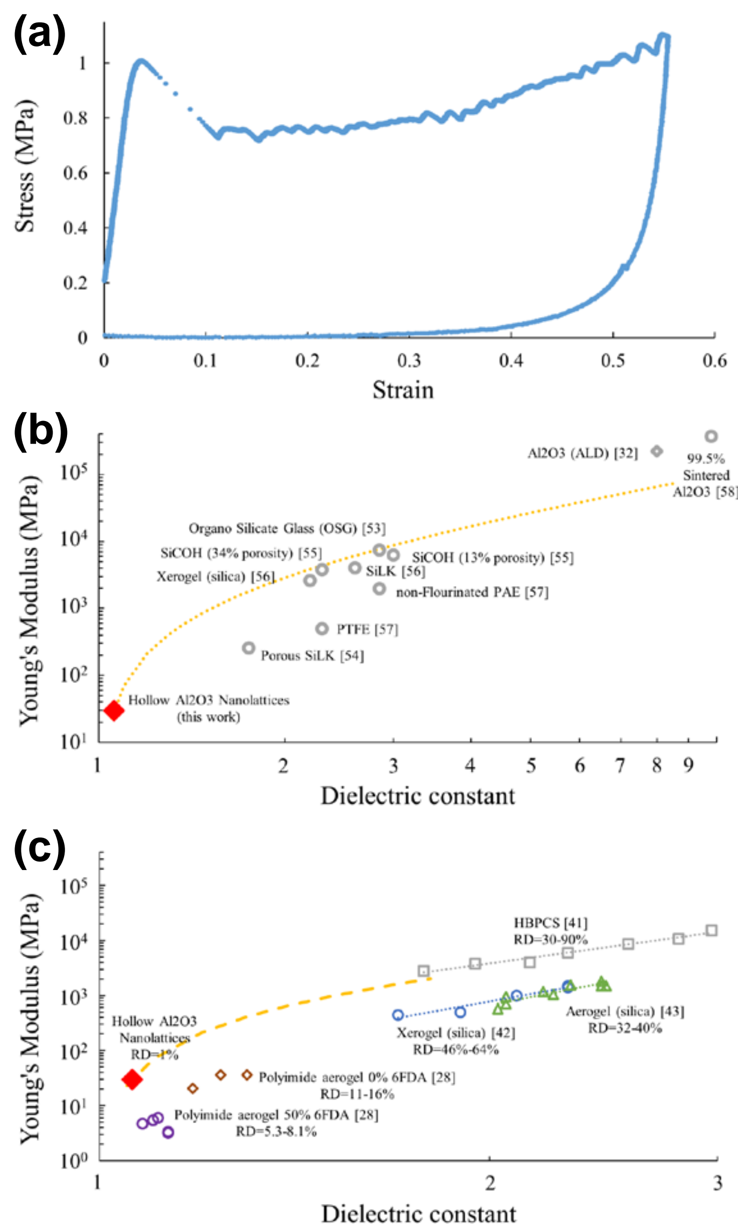

Figure 3. Mechanical properties of a representative nanolattice and correlation with its dielectric constant compared to other low-*k* materials. (a) Representative strain vs. stress plot of a hollow alumina nanolattice. (b and c) Young's modulus vs. dielectric constant plots of the nanolattice compared with other low-*k* materials.

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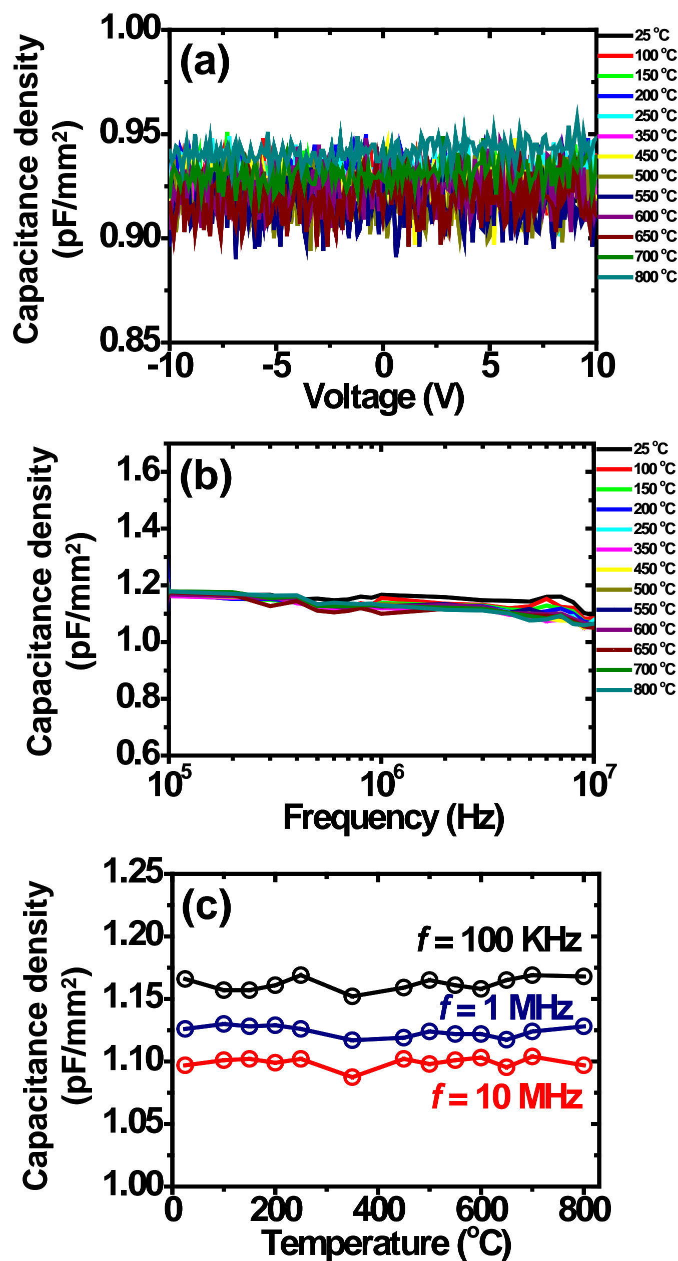

Figure 4. Temperature stability of the nanolattice capacitor with 8 μm single unit cell layer. (a) capacitance density vs. voltage plots at varied temperatures (25 ~ 800 °C). (b) capacitance density vs. frequency plots at varied temperatures. (c) capacitance density vs. temperature plots at 100 KHz, 1 MHz, and 10 MHz.

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Material	Unit cell size (μm)	Area (μm^2)	Thickness (μm)	Measured dielectric constant (1MHz, -20 V~ +20 V)	Calculated dielectric constant	Dielectric loss (1MHz, -20 V~ +20 V)
Al_2O_3 / air = 0.93 / 99.07%	4	128 x 128	4	1.10	1.07	0.034 (± 0.004)
Al_2O_3 / air = 1.0 / 99.0%	4	128 x 128	8	1.10	1.07	0.026 (± 0.004)
Al_2O_3/air = 0.89 / 99.11%	8	128 x 128	8	1.06	1.06	0.036 (± 0.004)
Al_2O_3/air = 0.93 / 99.07%	4	384 x 384	4	1.10	1.07	0.026 (± 0.003)

Table 1. Summary of the alumina/air ratios (relative density) of the nanolattices with diverse dimensions and unit cell geometries, and comparison of the measured dielectric constants with their calculated ones estimated from the density.

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