Optics Letters

Vertically integrated spot-size converter in AlGaAs-GaAs

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Received 11 August 2017; accepted 14 September 2017; posted 18 September 2017 (Doc. ID 304327); published 11 October 2017

We report on the demonstration of a spot size converter (SSC) for monolithic photonic integration at a wavelength of 850 nm on a GaAs substrate. We designed and fabricated a dual-waveguide AlGaAs chip. The design consists of a lower waveguide layer for efficient end-fire coupling to a single-mode fiber, an upper waveguide layer for high refractive index contrast waveguides, and a vertical SSC to connect the two waveguide layers. We measured a SSC conversion efficiency of 91% (or −0.4 dB) between the upper and lower waveguide layers for the TE mode at a wavelength of 850 nm.

OCIS codes: (130.3120) Integrated optics devices; (250.5300) Photonic integrated circuits; (220.4241) Nanostructure fabrication.

https://doi.org/10.1364/OL.42.004167

The development of photonic integrated circuits (PICs) has been advancing rapidly over the last two decades. Aluminum gallium arsenide (AlGaAs) semiconductors are widely used for discrete optoelectronic devices such as light-emitting diodes, lasers and detectors, and electronic devices such as high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs). Many of the basic material properties of AlGaAs are advantageous to designing PICs. All compositions of AlGaAs are lattice matched. The band gap energy can be varied from 1.42 eV (GaAs) to 2.17 eV (AlAs) and, similarly, the index of refraction at 850 nm can be varied from 3.68 (GaAs) to 2.99 (AlAs). These provide for a flexible epitaxy growth and offer more design flexibility. The 785–850 nm spectral window has several potential applications. For noninvasive biosensing, it is the wavelength range where hemoglobin has the lowest absorption coefficient [1]. As current data center communications systems use 850 nm vertical cavity lasers, monolithic integration would enable efficient wavelength division multiplexing devices [2]. AlGaAs has also been identified as the promising semiconductor system for quantum optics [3–6]. The integration of pump lasers, nonlinear optical elements, and signal processing waveguides opens the possibility of a true quantum optics technology.

Currently, PICs are based on many different integration schemes, including etch-and-regrowth [7,8], quantum-well intermixing (QWI) [9,10], and hybrid material integration [11]. These methods have several drawbacks that either limit the integration complexity or incur high fabrication costs. One alternative is regrowth-free vertical integration, in which functional waveguides composed of different yet compatible III-V semiconductor materials are vertically stacked in one epitaxial growth run and coupled to each other by means of lateral tapers defined in a process of fabrication. This integration scheme, known by the names of single-mode vertical integration [12], asymmetric twin-waveguide (ATG) technology [13], multiguide vertical-integration (MGVI) [14], or taper-assistant vertical integration (TAVI) [15], has been proven a versatile PIC platform in indium phosphide (InP). Two-guide [16,17], three-guide [18], and even four-guide [19] vertical integration PICs have been successfully developed and commercialized in InP. The major advantage of the vertical integration is the ability for independent optimization of the functional waveguides without additional growth steps or any other alteration of as-grown material; this is not limited to InP and can be extended to GaAs-based PICs [2]. To do this, however, a fundamental problem of the TAVI of the different functional waveguides formed in the common AlGaAs-GaAs vertical stack should be solved first.

In this Letter, we report on the first, to our knowledge, TAVI of two AlGaAs–GaAs based waveguides operating in 850 nm, the most important wavelength window covered by this material system. We demonstrate a SSC, which allows for a low loss and high displacement tolerance coupling of the optical fiber with large-size and round-shape of the optical mode to the semiconductor waveguide featuring a small-size and flattened-shape optical mode. Vertically integrated SSC in InP PICs [20,21] is known to be a robust solution to high-efficiency fiber to PIC coupling, which is commonly used in the vertically integrated PICs in InP [22], and so could be its AlGaAs–GaAs counterpart.

To demonstrate the TAVI SSC in AlGaAs–GaAs, we designed and fabricated a dual waveguide chip. The design consists of a lower waveguide layer for an efficient and displacement-tolerant coupling to a single-mode fiber (SMF), and an upper waveguide layer for on-chip routing, interconnecting, and other passive functions. The former is a relatively weakly vertically confined waveguide with the mode size suitable for a PIC to fiber coupling. The latter is a strongly vertically confined waveguide intended for a passive guiding in a limited footprint area of the PIC. Because of the significant, and intentional, mode mismatch between the two waveguides, the lateral tapering system is designed to adiabatically connect them, by facilitating controllable low-loss transmission from one to another. We measured a SSC conversion efficiency of 91% (or –0.4 dB) between the upper and lower waveguide layers for the TE mode at the wavelength of 850 nm.

The wafer used in the experiment consists of five layers of AlGaAs with different aluminum concentrations. They are 5 nm of GaAs, 120 nm of $Al_{0.2}Ga_{0.8}As$, 250 nm of $Al_{0.34}Ga_{0.66}As$, 4 μm of $Al_{0.5}Ga_{0.5}As$, and 3.5 μm of $Al_{0.63}Ga_{0.37}As$ from top to bottom and are grown on an *n*-type (100) GaAs substrate. The first three layers on the top are suitable for implementing high refractive index contrast waveguides (later we call these *Device WGs*) for on-chip signal processing. The two bottom layers were designed as a large-dimension waveguide (later we call these *Coupling WGs*) for efficient end-fire coupling to single-mode fibers. A schematic of the wafer structure is shown in Fig. 1(a). Modal fields were simulated using Lumerical MODE Solutions. The Device WG has a width of 800 nm and a height of 3.175 μm, whereas the Coupling WG has a width of 4 μm and a height of 2.8 μm. The relative power density profiles of the TE_{00} modes of the Device WG and Coupling WG are shown in Figs. 1(b) and 1(c), respectively.

Monolithically integrated SSCs on GaAs substrates can be sorted into two main categories [23]. In the first category, the SSCs include vertical and lateral tapers to adiabatically transfer optical power between waveguides. This approach requires epitaxial regrowth and a more complicated fabrication process. In the second category, SSCs transfer optical power by means of lateral tapers and do not require epitaxial regrowth. In this Letter, we adopted a two-step lateral tapering scheme, which reduces the overall length compared with a single taper. The Device WG includes the 5 nm GaAs cap layer, the 120 nm $Al_{0.2}Ga_{0.8}As$ upper cladding, and the 250 nm $Al_{0.34}Ga_{0.66}As$ core layer. The Coupling WG includes the 4 μm thick $Al_{0.5}Ga_{0.5}As$ as its core layer and the 3.5 μm thick $Al_{0.63}Ga_{0.37}As$ layer for the lower cladding. The dimensions of the Coupling WG were optimized for the highest power overlap integral with

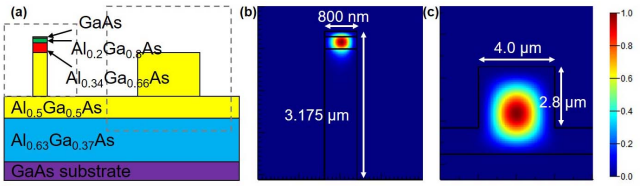

Fig. 1. (a) Wafer structure and schematics of Device WG and Coupling WG. (b) TE_{00} mode profile for an 800 nm wide and 3.175 μm deep Device WG. (c) TE_{00} mode profile for a 4 μm wide and 2.8 μm deep Coupling WG.

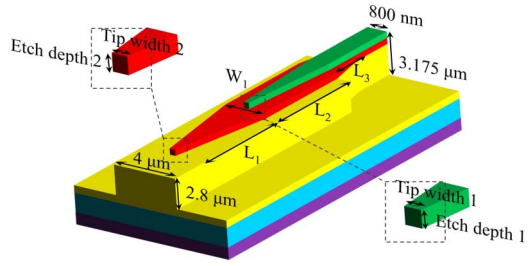

Fig. 2. Perspective view of the proposed SSC. The Device WG is green, the Transition WG is red, and the Coupling WG is yellow.

the fundamental mode of a lensed SMF (OZ optics, TSMJ-3U-840-5/125-0.25-23-2.9-13-1-AR) at a wavelength of 850 nm.

Because the dimensions of the Device WG and Coupling WG have been set in the wafer structure, the design focus is on the tapers. The design parameters of the tapers are noted in Fig. 2. The width of the Device WG is tapered down from 800 nm to 200 nm, a critical dimension that can be easily achieved using electron beam lithography (EBL), over a length of L_2. The width of the transition waveguide (*Transition WG*), which is shown in red in Fig. 2, is tapered down from W_1 to 200 nm over a length of L_1. A third taper section that connects the Device WG and the Transition WG is added, which mainly ensures smooth conversion and eliminates beating effects but does not influence overall conversion efficiency much. As such, its length, L_3, is set to a constant value, 100 μm.

The initial values of L_1, L_2, and W_1 are 600 μm, 280 μm, and 2.4 μm, respectively. These parameters were optimized iteratively. First, we optimized L_2 and W_1 by monitoring the conversion efficiency of Device WG TE_{00} mode to Coupling WG TE_{00} mode with RSoft CAD BPM. The results are shown in Fig. 3(a). As can be seen, the optimum value for the Transition WG width W_1 is about 2.4 μm and that for L_2 is 280 μm. Second, we optimized L_2 and L_1. As shown in Fig. 3(b), the conversion efficiency is more sensitive to L_2 than L_1.

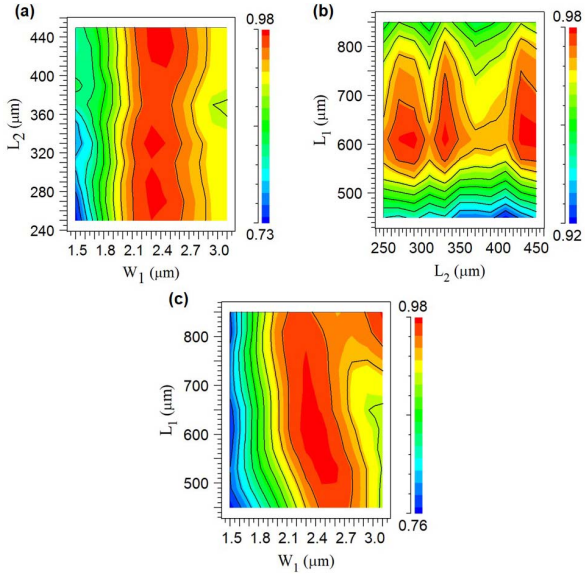

Fig. 3. Dependence of the SSC's conversion efficiency on (a) L_2 and W_1, (b) L_2 and L_1, (c) L_1 and W_1.

The optimum values of L_2 and L_1 are about 600 μm and 280 μm, respectively. Third, we confirmed that the set of values of $L_2 = 600$ μm and $W_1 = 2.4$ μm were optimized, as shown in Fig. 3(c). Last, final taper simulation results are shown in Fig. 4. A total length of about 1000 μm was necessary, and a theoretical conversion efficiency of 97% (or −0.1 dB) was obtained.

We studied the fabrication tolerance of the critical design parameters of the SSC, especially the two shallow etch depths and two taper tip widths, as shown in the two insets in Fig. 2. It is found that *etch depth 2* is more tolerant compared with *etch depth 1*. While etch depth 2 can vary by 40 nm (16% of targeted 250 nm) with only a 5% reduction in conversion efficiency, the same amount of variation in etch depth 1 (20 nm, 16% of targeted 125 nm) would induce a 10% reduction in conversion efficiency. Overall, the conversion efficiency is higher than 88%, as shown in Fig. 5(a).

Overall, the fabrication tolerance of taper tip widths is very high. As shown in Fig. 5(b), a 100% variation (of 200 nm target width) in *taper width 1*, the conversion efficiency reduces by only 9%, while the same amount of variation in taper *tip width 2* barely affects the conversion efficiency. In conclusion, *etch depth 1* and *taper tip width 1* are the most critical dimensions in achieving a high experimental conversion efficiency.

Device fabrication involved electron beam lithography (EBL) followed by inductively coupled plasma, reactive ion etching. In order to achieve precise and highly anisotropic etching, which was critical in fabricating the SSC, two dry etch recipes were developed [24]. The first recipe gives an etch rate of 0.25 nm/s, while the second one gives an etch rate of 20 nm/s. First, we masked the sample with HSQ using EBL, used the slow etch recipe to etch through the 5 nm GaAs and 120 nm $Al_{0.2}Ga_{0.8}As$, and achieved an accurate etch depth of 125 nm. We then removed HSQ using buffered oxide etcher (BOE). Next, we masked the sample with HSQ using EBL, etched through the 250 nm $Al_{0.34}Ga_{0.66}As$ layer using the slow-etch recipe, and removed HSQ using BOE afterward. Last, we masked the sample with HSQ using EBL and used the fast etch recipe to etch 2.8 μm into the 4 μm $Al_{0.5}Ga_{0.5}As$ layer. We used a Ti:sapphire laser as a light source at the wavelength of 850 nm to excite fundamental TE modes of the waveguides. The input and output objective lenses were Newport M-60× (0.85 NA and 2.9 mm focal length) and Newport M-40× (0.65 NA and 4.5 mm focal length), respectively, for the measurement of the waveguide output mode profiles, Device WG propagation loss and the conversion efficiency of the SSC. Some SEM images of fabricated SSCs along with measured waveguide output mode profiles are shown in Fig. 6. The propagation loss of Device WG was measured using samples with straight Device WGs of various lengths. The output power from the Device WG was measured as a function of waveguide length. An average propagation loss of 6.7 dB/cm was measured.

In order to measure the conversion efficiency of SSCs, four groups of SSC devices were fabricated. The first group consisted of straight Device WGs, which ran all the way from input facet to output facet, and served as a reference group. In other words, zero SSC were integrated in this group. The second group included one SSC that coupled light from Device WG to Coupling WG. The third group included two SSCs, which coupled light from Device WG to Coupling WG, then back to Device WG. The fourth group included three SSCs, which coupled light from Device WG to Coupling WG, then to Device WG, and finally to Coupling WG. Lengths of all these devices were the same at about 5 mm. We kept the input optical power before the input lens constant at 1 mW for all the devices and measured the output power. The output power of all four groups was normalized to the first group, as shown in Fig. 7. Each data point represents the average output power of one group of devices.

Using the experimental data in Fig. 7, we measured an average conversion efficiency of 91% for the spot size converters that we designed and fabricated. The propagation loss of the Coupling WG was fitted using the experimental data and was found to be negligible over the device lengths used. In order

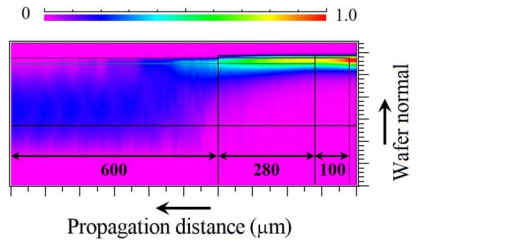

Fig. 4. Plot of the evolution of the relative power density along the two-layer taper-assisted coupler.

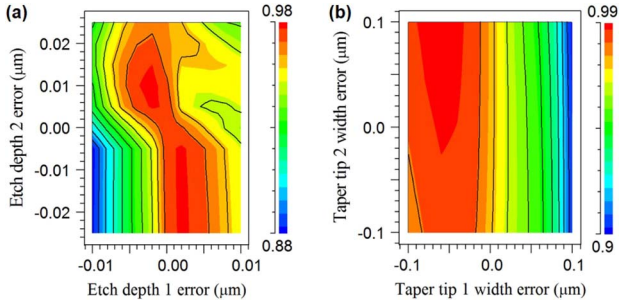

Fig. 5. Fabrication tolerance of the coupling efficiency: (a) two shallow etch depths and (b) two taper tip widths. Positive (negative) values on x and y axis means larger (smaller) than target depths or widths were achieved.

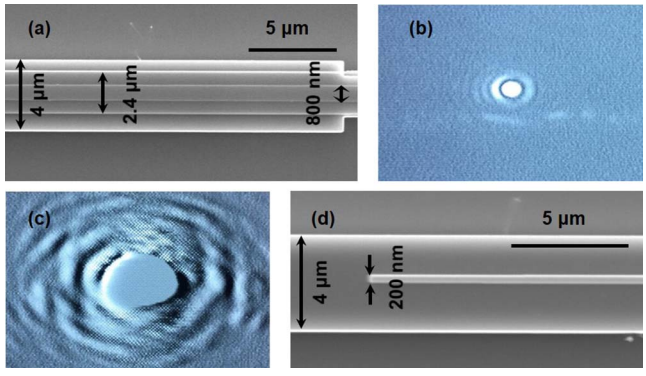

Fig. 6. SEM images of (a) the starting section and (d) ending section of the spot-size converter. Measured output mode profiles of the (b) Device WG and (c) Coupling WG.

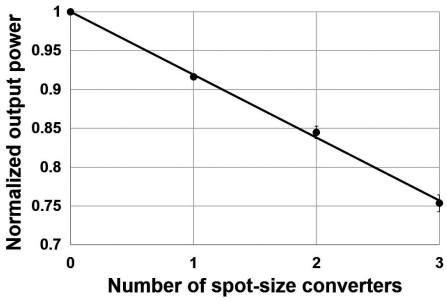

Fig. 7. Normalized output power of the four groups of devices with different number of integrated SSCs.

to measure the coupling efficiency between the Coupling WG and a SMF, we used two lensed SMFs with a focused beam waist of 2.5 μm (OZ optics, TSMJ-3U-840-5/125-0.25-23-2.9-13-1-AR). A group of straight Coupling WGs, which ran all the way from the input facet to the output facet, was used. The input power from the SMF to the Coupling WGs was 1 mW. After the light propagated in the Coupling WG for about 5 mm, the output power collected using the second SMF was 304 μW. Assuming the propagation loss of the Coupling WG was negligible over the device lengths used, as we had previously demonstrated, and that light was only lost at the input and output facets, the above results translated into a coupling efficiency of 55% per facet between the Coupling WG and a SMF. The effective index of the fundamental TE/TM modes of the Coupling WG was 3.251, giving rise to a Fresnel reflection coefficient of 28% between air and the Coupling WG. After correcting for the Fresnel reflection, a 77% power overlap integral was obtained. The result agreed well with the theoretical power overlap integral between the fundamental TE/TM modes of the Coupling WG and those of the SMF by Lumerical MODE Solutions, which was calculated to be about 80%. The same approach was used to measure the power overlap integral between the Device WG and the SMF, which was 15% after correcting the Fresnel reflection. The integration of SSCs increased the coupling efficiency by fivefold. We theoretically studied the displacement tolerance for two cases: with and without SSCs. The 1 dB horizontal and vertical displacement tolerances for the Coupling WG were both 1.4 μm. The 1 dB horizontal and vertical displacement tolerances for the Device WG were both 0.9 μm.

In conclusion, we have designed and fabricated a vertically integrated SSC in AlGaAs–GaAs, which allows for an efficient and displacement-tolerant coupling of the SMF to the Device Waveguide, via Coupling Waveguide. The measured insertion loss on a transmission from the Coupling Waveguide to the Device Waveguide is only 0.4 dB (91% transmission), suggesting high efficiency of the adiabatic tapering system that connects two waveguides. SMF to the Device Waveguide insertion loss measured at −3 dB (−1.5 dB after correction for 28% Fresnel reflection at uncoated facet), still leaving room for improvement, e.g., by optimization of the Coupling Waveguide layer structure and layout. Demonstration of the vertically integrated SSC well-performing at 850 nm marks a major step toward building the TAVI platform in GaAs as a versatile and cost-efficient PIC technology for applications in data center interconnects, noninvasive biosensing, and quantum optics.

Funding. Canadian Microelectronics Corporation Microsystems (CMC); Natural Sciences and Engineering Research Council of Canada (NSERC); Collaborative Research and Training Experience (CREATE) program of Canada.

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