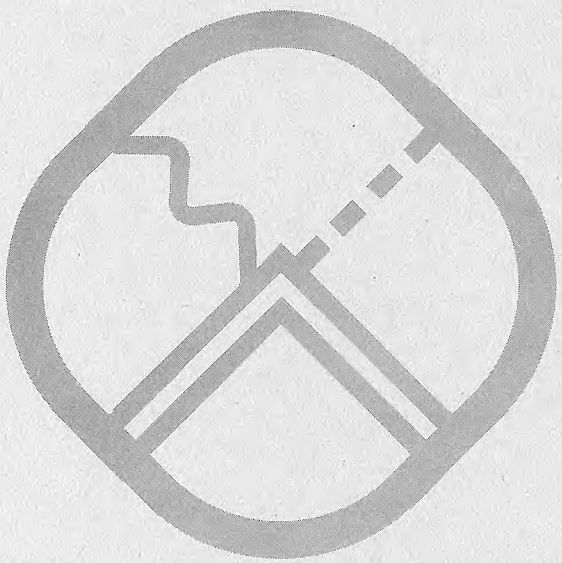
REPORT CTSL– 22

# SOME TRANSISTOR SMALL SIGNAL EQUIVALENT CIRCUIT CALCULATIONS

*ARPAD BARNA*

MARCH 28, 1961



*SYNCHROTRON LABORATORY*

CALIFORNIA INSTITUTE OF TECHNOLOGY

PASADENA

Report CTSL-22

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# SOME TRANSISTOR SMALL SIGNAL EQUIVALENT CIRCUIT CALCULATIONS

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Contents

## Introduction

Transient responses, input and output impedances have been derived for the use of the circuit designer. A hybrid equivalent circuit was assumed to be correct and has been used as the basis of the derived relationships.

Grounded emitter, grounded base, grounded collector and emitter degenerated configurations are discussed.

## I Basic Equivalent Circuits

A small signal emitter input transistor equivalent circuit for diffused base transistors, for times larger than $\tau_o$ is shown in Fig. 1.1. The corresponding base input circuit is in Fig. 1.2.

In both circuits

$$r_e = \frac{kT}{qI_{eDC}} \approx \frac{25 \text{ mv}}{I_{eDC}}$$

and $$\tau_o = \tau_\alpha + \tau_d \ .$$

## II Some Typical Transistor Parameter Values

| Transistor | $\tau_\alpha$ nsec | $\tau_o$ nsec | rs ohms | $\beta_o$ | Ccb* pF | at Vcb Volts |
|---|---|---|---|---|---|---|
| 2N 1500 | 0.25 | 0.5 | 5 | 75 | 2.5 | 3 |
| 2N 1742 | | 0.2 | 8 | 50 | 1.5 | 12 |

*$C_{cb} = Ccb_1 + C_{cb2}$

Theoretical value for Ccb:

$$C_{cb} \cong C_{stray} + \frac{k_1}{V^n} \qquad \text{where} \qquad n = \frac{1}{3} \text{ to } \frac{1}{2}$$

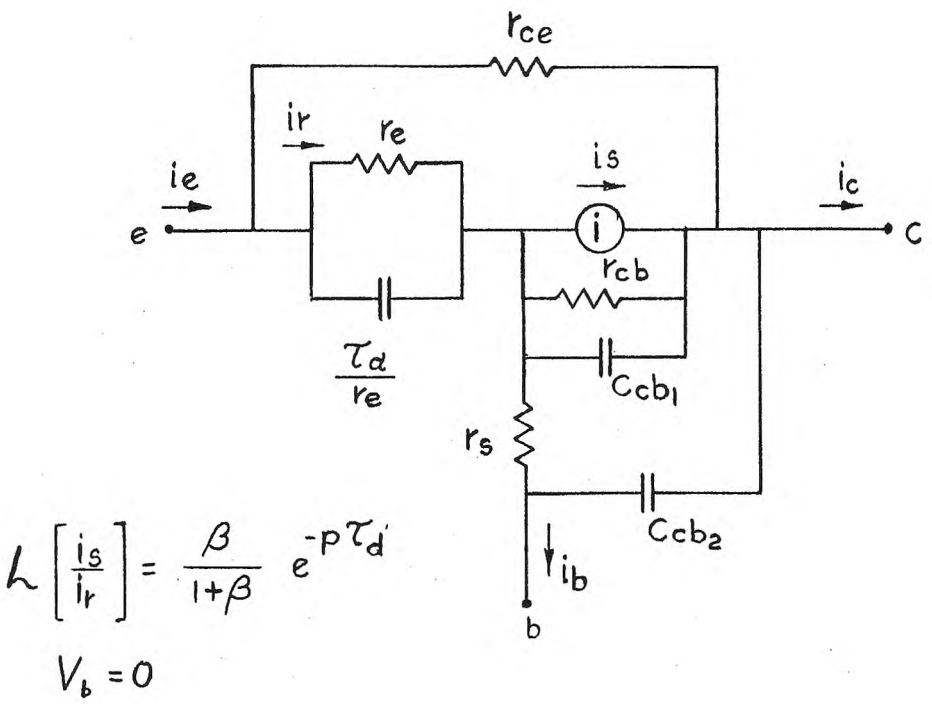


FIGURE 1.1

Emitter input small signal equivalent circuit.

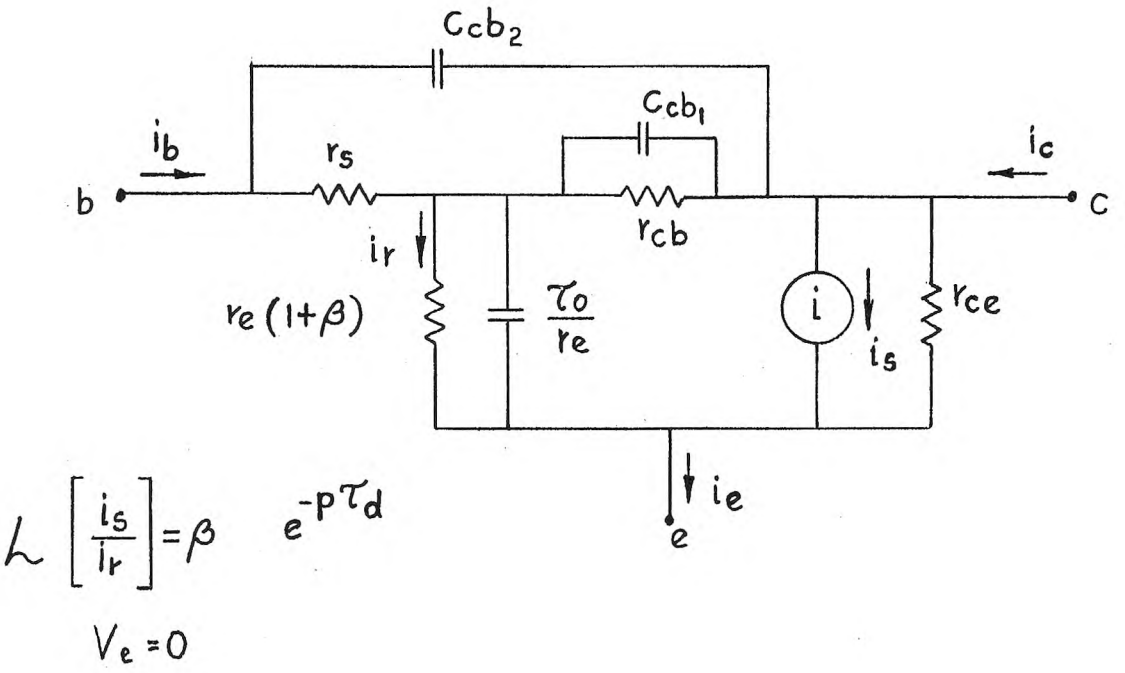


FIGURE 1.2

Base input small signal equivalent circuit.

III Grounded Emitter Configuration (Fig. 3.1)

Conditions: Current source input; short circuited output; $C_{cb2} = 0$; $C_{cb1} \ll \tau_o/\beta r_e$ ; $r_{cb} \gg \beta r_e$ ; $r_{ce} \gg \beta r_e$. Using the base input equivalent circuit, we get for the current transfer:

$$L\left[\frac{i_c}{i_b}\right] = \frac{\beta}{1 + p\tau_o\beta}\, e^{-p\tau_d}$$

and for the input impedance (Fig. 3.2):

$$L\left[\frac{V_b}{i_b}\right] = r_s + \frac{r_e(1 + \beta)}{1 + p\tau_o(\beta + 1)} \cong r_s + \frac{\beta r_e}{1 + p\tau_o\beta} \quad (\text{for } \beta \gg 1)$$

IV Grounded Base Configuration (Fig. 4.1.1)

4.1 Current transfer and input impedance.

Conditions: Current source input; short circuited output; $C_{cb} = 0$; $r_{ce} \gg r_s + r_e$. Using the emitter input circuit, we get for the current transfer:

$$L\left[\frac{i_c}{i_e}\right] = \frac{\beta}{1 + \beta}\, \frac{1}{1 + p\tau_\alpha}\, e^{-p\tau_d}$$

and the input impedance of Fig. 4.1.2.

4.2 Grounded base configuration with resistive input impedance.

If we load the input with a network of Fig. 4.2.1, the resulting impedance will have a resistive value of

$$\frac{r_s(r_e + r_s/\beta)}{r_s(1 + \frac{1}{\beta}) + r_e} \quad (\text{for } r_e \gg r_s/\beta) \quad .$$

Or if we insert a series network of Fig. 4.2.2, the resulting resistance will be

$$Z = r_e + r_s\,\frac{1 + \beta}{\beta} \cong r_e + r_s \quad (\text{for } \beta \gg 1) \quad .$$

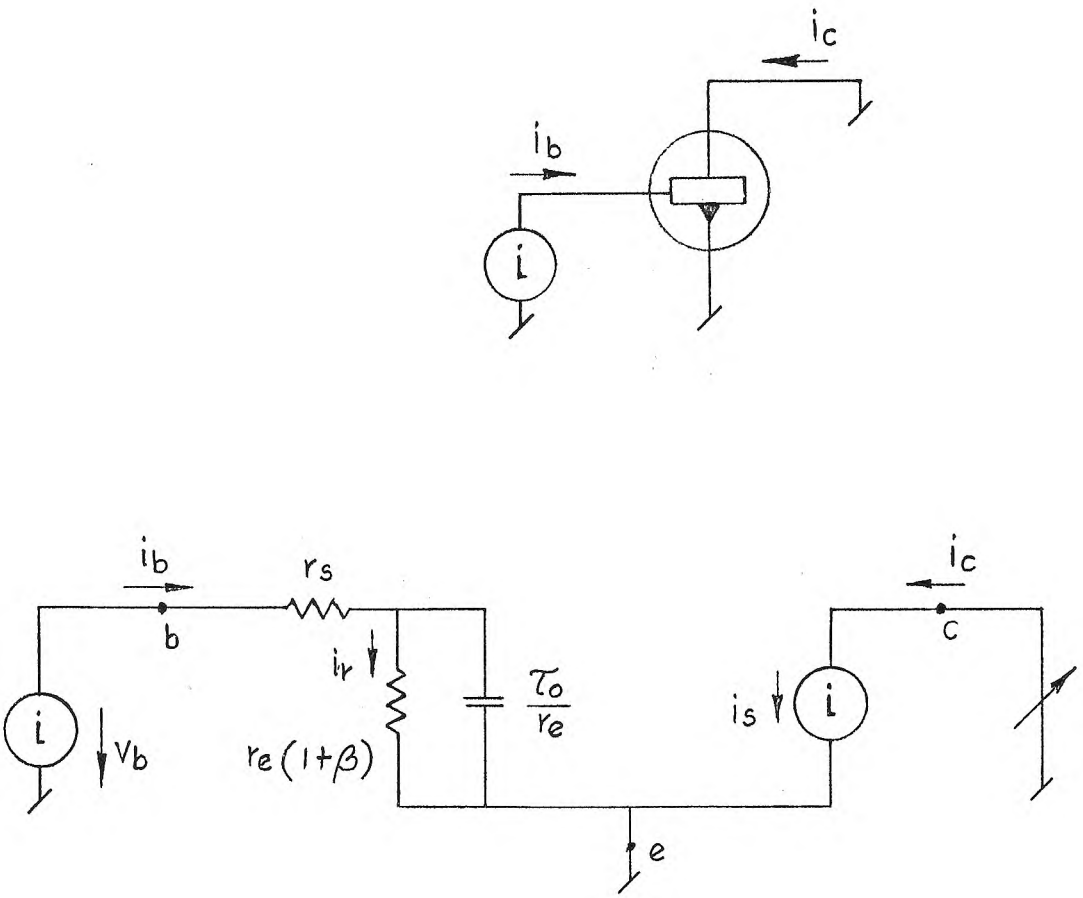


FIGURE 3.1

Grounded emitter stage.

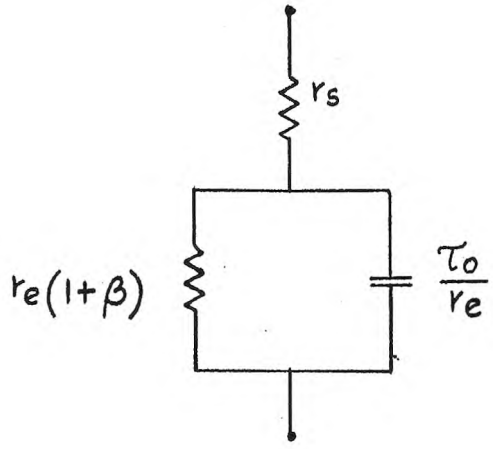


FIGURE 3.2

Input impedance of a grounded emitter stage.

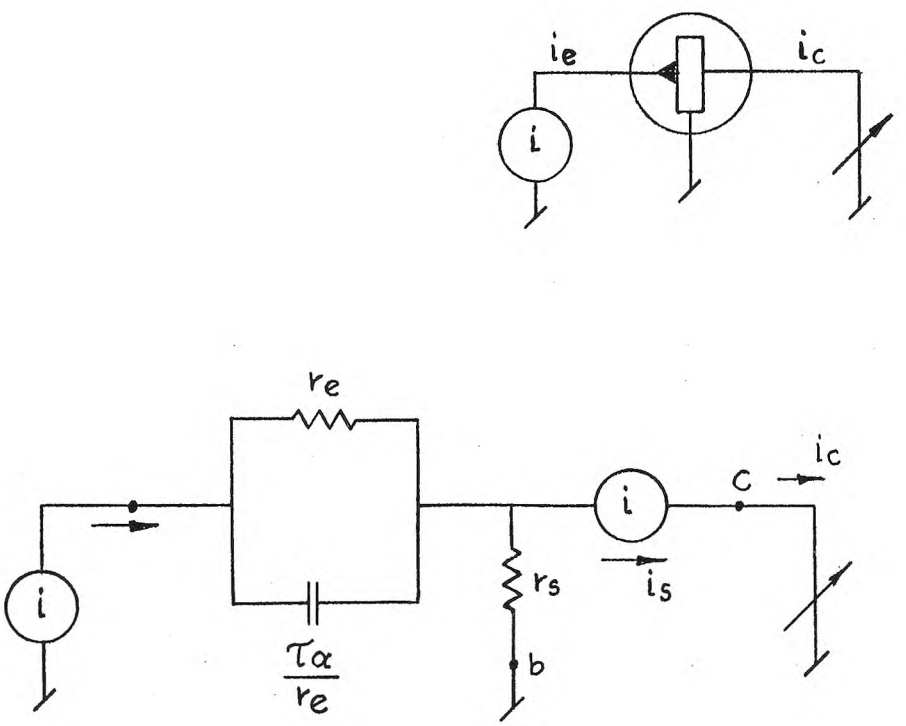


FIGURE 4.1.1

Grounded base stage.

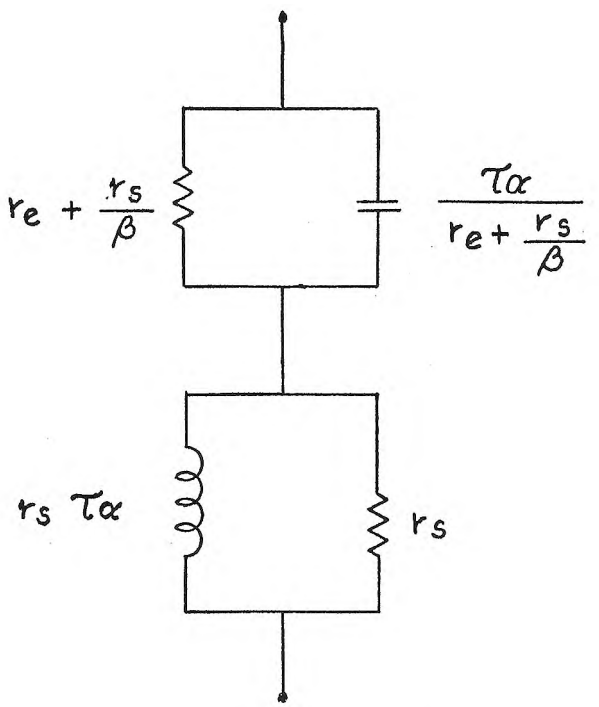


FIGURE 4.1.2

Input impedance of a grounded base stage.

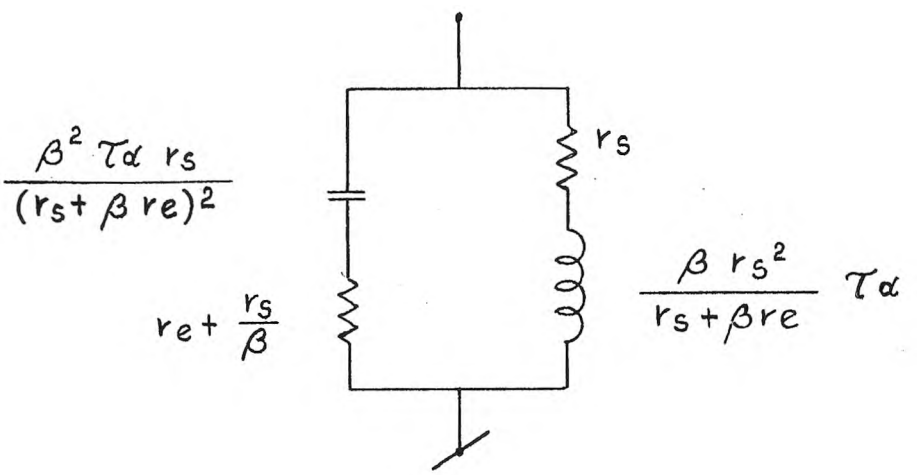


FIGURE 4.2.1

Parallel compensating network for the input of a grounded base stage.

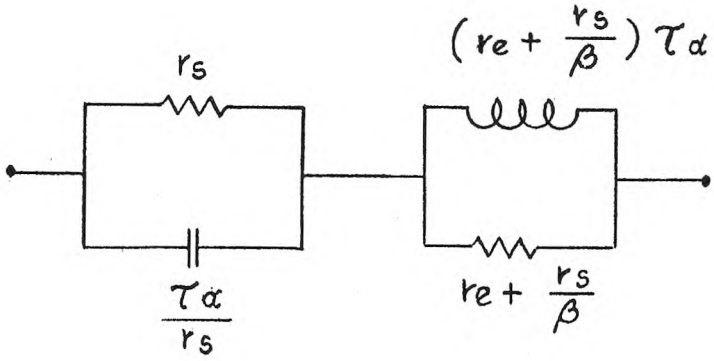


FIGURE 4.2.2

Series compensating network for the input of a grounded base stage.

## V Grounded Collector Configuration (Fig. 5.1.1)

### 5.1 Current transfer and input impedance.

Conditions: Current source input; short circuited output; $C_{cb2} = 0$; $C_{cb1} \ll \tau_o/\beta r_e$ ; $r_{cb} \gg \beta r_e$. Using the base input circuit, we get for the current transfer:

$$L\left[\frac{i_e}{i_b}\right] = \frac{\beta}{1 + p\tau_o\beta}\, e^{-p\tau_d} + 1$$

and obtain the input impedance of Fig. 5.1.2.

### 5.2 DC voltage transfer (Fig. 5.2.1).

Conditions: $r_{cb} \gg \beta r_e$ ; $r_{ce} \gg R_o$ ; $t \gg \beta\tau_o$ . Using the base input circuits, we get for the voltage transfer:

$$\frac{V_e}{V_o} = \frac{1}{1 + \dfrac{r_e + \dfrac{R_o + r_s}{1 + \beta}}{R_L}}$$

and for the input resistance (Fig. 5.2.2):

$$R_{in} = R_o + r_s + (r_e + R_L)(1 + \beta) \cong R_o + r_s + \beta(r_e + R_L)$$

(for $\beta \gg 1$)

$$R_{out} = \frac{-V_o}{i_e} = r_e + \frac{R_o + r_s}{1 + \beta} \cong r_e + \frac{R_o + r_s}{\beta} \qquad (\text{for } \beta \gg 1)$$

Thus, we obtain the DC equivalent circuit of Fig. 5.2.3.

### 5.3 Transient response for step voltage input (Fig. 5.3.1).

Conditions: Resistive source impedance ($R_o$); parallel RC load; $C_{cb} = 0$; $r_{ce} \gg R_o$ ; $\beta \gg 1$. Using the emitter input circuit, we get:

$$L\left[\frac{V_L}{V_{in}}\right] = \frac{1 + p\tau_\alpha}{\frac{R_o'}{R_L}(p\tau_o)^2 + \frac{r_e}{R_L}\left(1 + \frac{k}{c}\right) p\tau_o + \frac{r_e^2}{R_o' R_L c}}$$

where

$$R_o' = R_o + r_s$$

$$K = \frac{1 + \frac{R_L}{R_o'}\frac{\tau_\alpha}{\tau_o}}{1 + \frac{R_L}{r_e} + \frac{R_o'}{\beta r_e}}$$

$$c = \frac{C_L r_e^2}{\tau_o R_o'} \frac{1}{1 + \frac{r_e + R_o'/\beta}{R_L}}$$

The response for a step voltage input will be free of ringing if the roots of the denominator are real:

$$\left(1 + \frac{k}{c}\right)^2 \geq \frac{4}{c} \qquad \text{or} \qquad c^2 + c\left[2k - 4\right] + k^2 \geq 0 \ .$$

This represents a parabola, where $C_- < C < C_+$ leads to ringing. These critical values of C, $C_\pm = 2 - k \pm 2\sqrt{1 - k}$, are plotted on Fig. 5.3.2. Using either of these critical values, the response:

$$L\left[\frac{V_L}{V_{in}}\right] = \text{const.} \frac{1}{1 + p\tau^*}$$

where

$$\tau^* = \tau_o \frac{R_o'}{r_e} \frac{2}{1 + \frac{k}{c}} = \tau_o \frac{R_o'}{r_e} y = \frac{y}{k} \frac{1 + \frac{R_L}{R_o'}\frac{\tau_\alpha}{\tau_o}}{\frac{r_e + R_L}{R_o'} + 1/\beta}$$

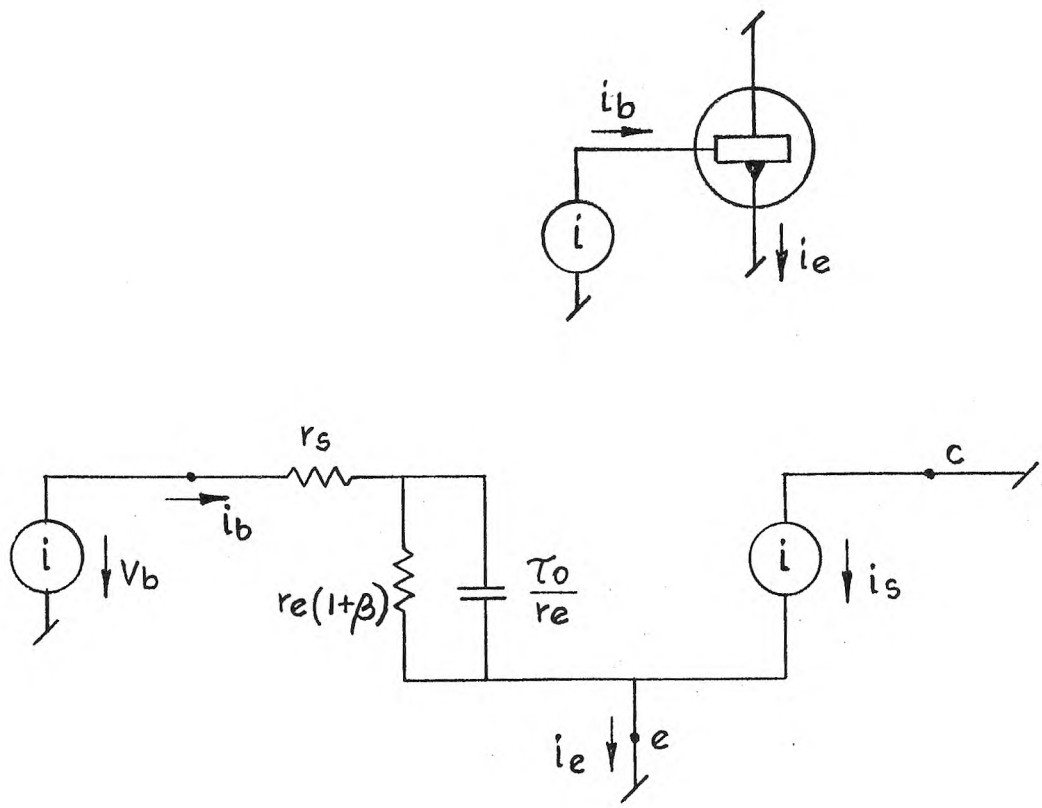


FIGURE 5.1.1

Grounded collector stage.

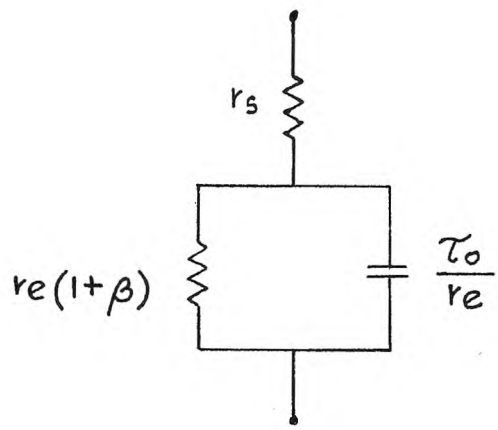


FIGURE 5.1.2

Input impedance of a grounded collector stage.

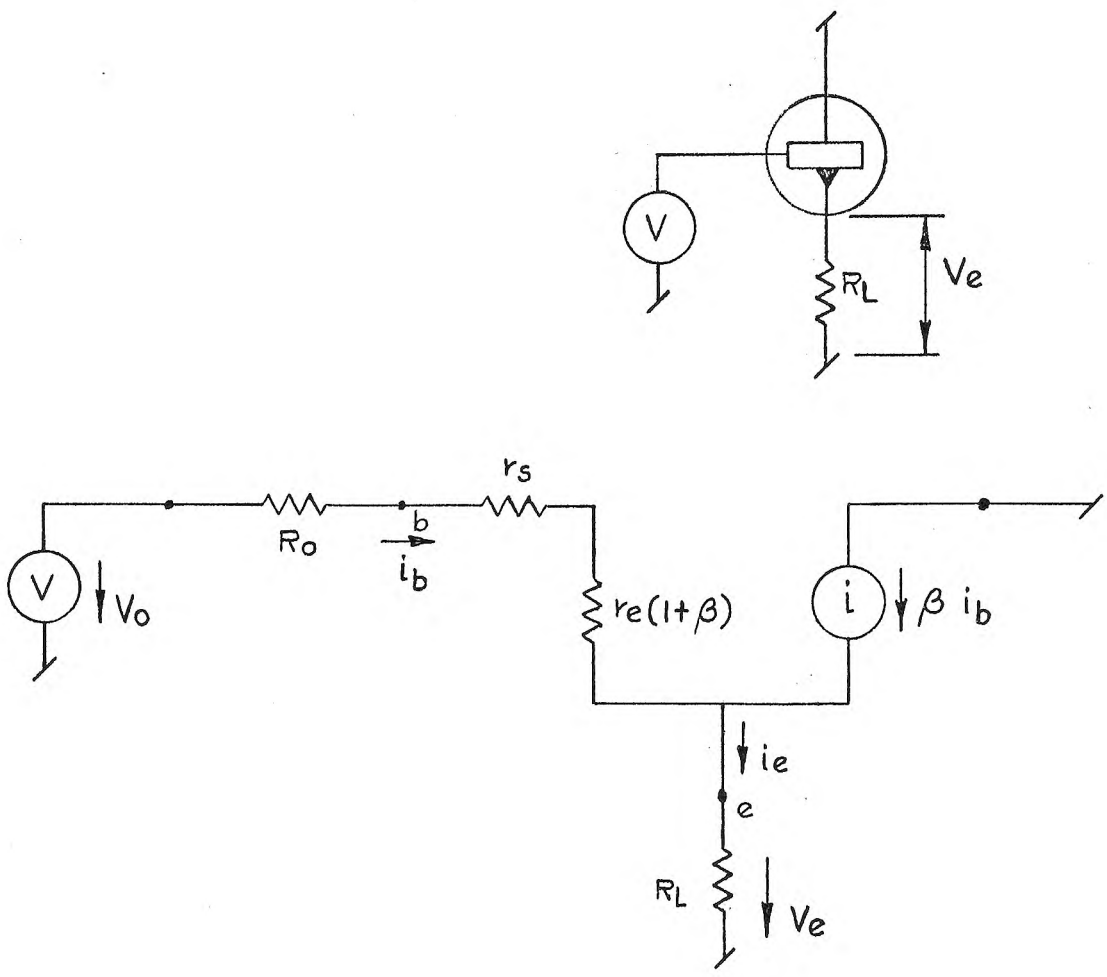


FIGURE 5.2.1

DC conditions for a grounded collector stage.

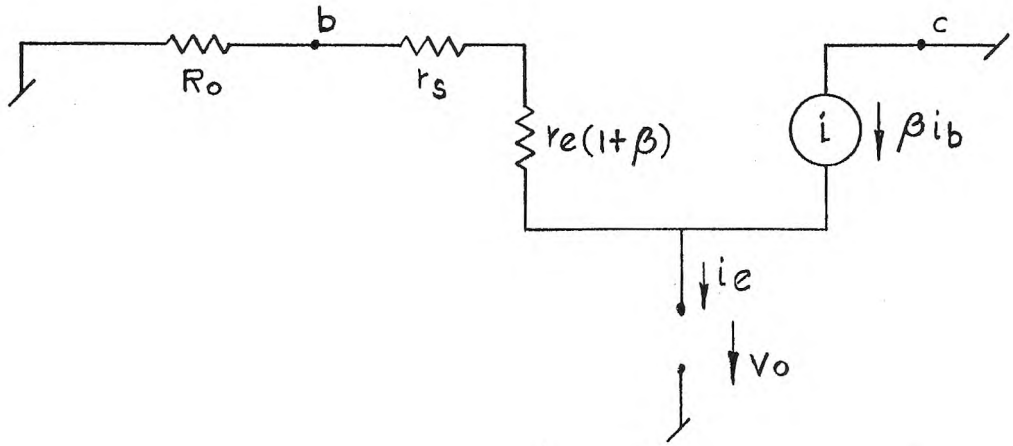


FIGURE 5.2.2

DC input impedance of a grounded collector stage.

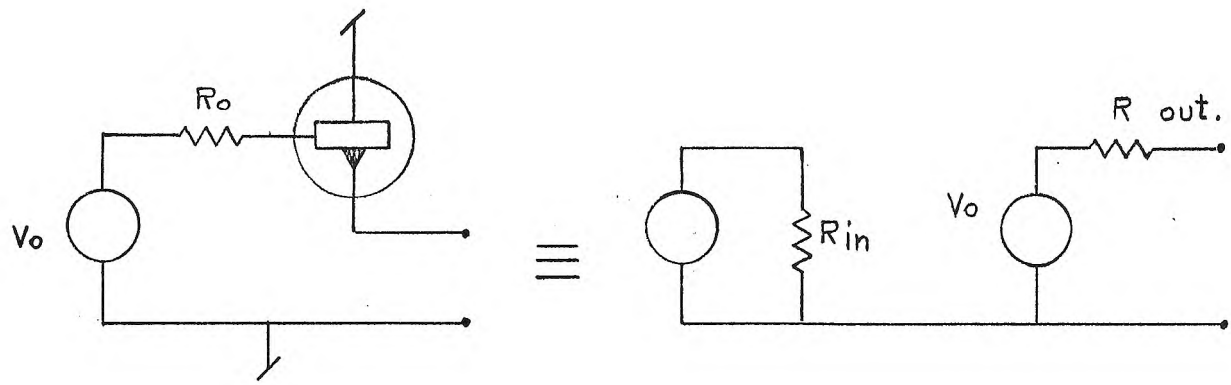


FIGURE 5.2.3

DC equivalent circuit of a grounded collector stage.

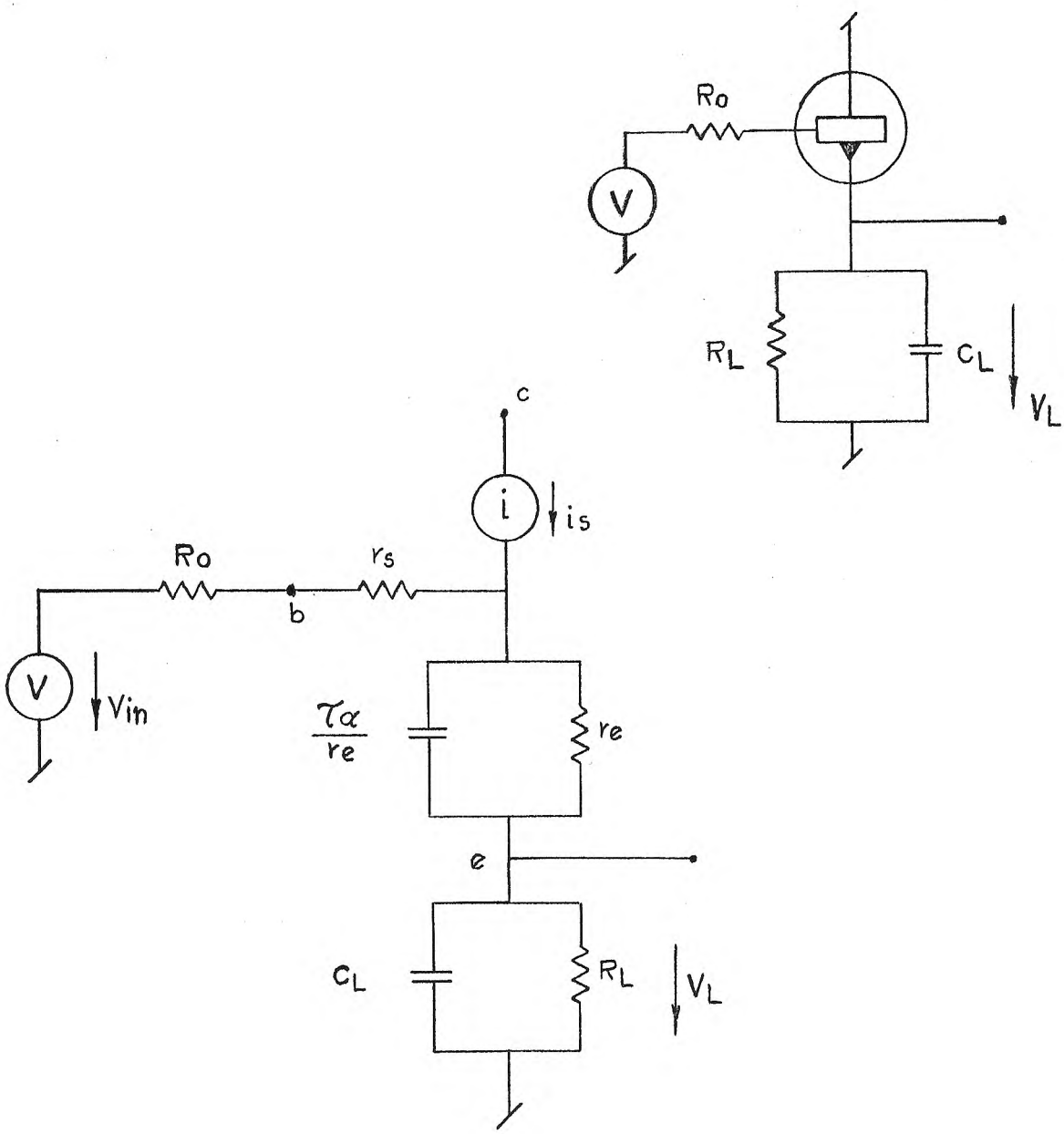


FIGURE 5.3.1

Grounded collector stage.

for $$\beta \gg \frac{R_o'}{r_e + R_L}$$

$$\frac{\tau^*}{\tau_o} \cong \frac{R_o' + R_L \frac{\tau_\alpha}{\tau_o}}{r_e + R_L} \frac{y}{k}$$

Values of $\frac{y}{k}$ as functions of k, $y_+$ corresponding to $c = c_+$, $y_-$ to $c = c_-$ are plotted on Fig. 5.3.2. Furthermore,

$$C_L \pm = (C \pm) \frac{\tau_o R_o'}{r_e^2} \left(1 + \frac{R_o' + \beta_{re}}{\beta R_L}\right)$$

for $k \ll 1$

$$C_+ \cong 4$$

$$C_- \cong \frac{k^2}{4}$$

$$Y_+ \cong 2$$

$$\frac{Y_-}{k} \cong 0.5$$

For $k > 1$ the response is always free of ringing.

## 5.4 Grounded collector configuration with resistive output impedance.

Conditions: $C_{cb} = 0$; $r_{ce} \gg R_o$ ; resistive source impedance (Fig. 5.4.1). The output impedance thus is as in Fig. 5.4.2.

If we load the output with a network of Fig. 5.4.3, the resulting impedance will be resistive. Or if we insert a series network of Fig. 5.4.2, the output impedance will be resistive:

$$Z = r_e + (r_s + R_o)\left(\frac{1 + \beta}{\beta}\right) \cong r_e + r_s + R_o \quad (\text{for } \beta \gg 1)$$

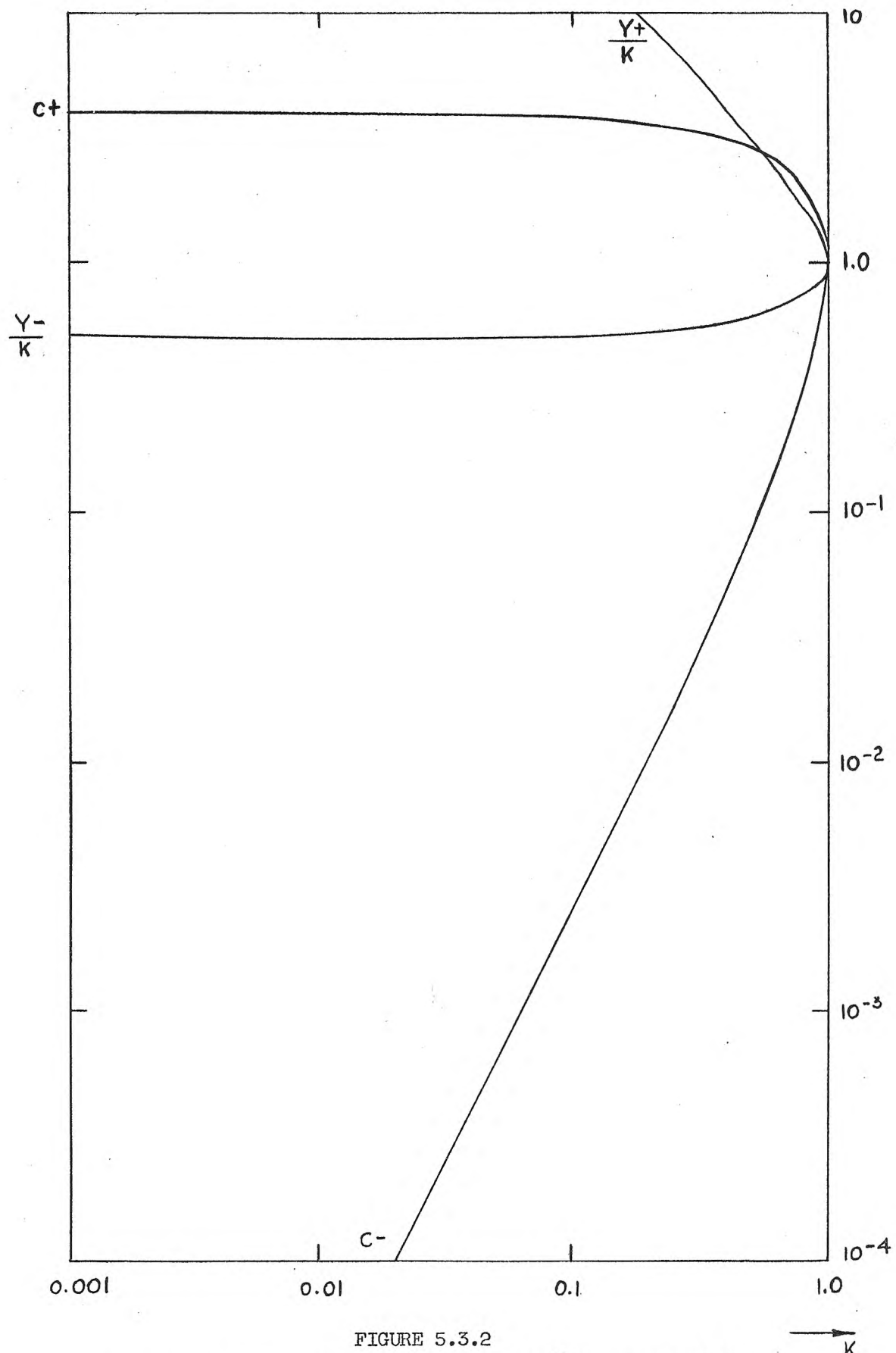


FIGURE 5.3.2

Critical load capacitances and values of $\frac{Y}{k}$ for a grounded collector stage.

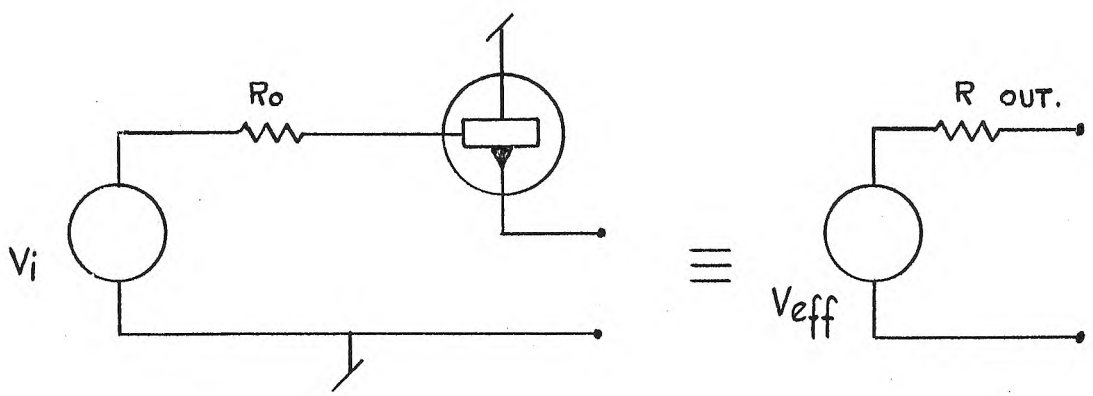


FIGURE 5.4.1

Equivalent circuit of a grounded collector stage with resistive output impedance.

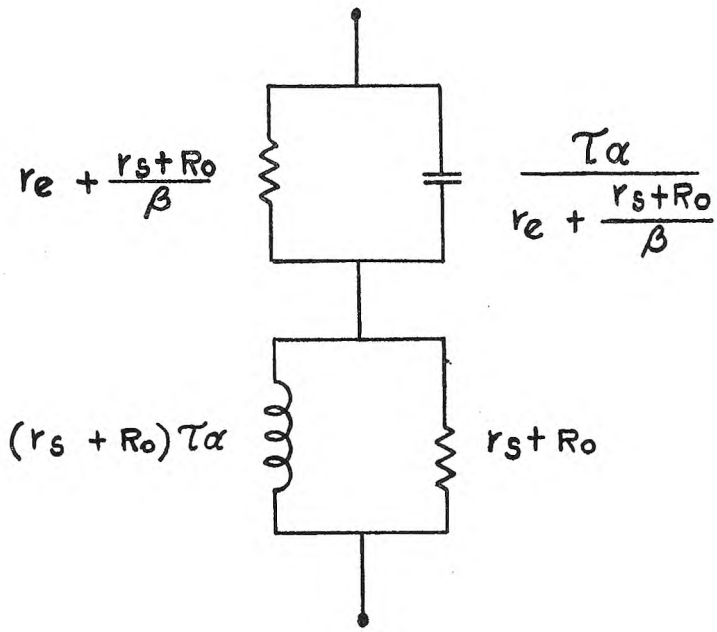


FIGURE 5.4.2

Output impedance of a grounded collector stage.

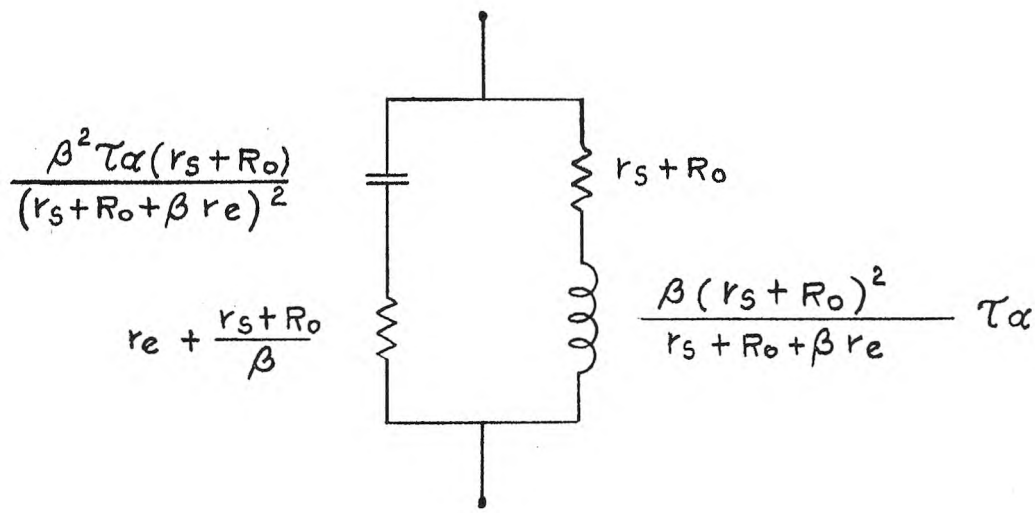


FIGURE 5.4.3

Parallel compensating network for the input of a grounded collector stage.

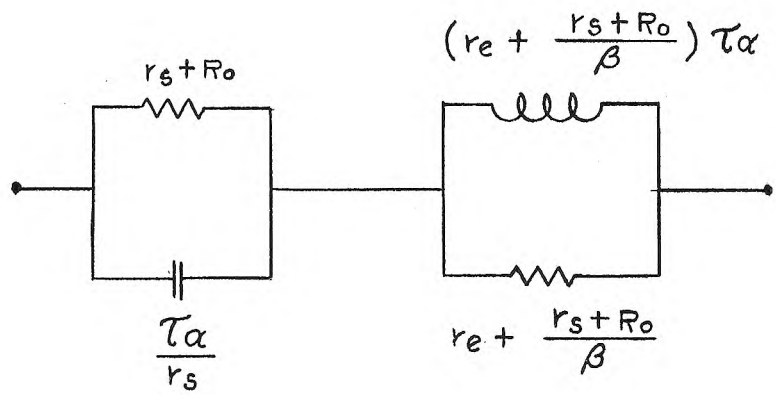


FIGURE 5.4.4

Series compensating network for the input of a grounded collector stage.

VI Emitter Degenerated Configuration (Fig. 6.1)

Conditions: Voltage source input, short circuited output, $r_s = 0$. Using the emitter input equivalent circuit, we get for the transconductance:

$$L\left(\frac{ic}{V_{in}}\right) = \frac{\alpha}{r_e + R_L} e^{-p\tau_o}$$

and obtain the input impedance of Fig. 6.2.

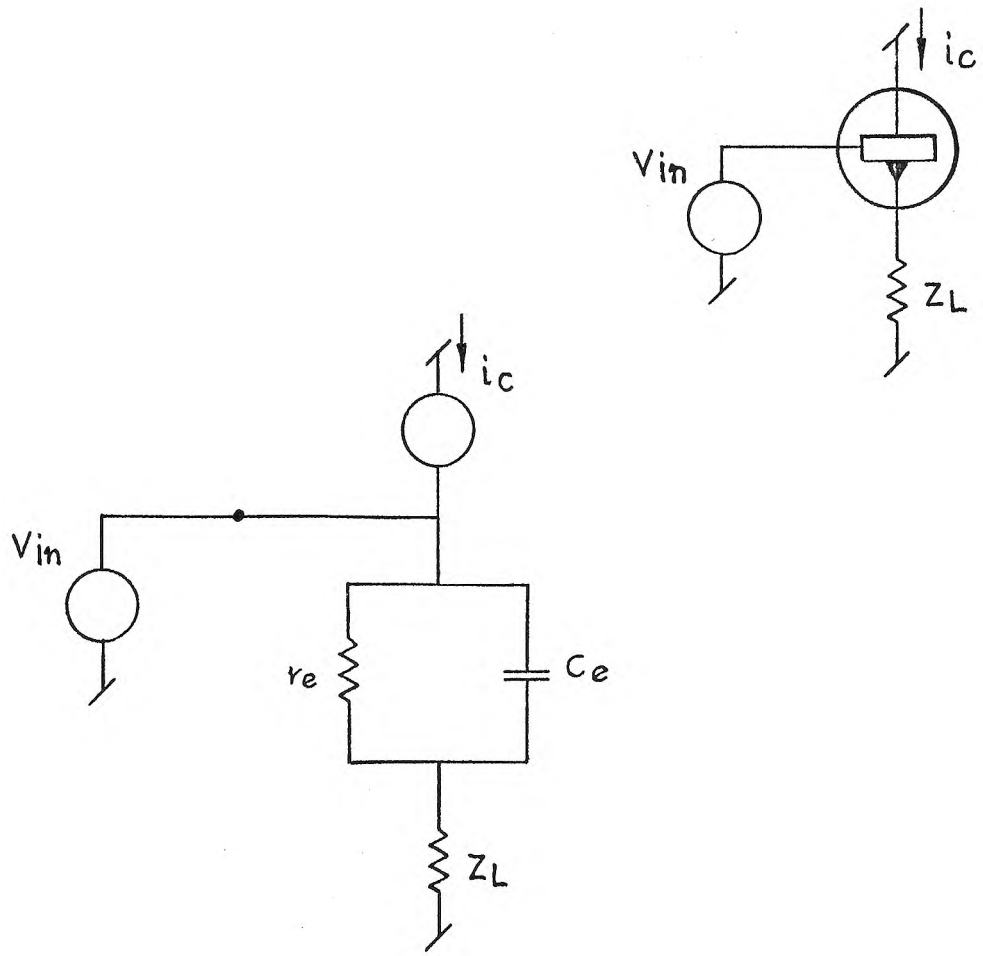


FIGURE 6.1

Emitter degenerated stage.

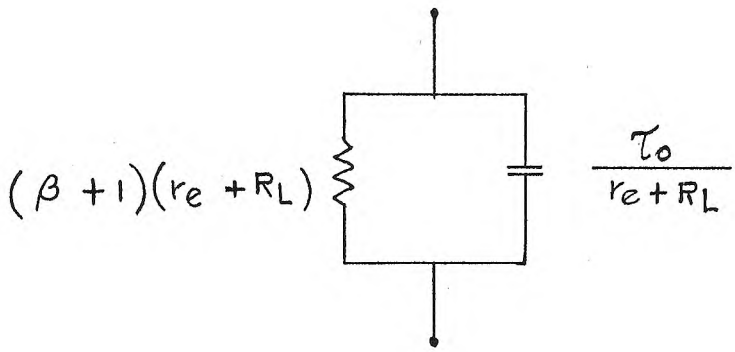


FIGURE 6.2

Input impedance of a critically damped emitter degenerated stage.

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