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A 50 NANOSECOND LINEAR GATE CIRCUIT USING TRANSISTORS

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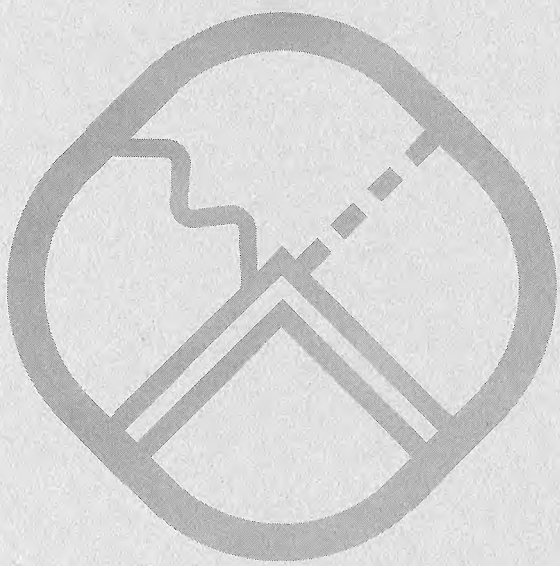

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Acknowledgments

The valuable comments and suggestions of M. Sands and A. V. Tollestrup are gratefully acknowledged.

I Introduction

In the past, linear gate circuits for gating pulses of photomultiplier tubes have been mostly based on semiconductor diodes[1,2,3]. Using diffused base transistors as a gate in an emitter input configuration provides favorable linearity and feedthrough properties. The circuit described here is an improved version of one developed by A. V. Tollestrup.

The basic circuit employs two 2N502A transistors in a difference amplifier configuration. The gating pulse is applied symmetrically to the bases with the signal entering at the common emitters. A proportion of the gating pulse is added to the output to cancel the pedestal, along with a slight positive feedback to reduce the transients. Three outputs are provided, each intended to drive a pulse shaper. A switch is provided to select "External", "Gate on", or "Gate off" operation.

II The Circuit

General:

The block diagram of the circuit is shown on Fig. 1.[4)*]

The input signal is first passed through a 125 Ω attenuator having a maximum attenuation of 50 in 40 per cent steps. The signal is then inverted by T_1 and passed to the gating transistors T_2 and T_3. The input inverter stage presents a 125 Ω input impedance and contains a 10:1 resistive divider for a monitor pick-off. The actual gating is done in the gate stage by T_2 and T_3. If the gate is open, the input signal is passed to the output inverter stage (T_4) and thence to the 3 output stages (T_5, T_6, T_7). If the gate is closed, the input signal is passed to ground on the collector of T_2.

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1) A. V. Tollestrup and J. B. Lindsay, CERN Report 58-20 (1958).

2) E. L. Garwin, Rev. Sci. Instr. 30 (1959).

3) F.P.G. Valckx and A. Dymanus, Nuclear Instr. and Methods 7, 1960.

4) A. Barna, J.H. Marshall, M. Sands, Nuc. Instr. and Methods, 7, 1960.

*) For symbols and equivalent circuits, see Ref. 4.

The gate signal input is terminated in 125 Ω containing a resistive divider monitor pick-off. If the Gate Switch is in the "Ext." position, the gate signal passes to the gate generator (T_8, T_9) where two standard, symmetrical signals are generated which open the gate. If the Gate Switch is in the "On" position, the gate is always open, and if it is in the "Off" position the gate is always closed. In both cases, the gate input is disconnected from the gate generator.

Attenuator

The attenuator consists of 125 ohm π networks inserted in 40 per cent steps with a maximum attenuation of 50. When loaded with 125 Ω, it presents a 125 Ω impedance to the signal input. (Fig. 2).

The values of the resistors are the following:

TABLE 1. 125 ohm Attenuator. Resistor Values.

Multiplier	R_1	R_3	R_4	R_5	R_6	R_7	R_8
1.0	Open	Short					
.75	910	36					
.5	375	95					
.3	235	190					
.2	187.5	300					
.15	169	407.5					
.1			330	125	120	250	200
.075			210	235	110	190	235
.05			190	300	100	235	200
.03			187.5	300	89	407.5	169
.02			172	385	75	482	161.5

Input Inverter (T_1 and T_{10}) (Fig. 3)

Transistor T_1 acts as an inverter and limiting stage. It provides a 125 Ω termination of the input cable due to the low input capacity of an emitter follower. It has a high output impedance at its collector making it nearly an ideal current source for driving the gating trans-

istors T_2 and T_3. Its output signal current is $-V_{input}/125\ \Omega$, thus making it an inverter stage for signals less than its saturation voltage of 6V. For larger signals the transistor saturates and thus limits the current driven into the gating transistors (T_2, T_3) reducing feedthrough of large inputs.

Transistor T_{10} is the other half of a difference amplifier for D.C. signals, and thus the setting of the Pedestal Adj. potentiometer (500 Ω) determines the fraction of the current in the 3K resistor to +27V which flows in T_1. Since this current is critical in the D.C. Pedestal Adjustment, a difference amplifier is used to minimize temperature drifts of this current. To aid this cancellation of temperature drifts of the emitter-base voltages of T_1 and T_{10}, they are transistors of the same type mounted in a common heat sink and carry roughly the same current at similar collector voltages.

T_{10} also presents a low impedance (~ 10 Ω) in order to recover the 50 μF condenser on its emitter against pile-up at high counting rates. This is done without producing a significant change in the current of T_1 so long as the average input current is less than the current in T_{10}. Since this current is about 2.5 mA, this corresponds to a 10 per cent duty cycle of -2.5V., 10 ns wide, pulses. This is part of an attempt to design the signal section of the gate before the output of the gating section (i.e., before T_4) to have no serious pile-up. For this reason the gate is D.C. coupled up to this point except at the emitter of T_{10}, and this point is recovered by a very low impedance.

Gate Generator (T_8 and T_9)

Transistors T_8 and T_9 convert the input gating pulse into two standard pulses; one positive and one negative. This circuit is D.C. coupled, allowing the use of very long gating pulses and the possibility of simulating gating pulses with the Gate Switch.

When the Gate Switch is in the "Off" or "Ext." positions, T_9 is conducting the current in the 2K and 3K resistors to +27V. T_8 is cut off since the base of T_9 is at -1.5V, while the base of T_8 is at ground. The D.C. levels are so arranged that D_1 and D_4 are conducting. When the Gate

Switch is "On", the base of T_8 is lowered to -2V, causing it to conduct and T_9 to be cut off. This reverses the role of T_8 and T_9 making D_2 and D_3 the conducting diodes. As discussed in the paragraph concerning the operation of the gating transistors (T_2 and T_3), these diodes (D_1, D_2, D_3, D_4) determine whether a signal is or is not passed by the gate.

When the Gate Switch is in either the "On" or "Off" positions, the gate input is disconnected from the rest of the circuit except for its 125 Ω termination. Thus, signals at the gate input have no effect on the gate in these switch positions, although the input cable is still terminated in 125 Ω.

When the Gate Switch is in the "Ext." position, gate input signals are applied to the base of T_8 which is cut off. To achieve fast operation of the gate, a gating pulse of about -1V in excess of the -1.5V bias is required. Since the collector of T_8 rises to -3.1V, input signals should be no more negative than -3V, in order to prevent saturation of T_8. Thus, the gate pulse amplitude should lie between -2.5V and -3V. The presence of such an input causes the transferral of current from T_9 to T_8, producing the same conditions as when the Gate Switch is in the "On" position. Thus, a proper gate pulse switches D_1 and D_4 off and turns D_2 and D_3 on. When it returns to zero, the -1.5V bias pulls T_9 back into conduction, cutting off T_8 and restoring the circuit to the normal D.C. operating condition. The time required to switch the conducting diodes is 10-15 ns for 12 ns rise time, -2.8V pulses.

Gate (T_2 and T_3)

The decision to pass or not to pass an input signal is made by T_2 and T_3. For the Gate Switch in the "Off" or "Ext." positions with no gate input, D_1 and D_4 are conducting, thus causing T_2 to conduct and T_3 to be cut off by about 0.5V*. Thus, any increase in the collector current of T_1 coming from a signal input will pass into the emitter of T_2 and thence to ground on its collector. This holds for voltages on the

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* For small pedestal transients, small voltage swings on the bases of T_8 and T_9 are desired to reduce capacitive currents which produce an output "spike" when the gate turns on.

emitter of T_3 which do not become large enough to turn it on, resulting in a feedthrough of an input pulse to the output. In order to prevent this, low impedance should be used from the base of T_2 to -6.3V and thus a transistor of very low base spreading resistance and τ_o should be chosen. The 2N502A is a transistor with base spreading resistance of about 5 Ω and a typical τ_o of 0.4 ns. A 100 pF condenser was used to by-pass the bases of T_2 and T_3 in order to prevent fast signals from turning on T_3.

When the Gate Switch is in the "On" position, D_2 and D_3 are conducting and thus T_3 conducts with T_2 cut off. Thus, input signals from the collector of T_1 are passed into the emitter of T_3, emerging at its collector and passing on to the output via T_4. In this case it is also undesirable for the cut-off transistor to receive part of the input signal since this results in the output not being equal to the input. Thus, the same precautions taken at the base of T_2 are taken with the base of T_3.

In order to prevent the occurrence of a pedestal when T_3 turns on under the influence of a gate signal input (Gate Switch "Ext."), the voltage swing across the 1.2K resistor on the collector of T_3 is designed so that the current flowing through the 1.2K resistor decreases by the same amount that the current in T_3 increases if the Pedestal Adjust is correctly set. Thus, the D.C. currents flowing into the base of T_4 due to the gating pulses cancel and no D.C. pedestal results. Due to the collector-base capacity of T_3 and the stray capacity across the 1.2K resistor, a small amount of charge (~ 3 pC) will leak into the output. In order to cancel this charge, the capacitor C_1 carries an equal, but opposite charge from the base of T_4 if the A.C. Pedestal Adjustment is properly set.

Output Inverter and Multiplexer

Transistor T_4 acts as an inverter with a transfer impedance of 150 Ω and an output impedance less than 10 Ω, and thus it converts current coming from the collector of T_3 into a voltage at a low impedance.

Transistors T_5, T_6, and T_7 are three emitter followers driven by

T_4. The overall charge gain to one output is nearly one with the small charge losses due to transistor α's being made up by the transfer impedance of T_4 being slightly larger than 125 Ω.

III Construction

The circuit is built on a 11.5 cm x 20 cm copper plate with a 4.5 cm x 13 cm front panel. Ten of these - or similar - units plug into a 13 cm x 45 cm rack. (Fig. 4).

Signals as well as power lines connect through the rear printed circuit connector. The input attenuator selector switch, the gate toggle switch and the output monitor coax, are mounted on the front plate.

Small components are mounted on ceramic terminal strips with coaxial cables and D.C. wires underneath.

IV Performance

The linearity and feedthrough measurements used 10 ns wide, less than 1 ns rise time, rectangular pulses. The pedestal measurements used 500 ns wide, 12 ns rise time gating pulses. The output pulse of the gate circuit was shaped to a 50 ns wide critically damped pulse, using a passive pulse shaper network. (See Appendix I.) When terminated by 125 ohms the pulse shaper has an output amplitude of approximately 1/5 of the amplitude of a 10 ns wide input pulse.

The same pulse shaper was used to calibrate the input amplitude for the linearity and feedthrough measurements. (Fig. 5). A TC-2 amplifier - discriminator[5] was used as gate generator, providing a 50 ns wide gating pulse with 12 ns rise time and -3 volts amplitude. (Fig. 6). For the low level feedthrough measurement an auxiliary transistor distributed amplifier with a gain of 20, rise time of 2.8 ns was inserted.

The linearity and feedthrough properties of the gate are plotted on Fig. 7 and a typical output seen through the shaper is shown in Fig. 9.

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5) A. Barna, J. H. Marshall, M. Sands, "A Multifold Coincidence-Veto Circuit Using Transistors" (CTSL Report 17, 8, 1961.)

The output as a function of input can be approximated as

$$V_{out(shaper)} \cong \left[k_1 V_{in(shaper)}\right]^{1+\varepsilon}$$

where $|\varepsilon| < 3$ per cent and

$$k = 1 \pm 5\ \% \left[\text{volts}\right]^{-\varepsilon}$$

For $-50\ mV > V_{in} > -5.0V$ the linearity is better than $\pm$ 1 per cent of 5.0V. The feedthrough is < 0.2 per cent for $V_{in(shaper)} > -1.0V$.

The gate output as a function of signal input delay is plotted in Fig. 10, for 10 ns wide signal and 50 ns wide gating pulse (Fig. 6). It is constant within $\pm$ 2 per cent for $-0.25V > V_{in} > -5.0V$ and is constant within $\pm$ 5 per cent for $-0.05V > V_{in} > -5.0V$.

The output rise time vs. amplitude is plotted on Fig. 11. It is essentially a constant 7.4 ns up to -1V pulse height with approximately 10 ns at -3V. The absolute value of the D.C. pedestal is $< 5mV$, the A.C. pedestal on the output of the 50 ns shaper is within $\pm$ 15mV.

This gate has been used successfully in a preliminary nine counter telescope designed for the detection of K^+ mesons produced by photons from the Caltech 1.5 GeV synchrotron. On six of the nine counters, accurate biases and pulse height information have been required in the presence of high singles counting rates. Thus, the need arose for the above gate which is not only stable and linear but fast and free from pile-up at input counting rates in excess of 1Mc. The fact that the telescope has operated as expected indicates that the gate meets the requirements for which it was designed.

At present, plans are being made to expand the telescope to about fifteen counters, most of which will be gated by the above circuit. With this telescope, it should be possible to detect K^+ mesons with a known efficiency over a large range of energy and angle.

APPENDIX I.

50 ns pulse shaper

For a delta function input of Q from a 125 Ω source the response of the shaper (Fig. 12) into a 125 Ω load can be written as:

$$i_{out} = \frac{Q}{2\tau} \frac{t}{\tau} \exp(-t/\tau)$$

where $\tau = 20$ ns.

The rise time $T_R = 0.56\ \tau = 11.2$ ns, the half width $T_{1/2} = 2.4\ \tau = 48$ ns and the time of the peak $T_{max} = \tau = 20$ ns.

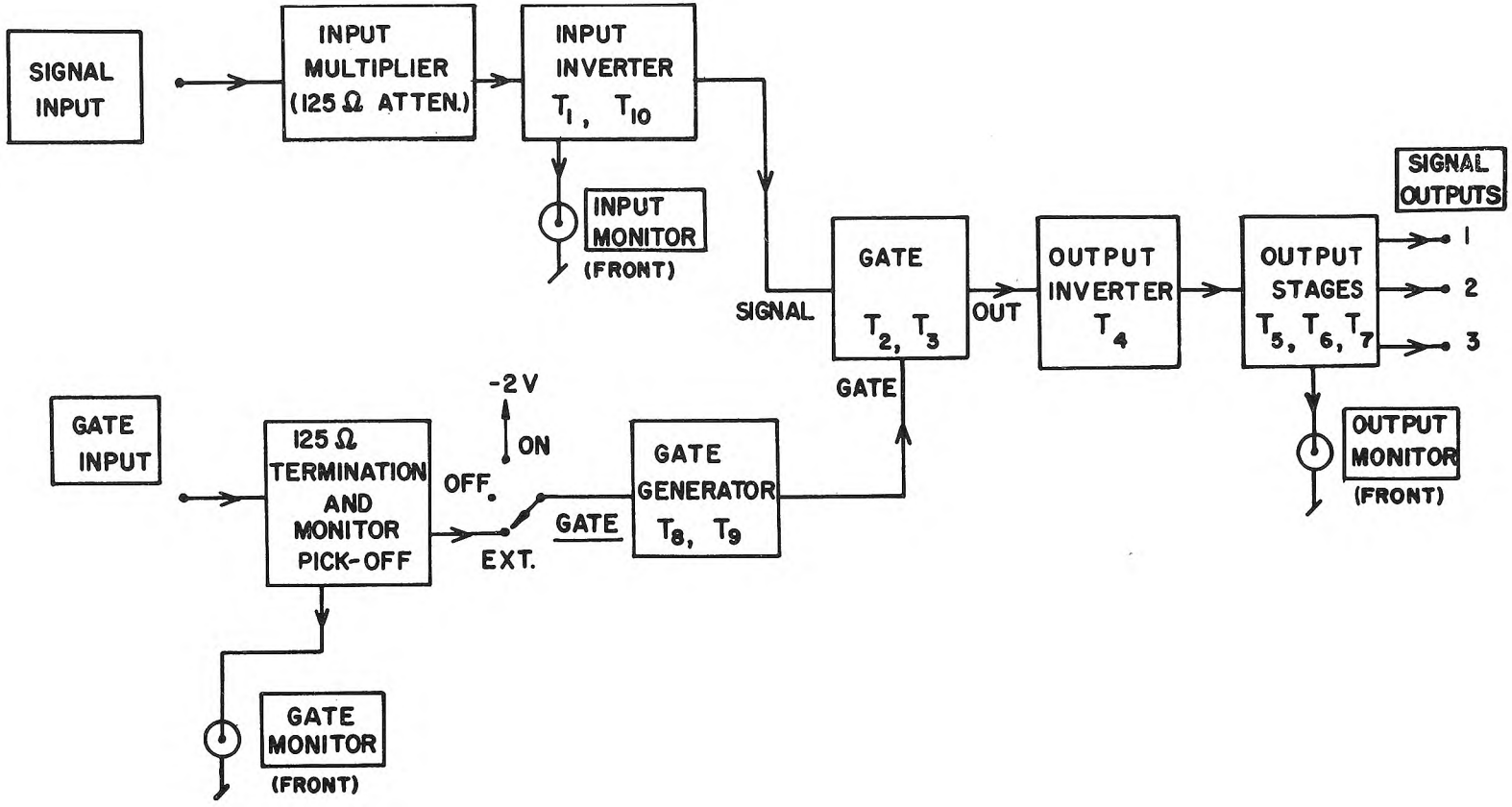


FIG. 1 BLOCK DIAGRAM

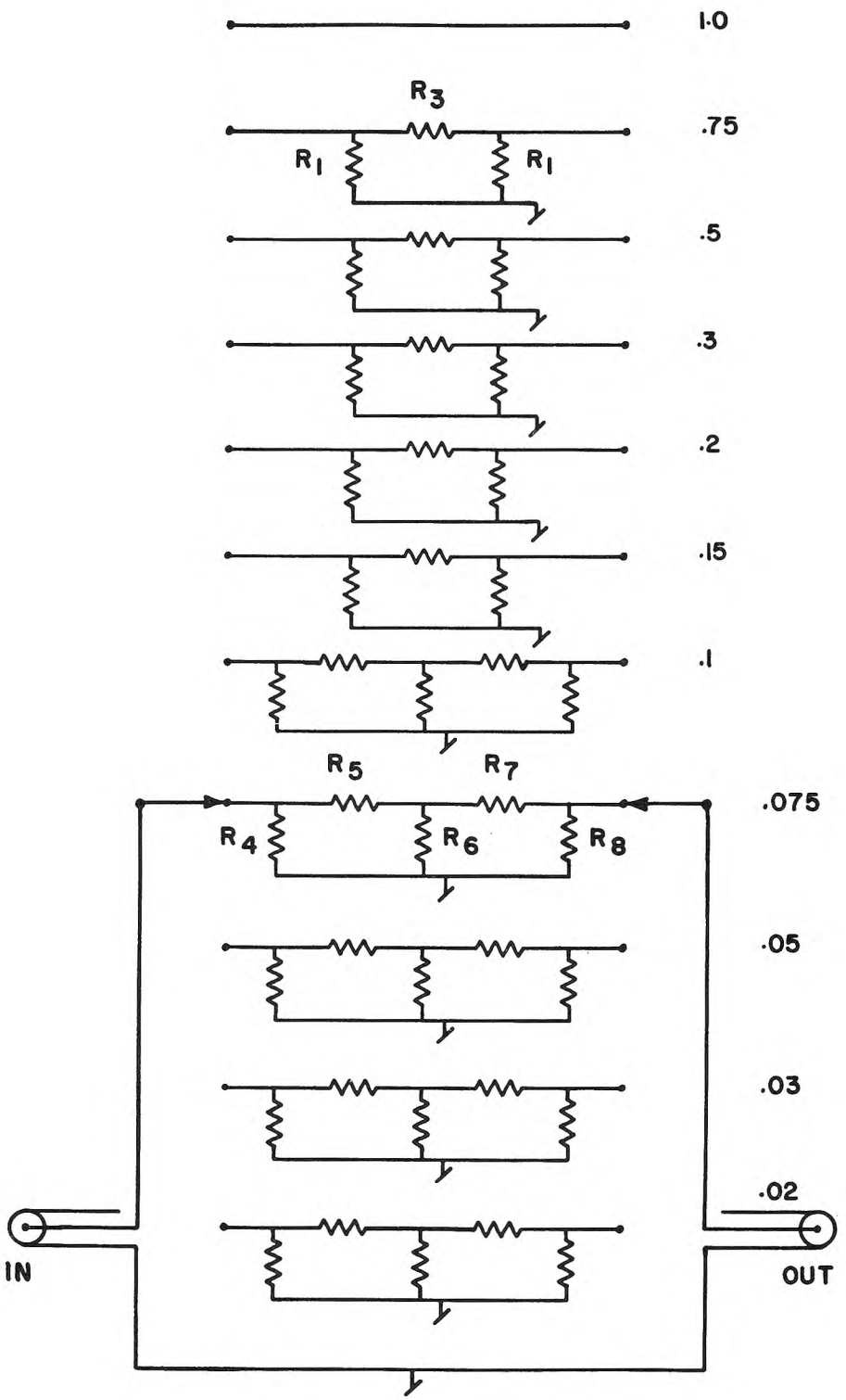
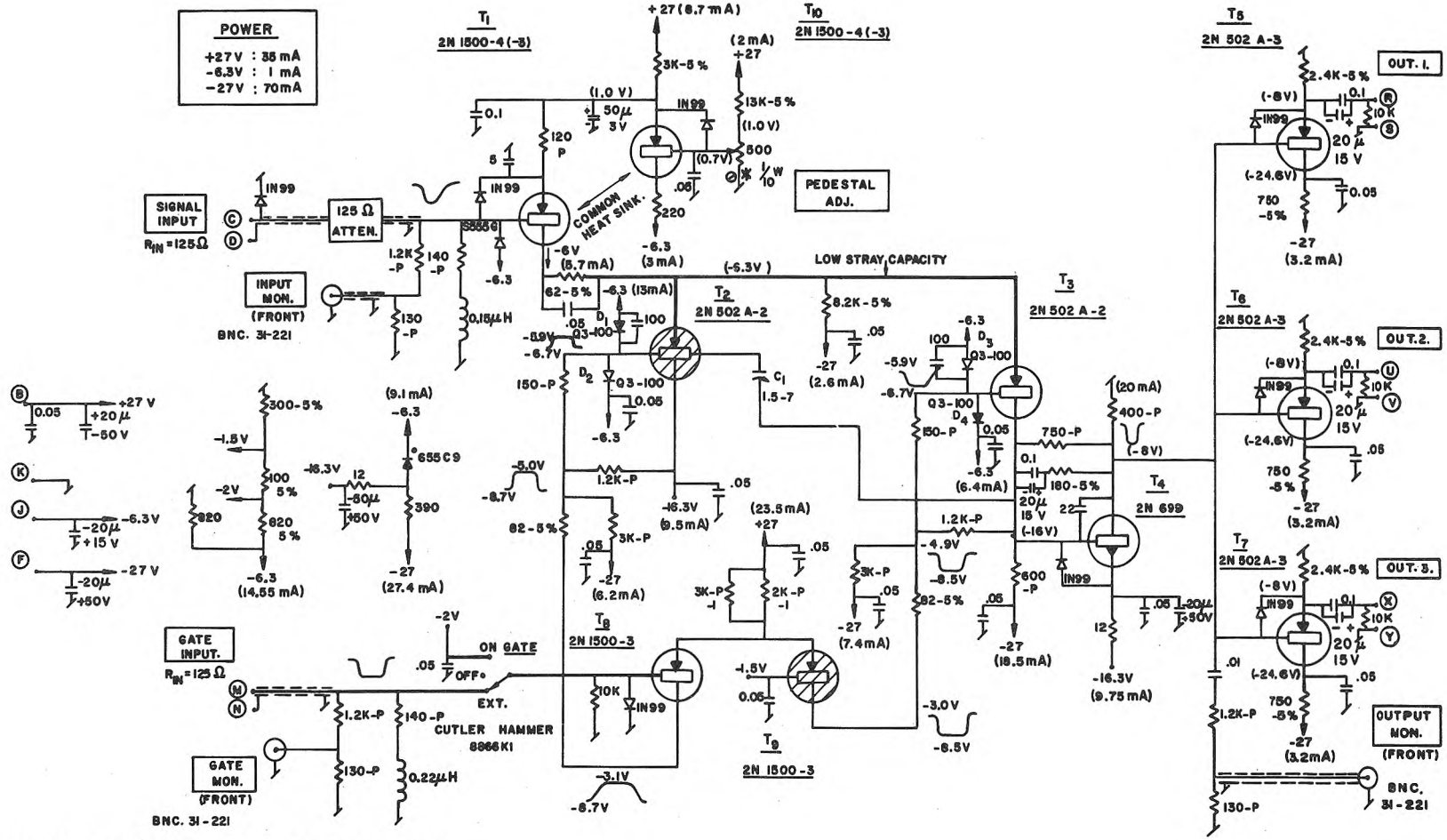


FIG. 2. 125Ω ATTENUATOR.



ALL RESISTORS 1/2W 10% UNLESS OTHERWISE NOTED.

ALL COAX CABLES SURPRENANT #9923

ALL CAPACITORS 50 V CERAMIC DISK UNLESS OTHERWISE NOTED.

FIG. 3 GATE SCHEMATIC.

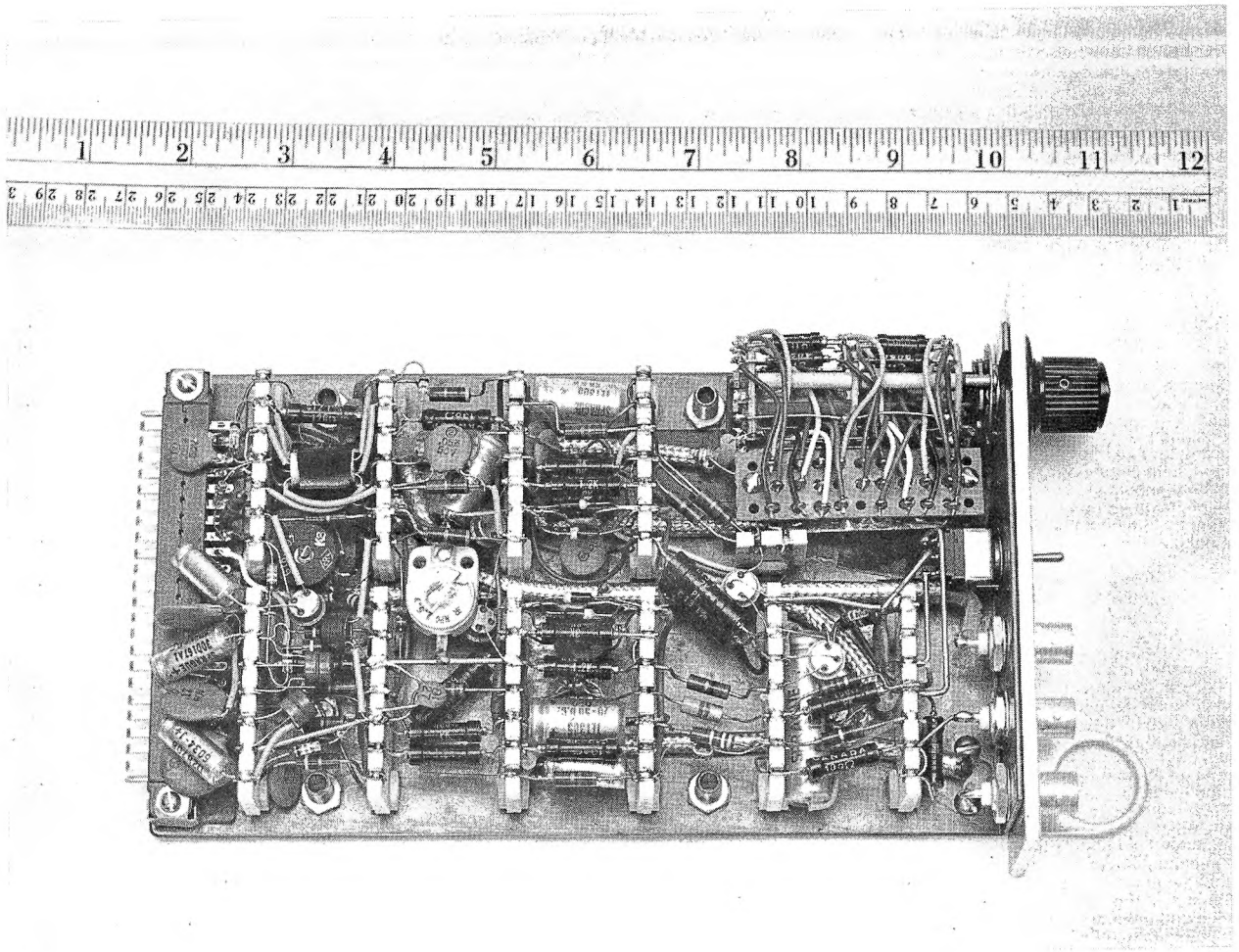
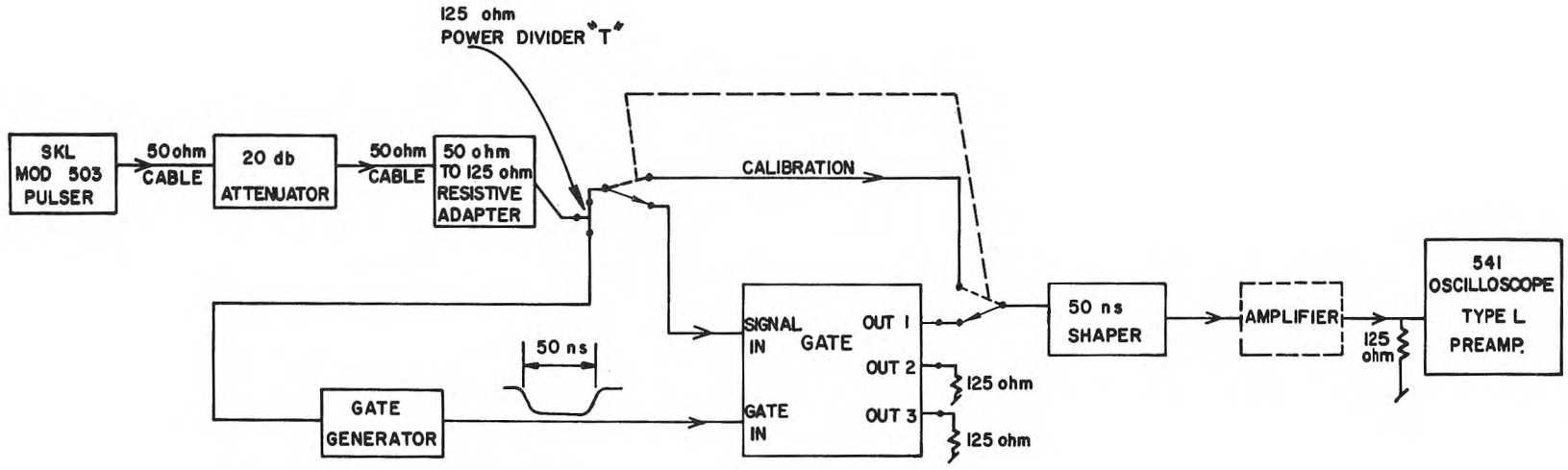


Fig. 4. Photograph of the gate,
with the shield removed.



CABLES 125 ohm, UNLESS OTHERWISE MARKED

FIG. 5. TEST SETUP

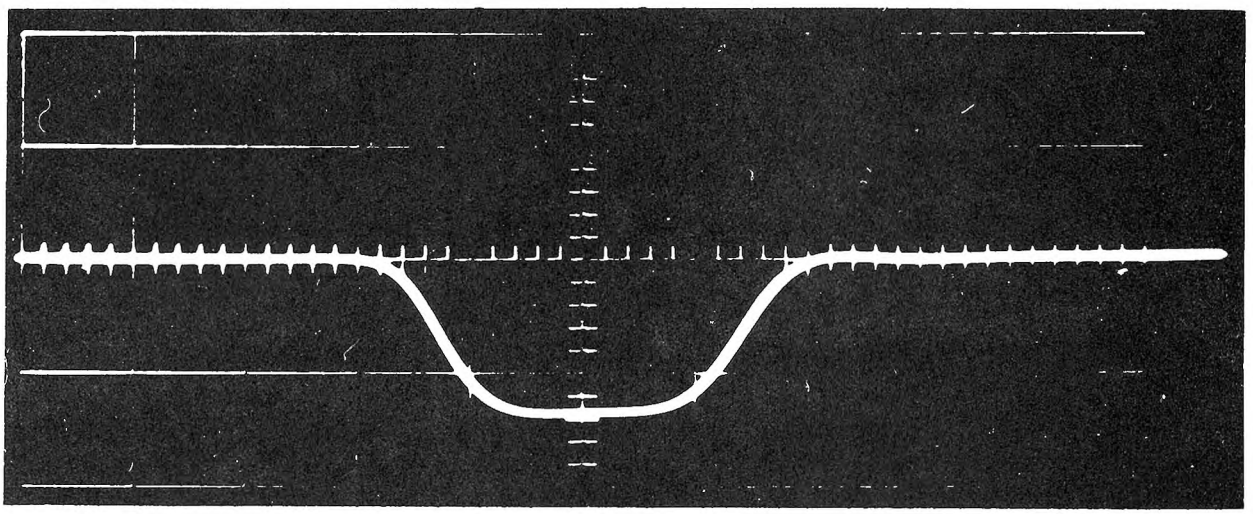


Fig. 6. Gating Pulse generated by TC-2.

Tektronix 541 scope, Type L preamp.

2V/Major division. 20 ns/Major division.

Scope Rise Time = 12 ns.

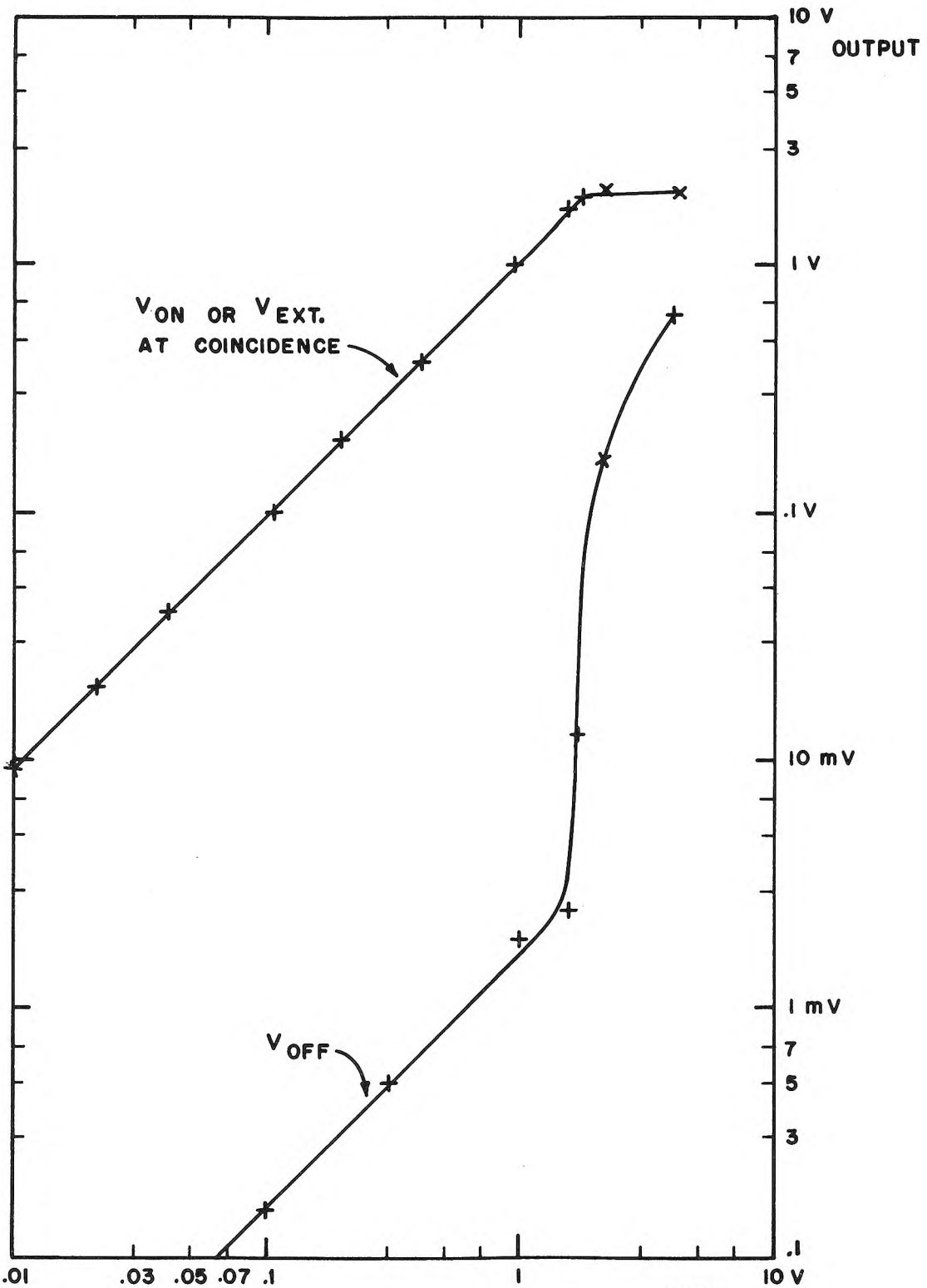


FIG. 7. LINEARITY AND FEEDTHROUGH.

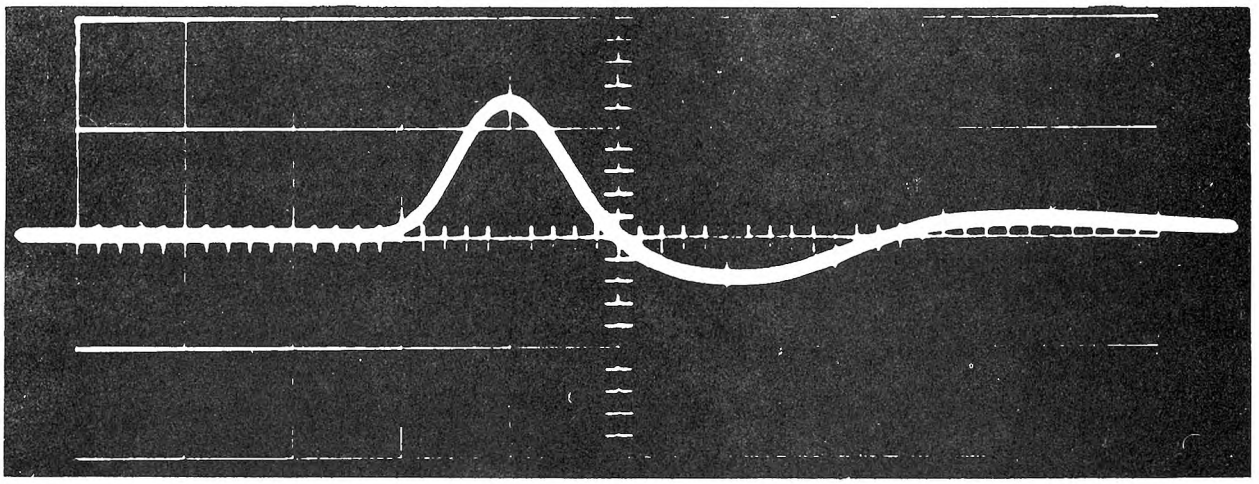


Fig. 8. Pedestal for no signal input and gate input of Fig. 6. 10 mV/Major division. 20 ns/Major division.

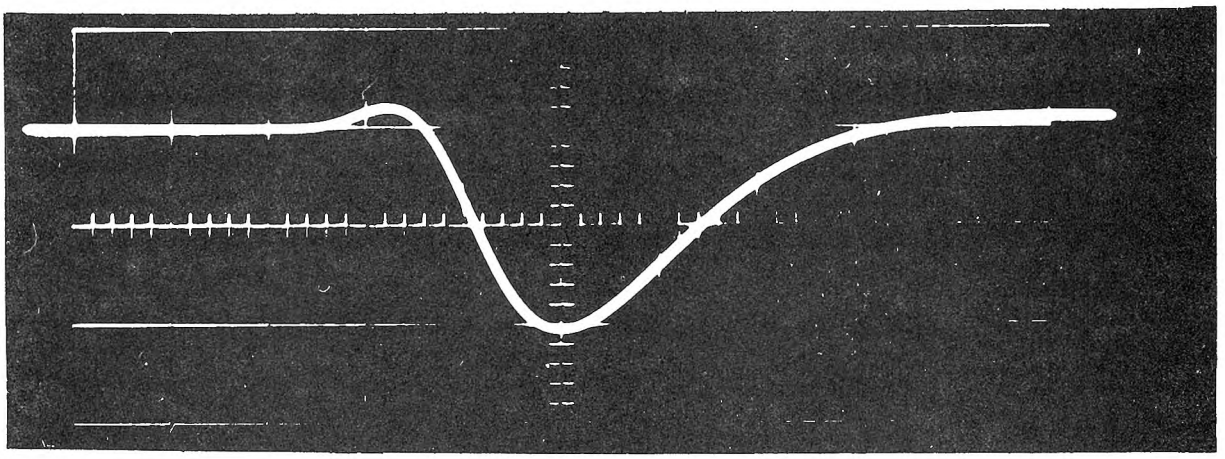


Fig. 9. Output for 0.5V, 10 ns input in coincidence with the gate of Fig. 6. 50 mV/Major division. 20 ns/Major division.

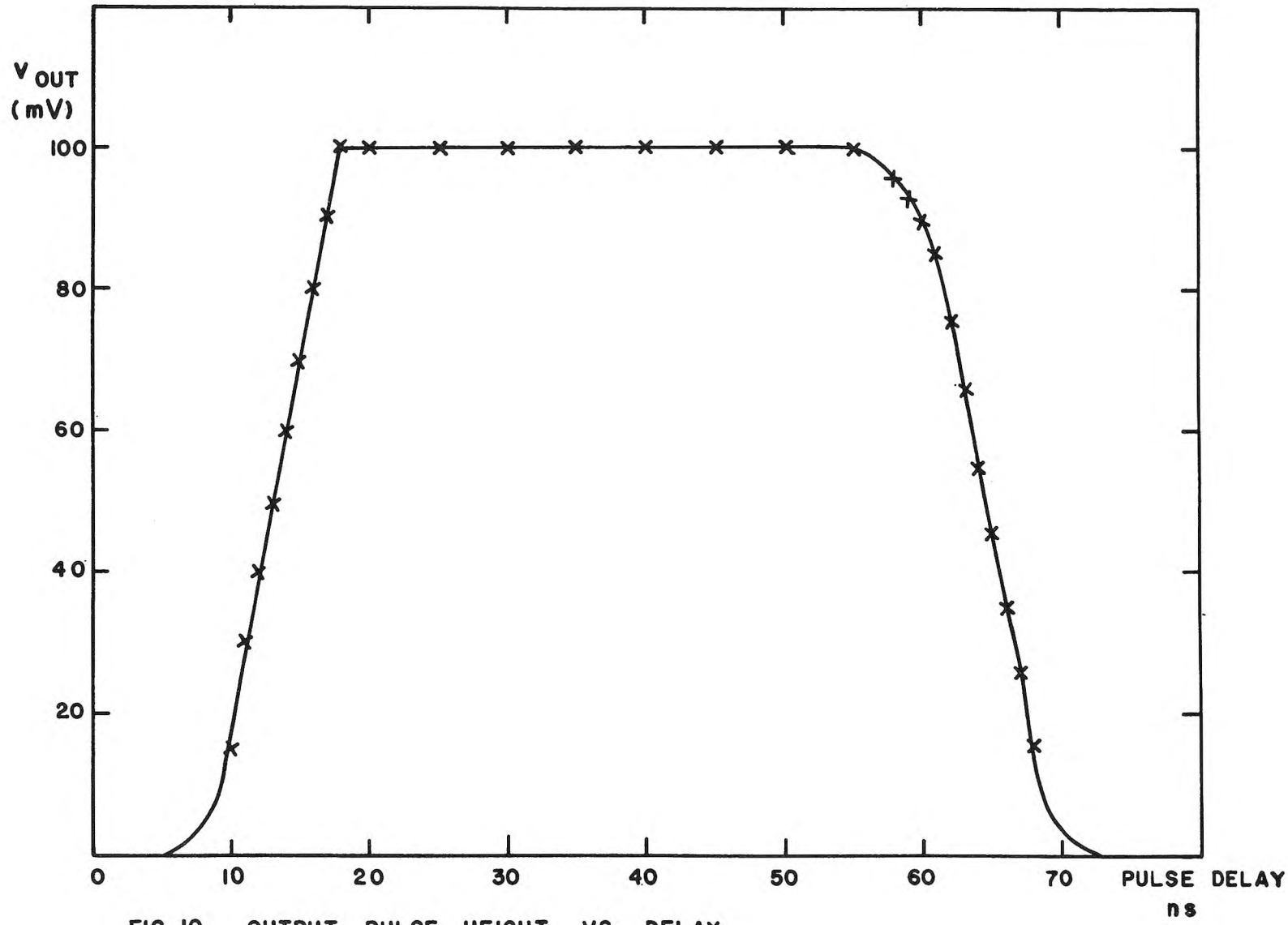


FIG. 10. OUTPUT PULSE HEIGHT VS. DELAY

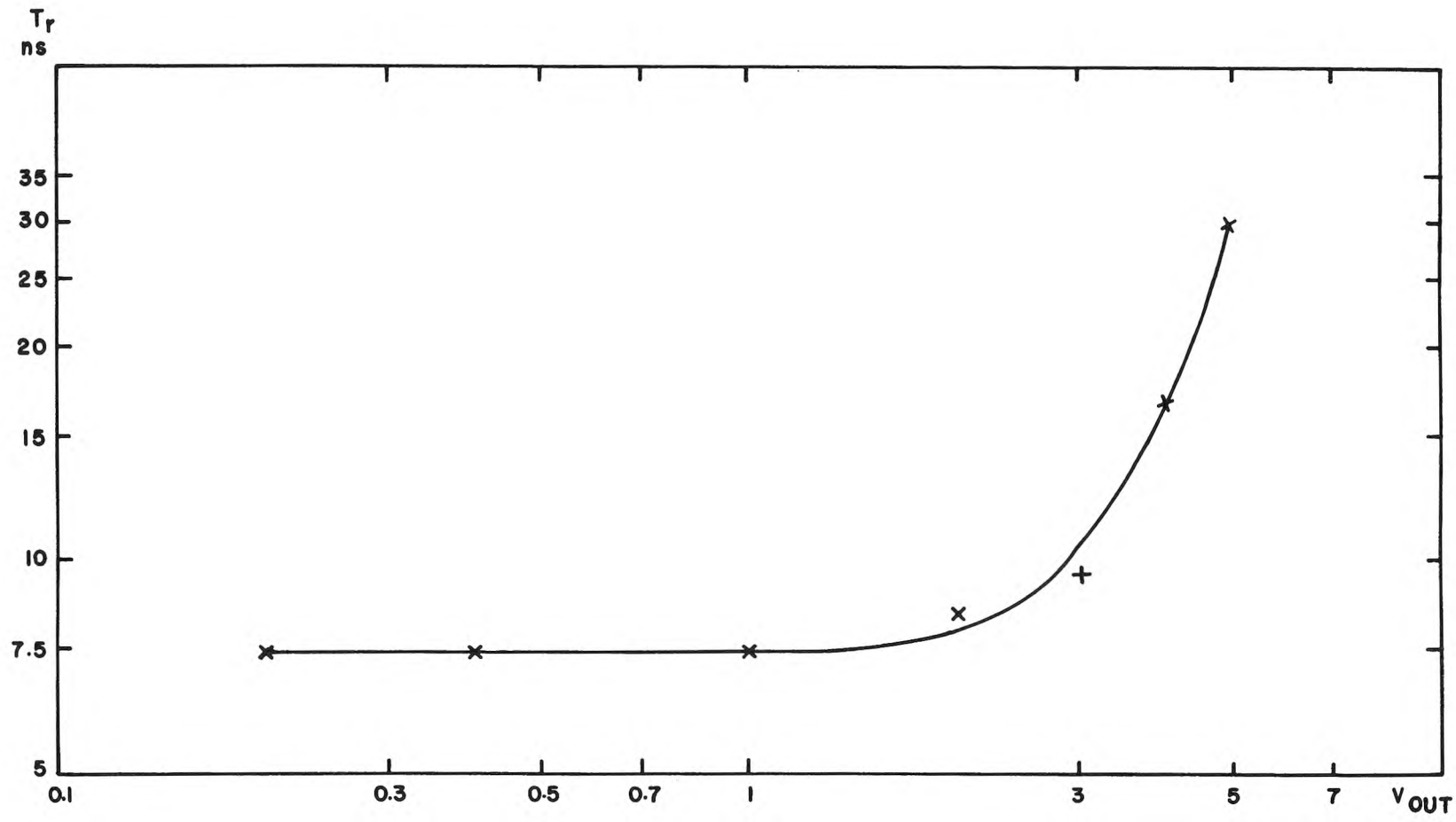


FIG. 11. RISETIME VS. OUTPUT PULSE HEIGHT.

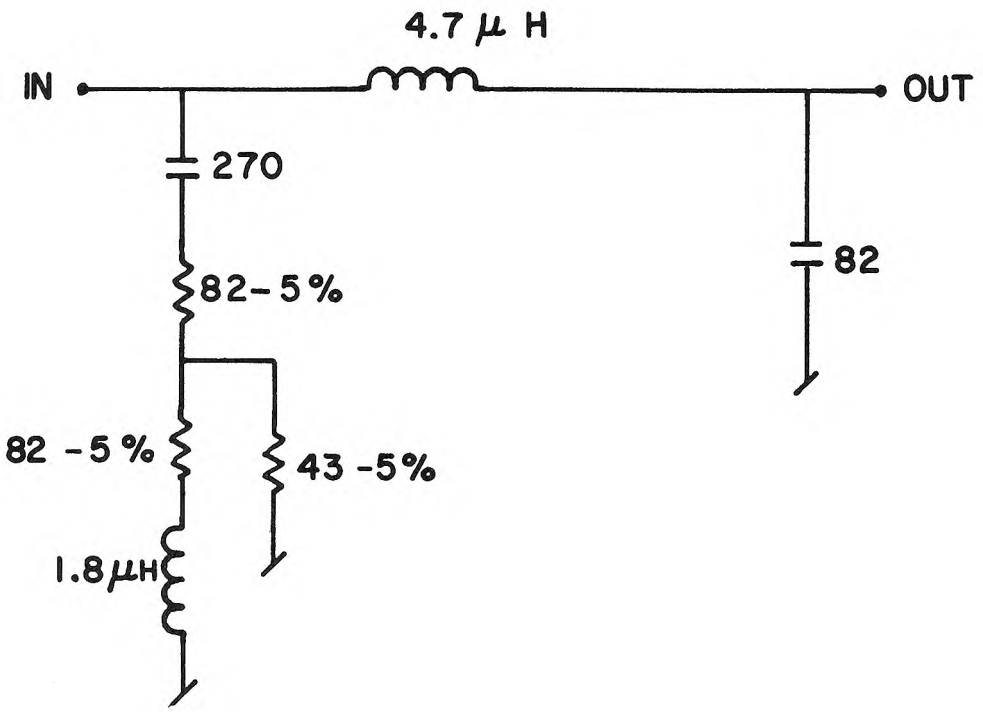


FIG. 12. 50 ns PULSE SHAPER